

19-3425; Rev 0; 10/04

EVALUATION KIT
AVAILABLE

MAXIM

Single-Chip Global Positioning System Receiver Front-End

General Description

The MAX2745 complete single-chip global positioning system (GPS) RF front-end downconverter utilizes many innovative and leading-edge RF CMOS design techniques. This high-performance, state-of-the-art device consumes extremely low power and eliminates the need for costly SAW and bulky discrete IF filters. The MAX2745 incorporates a fully integrated low-noise amplifier (LNA) and mixer, IF section, digital sampler, and local oscillator synthesizer. The MAX2745 also provides a voltage supply for an external LNA. In addition, the MAX2745 features a voltage booster, which can extend the power-supply voltage to as low as 1.6V.

The MAX2745 supports both 3rd overtone crystal designs in 32MHz and fundamental frequency crystal designs in 16MHz, as well as a TCXO implementation. In addition, the MAX2745 incorporates an on-chip temperature sensor and crystal oscillator with trimmed capacitors, resulting in a very accurate frequency and additional system cost savings.

The MAX2745 is available in a space-saving 48-pin TQFP package and is specified for the extended (-40°C to +85°C) temperature range. The power consumption of this device is as low as 41mW at 2.4V.

Applications

- In-Vehicle Navigation Systems (IVNSs)
- Location-Based Services (PDAs and Accessories)
- Telematics (Vehicle/Asset Tracking and Inventory Management)
- Recreational Handheld/Walkie Talkies
- Geographical Information Systems (GISs)
- Emergency Roadside Assistance
- Emergency Response Systems
- Digital Cameras/Camcorders
- Consumer Electronics

Features

- ◆ Complete Single-Chip GPS Radio for 16.368MHz and 32.736MHz Floorplans
- ◆ Single-Ended or Differential Outputs at 4.092MHz
- ◆ Low 3.5dB Typical Noise Figure
- ◆ No External IF SAW or Discrete Filters Required
- ◆ On-Chip Temperature Sensor
- ◆ 2.4V to 3.6V Operational Supply Voltage Range
- ◆ Power Consumption as Low as 41mW at 2.4V
- ◆ Wide -40°C to +85°C Operational Temperature Range

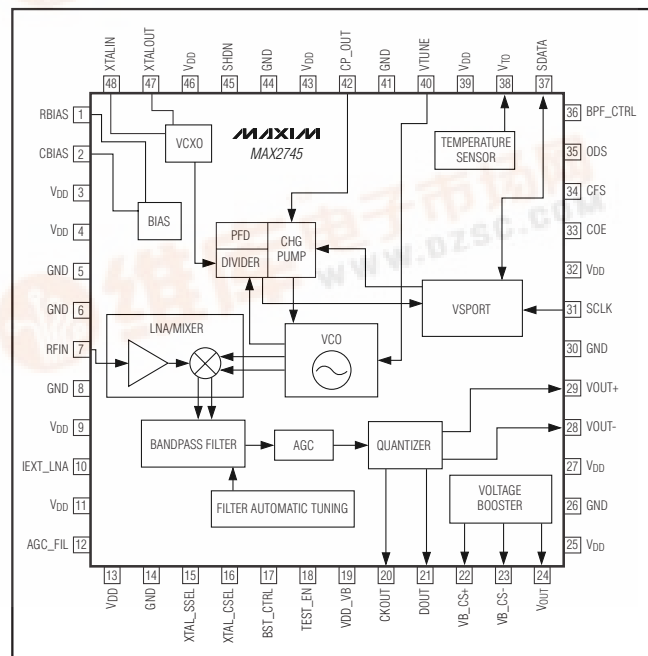
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX2745ECM	-40°C to +85°C	48 TQFP-EP*

*EP = Exposed paddle.

Typical Operating Circuit appears at end of data sheet

Block Diagram/ Pin Configuration



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ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND-0.3V to +3.7V
 Other Pins to GND-0.3V to (V_{DD} + 0.3V)
 RF LNA Input Power+10dBm
 Continuous Power Dissipation (T_A = +70°C)
 48-Pin TQFP-EP (derate 12.5mW/°C above +70°C)1W
 Operating Temperature Range-40°C to +85°C

Junction Temperature+150°C
 Storage Temperature Range-65°C to +150°C
 Soldering Temperature (10s)+300°C



CAUTION! ESD SENSITIVE DEVICE

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(MAX2745 EV kit, V_{DD} = +2.4V to +3.6V, SHDN = GND, T_A = -40°C to +85°C. Typical values are at V_{DD} = +3.0V and T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage		2.4		3.6	V
Supply Current	V _{DD} = +3.0V, T _A = +25°C (Note 1)		20.5	27	mA
	Shutdown mode		11		µA
Optional External LNA Supply Current	V _{DD} = +3.0V			10	mA
Logic-Input High Voltage		2.0			V
Logic-Input Low Voltage				0.5	V
Logic-Input Bias Current		-10		+10	µA

AC ELECTRICAL CHARACTERISTICS

(MAX2745 EV kit, V_{DD} = +2.4V to +3.6V, SHDN = GND, T_A = -40°C to +85°C. Typical values are at V_{DD} = +3.0V and T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL PERFORMANCE					
Maximum Conversion Gain	(Notes 2, 3)		105	120	dB
Input Frequency			1575.42		MHz
Noise Figure	Measured at quantizer output		3.5		dB
Return Loss (S11)			-14		dB
LNA/Mixer Input IP3	f ₁ = 5.09MHz and f ₂ = 7.09MHz above carrier frequency		-25		dBm
Output IF Frequency			4.092		MHz
OUTPUT STAGE					
Output Rise/Fall Time	Differential (VOUT+, VOUT-), C _L < 20pF		16		ns
	Single ended (DOUT), C _L < 20pF		6		
Output-Voltage-Level Low	Differential		V _{DD} - 0.9		V
	Single ended		0		
Output-Voltage-Level High	Differential		V _{DD}		V
	Single ended		V _{DD}		

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AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2745 EV kit, $V_{DD} = +2.4V$ to $+3.6V$, SHDN = GND, $T_A = -40^{\circ}C$ to $+85^{\circ}C$. Typical values are at $V_{DD} = +3.0V$ and $T_A = +25^{\circ}C$, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SYNTHESIZER					
Crystal Input Frequency	Fundamental frequency crystal		16.368		MHz
	3rd overtone crystal		32.736		
Charge-Pump Current			0.4		mA
Phase Noise	$f_{OFFSET} = 10kHz$ offset, $BW_{LOOP} = 70kHz$		-81		dBc/Hz
	$f_{OFFSET} = 1MHz$ offset, $BW_{LOOP} = 70kHz$		-104		
Maximum PLL Spur	$BW_{LOOP} = 70kHz$		-39		dBc
VCO Tuning Frequency Range	(Notes 2, 3)	150	210	270	MHz
VCO Tuning Gain	(Notes 2, 3)	150	210	310	MHz/V
IF STAGE					
IF Stage Gain	VGA set at maximum gain		80		dB
Dynamic Range IF Stage Gain			56		dB
Bandpass Filter 1dB Corner Frequency	Low-frequency corner		3.1		MHz
	High-frequency corner		5.1		
Bandpass Filter 3dB Bandwidth			2.0		MHz
Bandpass Filter 60dB High-Side Rejection			6.6		MHz
Bandpass Filter 60dB Low-Side Rejection			1.6		MHz
Image Rejection			17		dB
In-Band Ripple			1		dB
AGC Loop Lock Time			1		ms

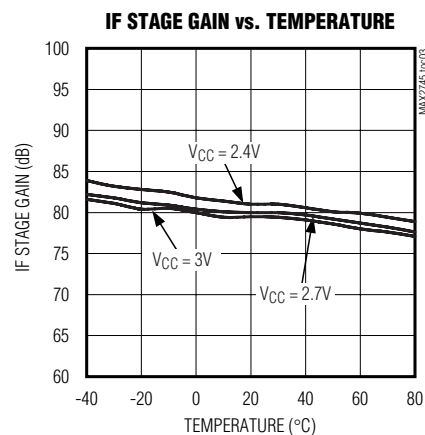
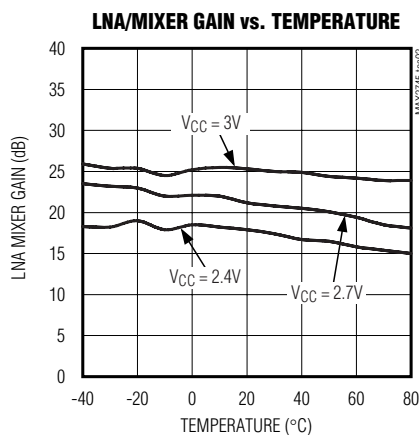
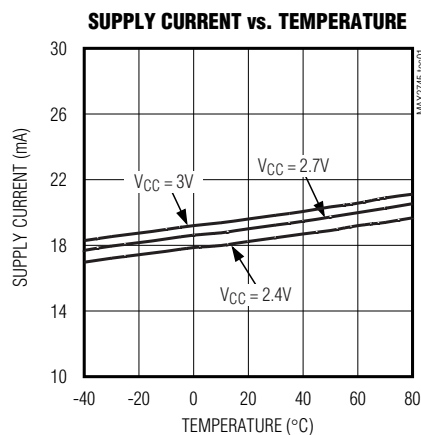
Note 1: At $T_A = +25^{\circ}C$, min/max limits are guaranteed by production test.

Note 2: At $T_A = -40^{\circ}C$, min/max limits are guaranteed by design and characterization.

Note 3: At $T_A = +25^{\circ}C$ and $+85^{\circ}C$, min/max limits are guaranteed by production test.

Typical Operating Characteristics

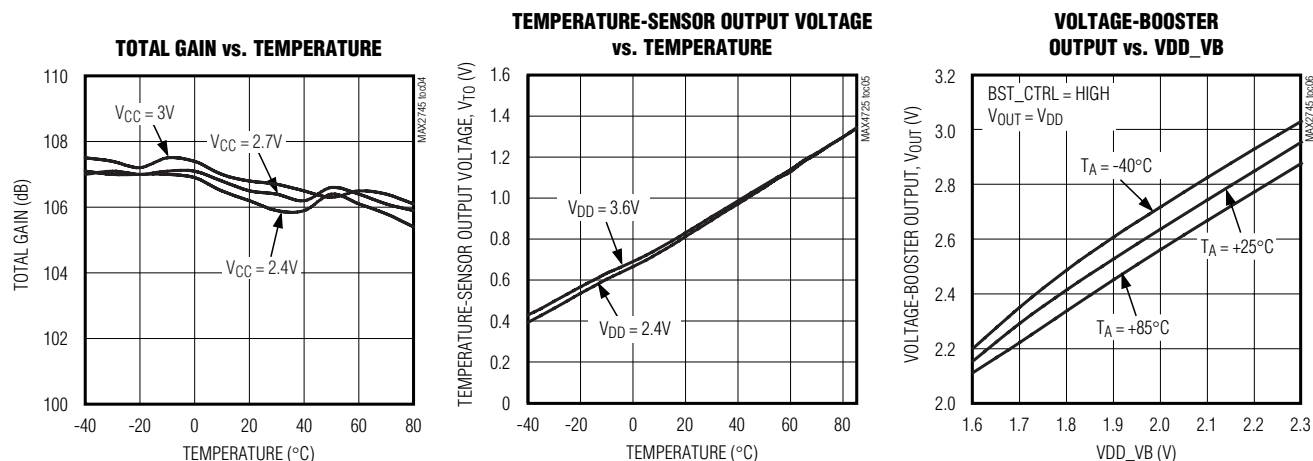
(MAX2745 EV kit, $V_{DD} = +3.0V$, SHDN = GND, $f_{RF} = 1575.42MHz$, and $T_A = +25^{\circ}C$, unless otherwise noted.)



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Typical Operating Characteristics (continued)

(MAX2745 EV kit, $V_{DD} = +3.0V$, SHDN = GND, $f_{RF} = 1575.42MHz$, and $T_A = +25^\circ C$, unless otherwise noted.)



Pin Description

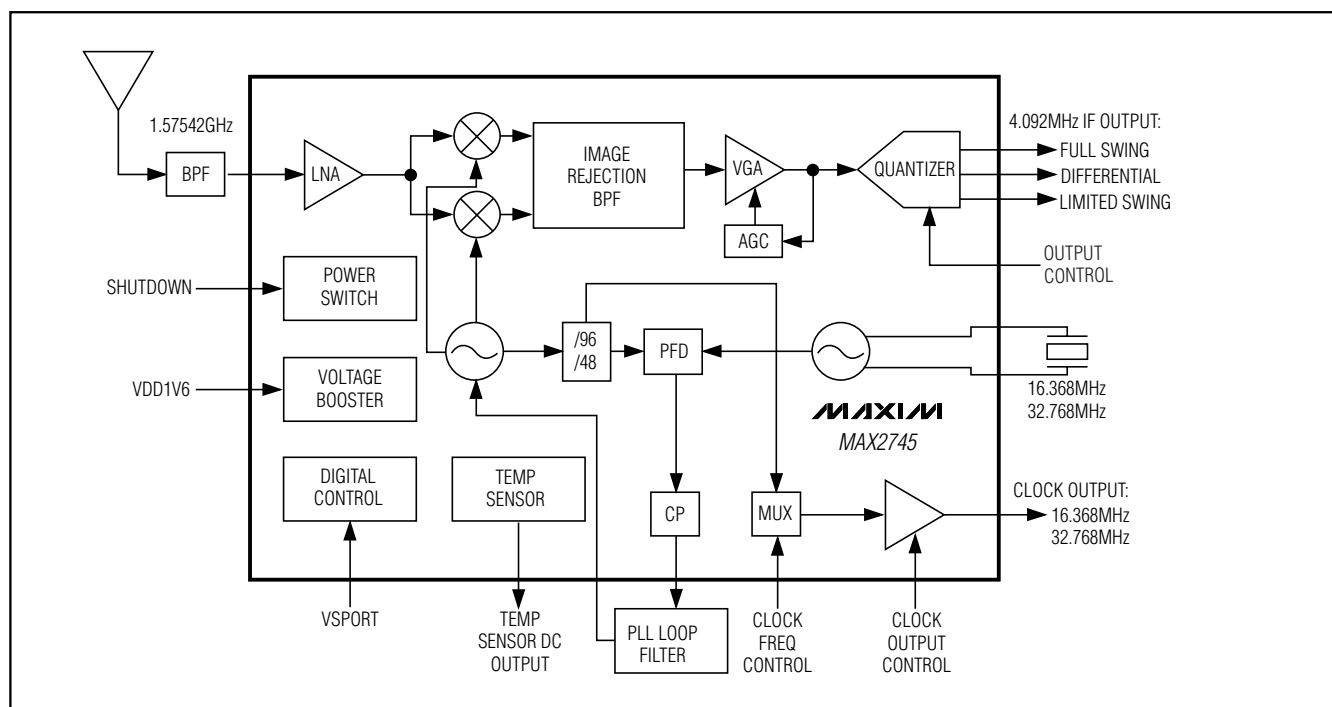
PIN	NAME	FUNCTION
1	RBIAS	External BIAS Resistor. For normal bias, connect a 100k Ω (1%) resistor to ground.
2	CBIAS	BIAS Bypass Capacitor. Connect a 0.1 μF capacitor to ground.
3, 4, 9, 11, 13, 25, 27, 32, 39, 43, 46	V_{DD}	Power-Supply Voltage. Bypass with a 0.1 μF capacitor to ground as close to the pins as possible.
5, 6, 8, 14, 26, 30, 41, 44	GND	Ground
7	RFIN	RF Input Signal. Requires external matching network.
10	IEXT_LNA	External LNA Voltage Supply
12	AGC_FIL	AGC External Filter. Requires external RC lowpass filter.
15	XTAL_SSEL	Crystal Swing Select. Drive logic high for full swing. Drive logic low for limited swing.
16	XTAL_CSEL	Crystal Clock Select. Drive logic high for fundamental mode of 16.368MHz. Drive logic low for third overtone mode of 32.736MHz.
17	BST_CTRL	Active-High Boost Control Input. Drive logic high to activate the voltage booster (crystal oscillator is biased from BIAS). Drive logic low to deactivate the voltage booster (crystal oscillator is self-biased).
18	TEST_EN	Connect to Ground for Normal Operation
19	V_{DD_VB}	Power Supply for Voltage Booster. Connect to V_{DD} if voltage booster is not used.
20	CKOUT	Full-Swing Clock Output
21	DOUT	Single-Ended Full-Swing Digital Output
22	VB_CS+	Positive Voltage Booster External Floating CAP. Connect a 6nF capacitor to GND.
23	VB_CS-	Negative Voltage Booster External Floating CAP. Connect a 6nF capacitor to GND.
24	V_{OUT}	Voltage Booster Output. Bypass to GND with a 1 μF capacitor as close to the pin as possible.

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Pin Description (continued)

PIN	NAME	FUNCTION
28	VOUT-	Quantizer Analog Negative Limited-Swing Output
29	VOUT+	Quantizer Analog Positive Limited-Swing Output
31	SCLK	Serial Port Clock Input (Bidirectional PAD)
33	COE	Clock Output Enable. Drive logic high to enable the clock output. Drive logic low to disable the clock output.
34	CFS	Clock Frequency Select. Drive logic high to select 16MHz. Drive logic low to select 32MHz.
35	ODS	Output Data Select. Drive logic high to select full-swing output. Drive logic low to select limited-swing output.
36	BPF_CTRL	Bandpass Filter (BPF) Control. Drive logic high to activate the tuning block control BPF. Drive logic low to let BPF be controlled by fuses.
37	SDATA	Serial Port Data (Bidirectional PAD)
38	TEMPOUT	Temperature Sense DC Voltage Output
40	VTUNE	VCO Tuning Input
42	CP_OUT	PLL Charge-Pump Output. Analog high-impedance output. Current source. Connect directly to the PLL loop filter input.
45	SHDN	Active-High Shutdown Input. Drive logic low to disable all device functions. Drive logic high for normal operation.
47	XTALOUT	Crystal Output. Connect directly to the external crystal.
48	XTALIN	Crystal Input. Connect directly to the external crystal or TCXO.

Functional Diagram



Single-Chip Global Positioning System Receiver Front-End

Detailed Description

The MAX2745 complete single-chip GPS front-end downconverter utilizes many innovative and leading-edge RF CMOS design techniques. This high-performance, state-of-the-art device consumes extremely low power and eliminates the need for costly SAW and bulky discrete IF filters. The MAX2745 incorporates a fully integrated LNA/mixer, IF section, digital sampler, and local oscillator synthesizer. The MAX2745 also provides voltage supply for an external LNA. In addition, the MAX2745 features a voltage booster that can extend the power-supply voltage to as low as 1.6V.

The MAX2745 supports both 3rd overtone crystal designs in 32MHz and fundamental frequency crystal design in 16MHz, as well as a TCXO implementation. In addition, the MAX2745 incorporates an on-chip temperature sensor and crystal oscillator with trimmed capacitors, resulting in a very accurate frequency and additional system cost savings.

The MAX2745 also incorporates a 2MHz bandwidth bandpass filter to reduce off-band noise. The bandwidth and the center frequency of the bandpass filter are guaranteed by an advanced tuning scheme.

The MAX2745 is offered in a space-saving 48-pin TQFP package. The operational temperature range is specified from -40°C to +85°C. The power consumption of this device is as low as 41mW at 2.4V.

LNA/Mixer

The RF input signal from the GPS antenna is fed through an LNA with a gain of 20dB. The amplified signal is then fed to a mixer that downconverts the signal (1575.42MHz) to a quadrature differential IF of 4.092MHz.

IF Stage

The quadrature IF signals pass through the IF filter, which rejects the out-of-band spurs by more than 60dB and the image noise by 17dB (typ). After the image reject filter, the signal is converted from quadrature to differential. The filtered IF signal is then amplified by the AGC block, which sets the VGA output signal level to a predetermined value through the application using 56dB of dynamic range.

IF Output Selection

The sampled outputs of the GPS signal are available in a single-ended or limited-differential format. The ODS pin controls the output format.

Synthesizer

An on-chip VCO provides quadrature differential LO signals to the downconverting mixer. An on-chip crystal

oscillator driver generates the reference frequency. The integrated synthesizer includes the VCO, crystal oscillator driver, main frequency divider, phase-frequency detector, and charge pump. It uses an off-chip PLL loop filter and crystal. If a TCXO is used, connect the output of the TCXO to XTALIN.

The main division ratio for the synthesizer is 96 or 48. With this division ratio, a low-side injection LO can be used with a 16.368MHz or 32.736MHz crystal. Note that if a 3rd overtone crystal is used for the 32.736MHz, an off-chip notch filter to reject the fundamental frequency is required. The notch filter can be built with one inductor and one capacitor.

Control Block

This block is used mainly for testing purposes and to set the internal trimmed capacitor. This block is programmed through the VSPORT.

VSPORT Serial Data Interface

The serial interface within the MAX2745 is used by the baseband to communicate control signals and is also used for internal testing of the device. (This serial port is described in a separate document, which is available upon request.)

Trimmed VCXO Frequency

An on-chip, trimmed capacitor with a temperature coefficient of better than 30ppm/°C is used to compensate for the component variation of the reference frequency associated circuitry. The value of the capacitor is programmed in 512 binary steps and ranges from a minimum of 80fF to a maximum of 40pF, $\pm 20\%$. Programming is accomplished with the VSPORT serial interface. The no load capacitance on the crystal out follows the equation:

$$C(\text{no load}) = ([\text{Register Value}] \times 40/512) \text{ pF}$$

Upon power-up, the capacitor value is set to the minimum value. This enables the MAX2745 to work with an off-chip, trimmed capacitor. If the baseband has the capability of programming the radio, the off-chip, trimmed capacitor can be omitted by setting the internal trimmed capacitor through the VSPORT.

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Temperature Sensor

The MAX2745 features an on-chip temperature sensor to facilitate system temperature compensations in conjunction with the trimmed capacitor. This circuit generates an output voltage at TEMPOUT, which is used to approximate the temperature by the following equation:

$$T = T_O + (V_{OUT} - V_{OUT,T_O})/SG$$

where SG is the sensor gain, T_O is factory-trimmed temperature, which can be any value (normally +27°C), and V_{OUT} is the temperature output voltage at T_O . The coefficient SG in the above equation is targeted to be between 6mV/°C and 8mV/°C, depending on the temperature.

Voltage Booster

The MAX2745 integrates an internal voltage booster to allow proper operation with supply voltages as low as 1.6V. The circuit includes two 6nF floating external capacitors connected to VB_CS± (pins 22 and 23) and a 1μF capacitance to VOUT (boosted voltage output, pin 24). To reduce the output voltage ripple, use an external LC lowpass filter, which can be built with two inductors and one capacitor.

Applications Information

Operation with Voltage Booster

Under normal operating conditions, the recommended power-supply voltage ranges from 2.4V to 3.6V. But with the integrated voltage booster on-chip, the MAX2745 can be powered from power-supply voltages as low as 1.6V, and only requires a minimal number of external components. This is not the most efficient operating mode, since the power efficiency will be lowered to less than 50%.

As described in the *Detailed Description* section, to use the voltage booster, connect 6nF floating capacitors to

VB_CS±, pins 22 and 23, and 1μF bypass capacitor to VOUT, pin 24. Connect VOUT (pin 24) to all the power-supply (VDD) pins and pull BST_CTRL, pin 17, high to activate the booster. Then the MAX2745 can be powered from supply voltages ranging from 1.6V to 2.3V at VDD_VB, pin 19, and the voltage booster output can source up to 25mA current. It is recommended that the voltage booster be used as a backup supply. To do this, additional circuits including a voltage monitor and a switch are needed. These components are inexpensive and can be found in the Maxim product family.

Layout Issues

A properly designed PC board is an essential part of any RF/microwave circuit. Use the MAX2745 EV kit as a guide. Use controlled-impedance lines on all frequency inputs and outputs. Use low inductance connections to ground on all ground pins and wherever the components are connected to ground. Place decoupling capacitors close to all VCC connections. For proper operation, connect the metal exposed paddle at the back of the IC to the PC board ground plane with multiple vias.

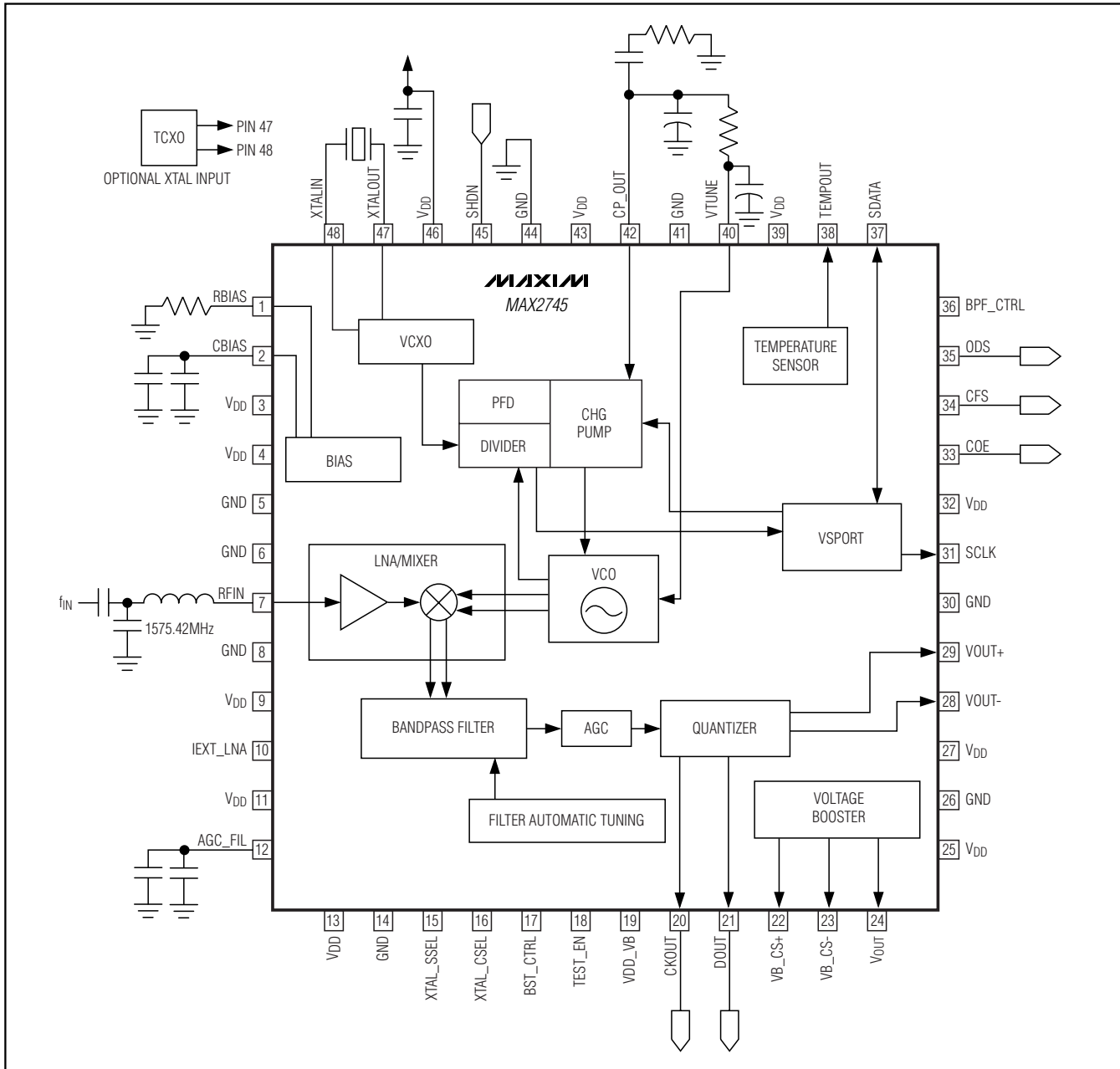
Chip Information

TRANSISTOR COUNT: 9205

PROCESS: CMOS

Single-Chip Global Positioning System Receiver Front-End

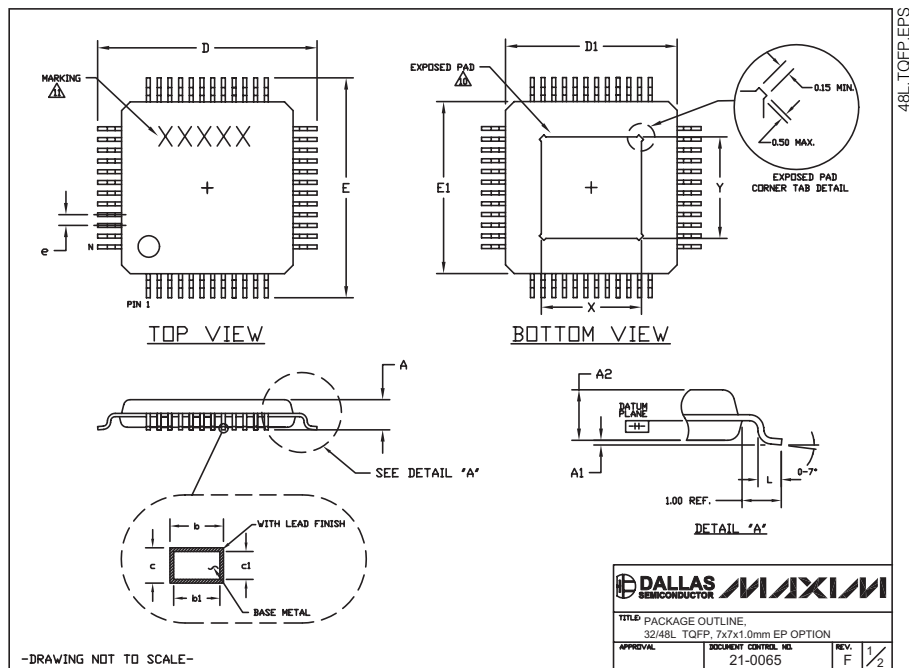
Typical Application Circuit



SSingle-Chip Global Positioning System Receiver Front-End

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



- NOTES:
1. ALL DIMENSIONS AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
 2. DATUM PLANE \square IS LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
 3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
 4. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15 MILLIMETERS.
 5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. ALL DIMENSIONS ARE IN MILLIMETERS.
 7. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS-026, VARIATIONS ABA-HD AND ABC-HD.
 8. LEADS SHALL BE COPLANAR WITHIN .004 INCH.
 9. EXPOSED DIE PAD SHALL BE COPLANAR WITH BOTTOM OF PACKAGE WITHIN 2 MILS (.05 MM).
 10. DIMENSIONS X & Y APPLY TO EXPOSED PAD (EP) VERSIONS ONLY. SEE INDIVIDUAL PRODUCT DATASHEET TO DETERMINE IF A PRODUCT USES EXPOSED PAD PACKAGE.
 11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
 12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.

SYMBOL	JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS					
	ABA-HD			ABC-HD		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.20			1.20
A1	0.05	0.10	0.15	0.05	0.10	0.15
A2	0.95	1.00	1.05	0.95	1.00	1.05
D	8.90	9.00	9.10	8.90	9.00	9.10
D1	6.90	7.00	7.10	6.90	7.00	7.10
E	8.90	9.00	9.10	8.90	9.00	9.10
E1	6.90	7.00	7.10	6.90	7.00	7.10
L	0.45	0.60	0.75	0.45	0.60	0.75
N	32			48		
e	0.80 BSC.			0.50 BSC.		
b	0.30	0.37	0.45	0.17	0.22	0.27
bl	0.30	0.35	0.40	0.17	0.20	0.23
c	0.09	---	0.20	0.09	---	0.20
cl	0.09	---	0.16	0.09	---	0.16
X	3.20	3.50	3.80	3.70	4.00	4.30
Y	3.20	3.50	3.80	3.70	4.00	4.30

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM			
TITLE: PACKAGE OUTLINE, 32/48L TOFP, 7x7x1.0mm EP OPTION			
APPROVAL:	DOCUMENT CONTROL NO.	REV.	
	21-0065	F	1/2

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