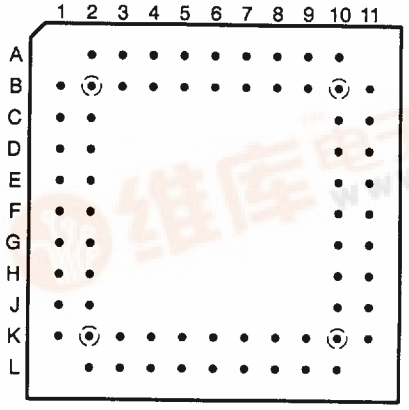
TMS320C25, TMS320E25
DIGITAL SIGNAL PROCESSORS

SPRS010C—MAY 1987—REVISED DECEMBER 1992

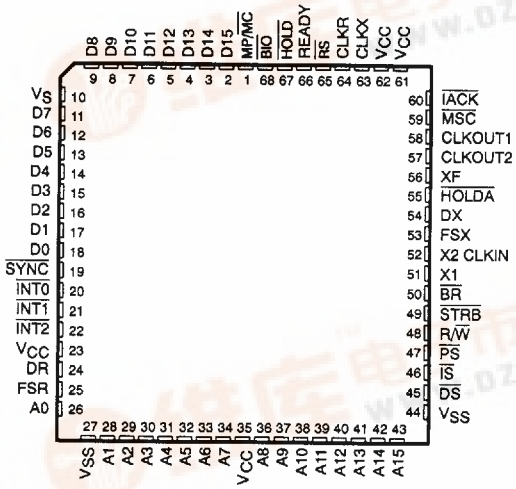
- 80-ns Instruction Cycle Time
- 544 Words of On-Chip Data RAM
- 4K Words of On-Chip Secure Program EPROM (TMS320E25)
- 4K Words of On-Chip Program ROM (TMS320C25)
- 128K Words of Data/Program Space
- 32-Bit ALU/Accumulator
- 16 × 16-Bit Multiplier With a 32-Bit Product
- Block Moves for Data/Program Management
- Repeat Instructions for Efficient Use of Program Space
- Serial Port for Direct Codec Interface
- Synchronization Input for Synchronous Multiprocessor Configurations
- Wait States for Communication to Slow Off-Chip Memories/Peripherals
- On-Chip Timer for Control Operations
- Single 5-V Supply
- Packaging: 68-Pin PGA, PLCC, and CER-QUAD
- 68-to-28 Pin Conversion Adapter Socket for EPROM Programming
- Commercial and Military Versions Available
- CMOS Technology:

TMS320C25	100-ns Cycle Time
TMS320E25	100-ns Cycle Time
TMS320C25-50	80-ns Cycle Time
TMS320C25-33	120-ns Cycle Time

68-PIN GB PACKAGE
(TOP VIEW)



68-PIN FN AND FZ PACKAGES
(TOP VIEW)



description

This data sheet provides complete design documentation for the second-generation devices of the TMS320 family. This facilitates the selection of the devices best suited for user applications by providing all specifications and special features for each TMS320 member. This data sheet is divided into four major sections: architecture, electrical specifications, timing diagrams, and mechanical data. In each of these sections, generic information is presented first, followed by specific device information. An index is provided for quick reference to specific information about a device.

PGA AND PLCC/CER-QUAD PIN ASSIGNMENTS

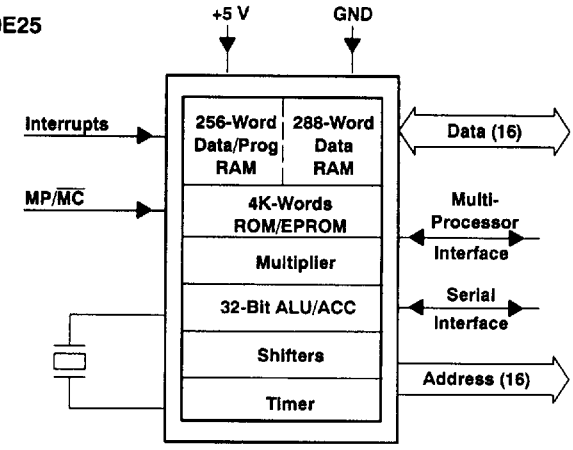
FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN
A0	K1/26	A12	K8/40	D2	E1/16	D14	A5/3	$\overline{INT2}$	H1/22	V_{CC}	H2/23
A1	K2/28	A13	L9/41	D3	D2/15	D15	B6/2	$\overline{IS}$	J11/46	V_{CC}	L6/35
A2	L3/29	A14	K9/42	D4	D1/14	DR	J1/24	MP/$\overline{MC}$	A6/1	V_{SS}	B1/10
A3	K3/30	A15	L10/43	D5	C2/13	$\overline{DS}$	K10/45	$\overline{MSC}$	C10/59	V_{SS}	K11/44
A4	L4/31	$\overline{BIO}$	B7/68	D6	C1/12	DX	E11/54	$\overline{PS}$	J10/47	V_{SS}	L2/27
A5	K4/32	$\overline{BR}$	G11/50	D7	B2/11	FSR	J2/25	READY	B8/66	XF	D11/56
A6	L5/33	CLKOUT1	C11/58	D8	A2/9	FSX	F10/53	$\overline{RS}$	A8/65	X1	G10/51
A7	K5/34	CLKOUT2	D10/57	D9	B3/8	$\overline{HOLD}$	A7/67	R/$\overline{W}$	H11/48	X2/CLKIN	F11/52
A8	K6/36	CLKR	B9/64	D10	A3/7	$\overline{HOLDA}$	E10/55	$\overline{STRB}$	H10/49		
A9	L7/37	CLKX	A9/63	D11	B4/6	$\overline{IACK}$	B11/60	$\overline{SYNC}$	F2/19		
A10	K7/38	D0	F1/18	D12	A4/5	$\overline{INT0}$	G1/20	V_{CC}	A10/61		
A11	L8/39	D1	E2/17	D13	B5/4	$\overline{INT1}$	G2/21	V_{CC}	B10/62		

SIGNALS	I/O/Z†	DEFINITION
V_{CC}	I	5-V supply pins
V_{SS}	I	Ground pins
X1	O	Output from internal oscillator for crystal
X2/CLKIN	I	Input to internal oscillator from crystal or external clock
CLKOUT1	O	Master clock output (crystal or CLKIN frequency/4)
CLKOUT2	O	A second clock output signal
D15-D0	I/O/Z	16-bit data bus D15 (MSB) through D0 (LSB). Multiplexed between program, data, and I/O spaces.
A15-A0	O/Z	16-bit address bus A15 (MSB) through A0 (LSB)
$\overline{PS}$, $\overline{DS}$, $\overline{IS}$	O/Z	Program, data, and I/O space select signals
R/$\overline{W}$	O/Z	Read/write signal
$\overline{STRB}$	O/Z	Strobe signal
$\overline{RS}$	I	Reset input
$\overline{INT2}$-$\overline{INT0}$	I	External user interrupt inputs
MP/$\overline{MC}$	I	Microprocessor/microcomputer mode select pin
$\overline{MSC}$	O	Microstate complete signal
$\overline{IACK}$	O	Interrupt acknowledge signal
READY	I	Data ready input. Asserted by external logic when using slower devices to indicate that the current bus transaction is complete.
$\overline{BR}$	O	Bus request signal. Asserted when the TMS320C2x requires access to an external global data memory space
XF	O	External flag output (latched software-programmable signal)
$\overline{HOLD}$	I	Hold input. When asserted, TMS320C2x goes into an idle mode and places the data, address, and control lines in the high impedance state.
$\overline{HOLDA}$	O	Hold acknowledge signal
$\overline{SYNC}$	I	Synchronization input
$\overline{BIO}$	I	Branch control input. Polled by BIOZ instruction.
DR	I	Serial data receive input
CLKR	I	Clock for receive input for serial port
FSR	I	Frame synchronization pulse for receive input
DX	O/Z	Serial data transmit output
CLKX	I	Clock for transmit output for serial port
FSX	I/O/Z	Frame synchronization pulse for transmit. Configuration as either an input or an output.

† I/O/Z denotes input/output/high-impedance state.

Key Features: TMS320C25, TMS320C25-50, TMS320E25

- **80-ns Instruction Cycle Time (TMS320C25-50)**
- **100-ns Instruction Cycle Time (TMS320C25)**
- **4K Words of On-Chip Secure Program EPROM (TMS320E25)**
- **4K Words of On-Chip Program ROM (TMS320C25)**
- **544 Words of On-Chip RAM**
- **128K Words of Total Program/Data Memory Space**
- **Wait States for Communications to Slower Off-Chip Memories**
- **Object-Code Compatible With the TMS32020**
- **Source-Code Compatible With TMS320C1x**
- **24 Additional Instructions to Support Adaptive Filtering, FFTs, and Extended-Precision Arithmetic**
- **Block Moves for Data/Program Management**
- **Single-Cycle Multiply/Accumulate Instructions**
- **Eight Auxiliary Registers With Dedicated Arithmetic Unit**
- **Bit-Reversed Indexed-Addressing Mode for Radix-2 FFTS**
- **Double-Buffered Serial Port**



- **On-Chip Clock Generator**
- **Single 5-V Supply**
- **Internal Security Mechanism (TMS320E25)**
- **68-to-28 Pin Conversion Adapter Socket**
- **CMOS Technology**
- **68-Pin Grid Array (PGA) Package (TMS320C25)**
- **68-Lead Plastic Leaded Chip Carrier (PLCC) Package (TMS320C25, TMS320C25-50)**
- **68-Lead CER-QUAD Package (TMS320E25)**

Table 1 provides an overview of the second-generation TMS320 processors with comparisons of memory, I/O, cycle timing, power, package type, technology, and military support. For specific availability, contact the nearest TI Field Sales Office.

Table 1. TMS320 Second-Generation Device Overview

DEVICE		MEMORY				I/O†			TIMER	CYCLE TIME (ns)	TYP POWER (mW)	PACKAGE TYPE		
		RAM	ON-CHIP ROM/EPROM	OFF-CHIP PROG	OFF-CHIP DATA	SER	PAR	DMA				PGA	PLCC	CER-QUAD
TMS320C25‡	(CMOS)	544	4K	64K	64K	YES	16 × 16	CON	YES	100	500	68	68	—
TMS320C25-50§	(CMOS)	544	4K	64K	64K	YES	16 × 16	CON	YES	80	500	—	68	—
TMS320E25§		544	4K	64K	64K	YES	16 × 16	CON	YES	100	500	—	—	68
TMS320C26	(CMOS)	1568	256	64K	64K	YES	16 × 16	CON	YES	100	500	—	68	—

† SER = serial; PAR = parallel; DMA = direct memory access; CON = concurrent DMA.
‡ Military version available; contact nearest TI Field Sales Office for availability.
§ Military version planned; contact nearest TI Field Sales Office for details.

architecture

The TMS320 family utilizes a modified Harvard architecture for speed and flexibility. In a strict Harvard architecture, program and data memory lie in two separate spaces, permitting a full overlap of instruction fetch and execution. The TMS320 family's modification of the Harvard architecture allows transfers between program and data spaces, thereby increasing the flexibility of the device. This modification permits coefficients stored in program memory to be read into the RAM, eliminating the need for a separate coefficient ROM. It also makes available immediate instructions and subroutines based on computed values.

Increased throughput on the TMS320C2x devices for many DSP applications is accomplished by means of single-cycle multiply/accumulate instructions with a data move option, up to eight auxiliary registers with a dedicated arithmetic unit, and faster I/O necessary for data-intensive signal processing.

The architectural design of the TMS320C2x emphasizes overall speed, communication, and flexibility in processor configuration. Control signals and instructions provide floating-point support, block-memory transfers, communication to slower off-chip devices, and multiprocessing implementations.

32-bit ALU/accumulator

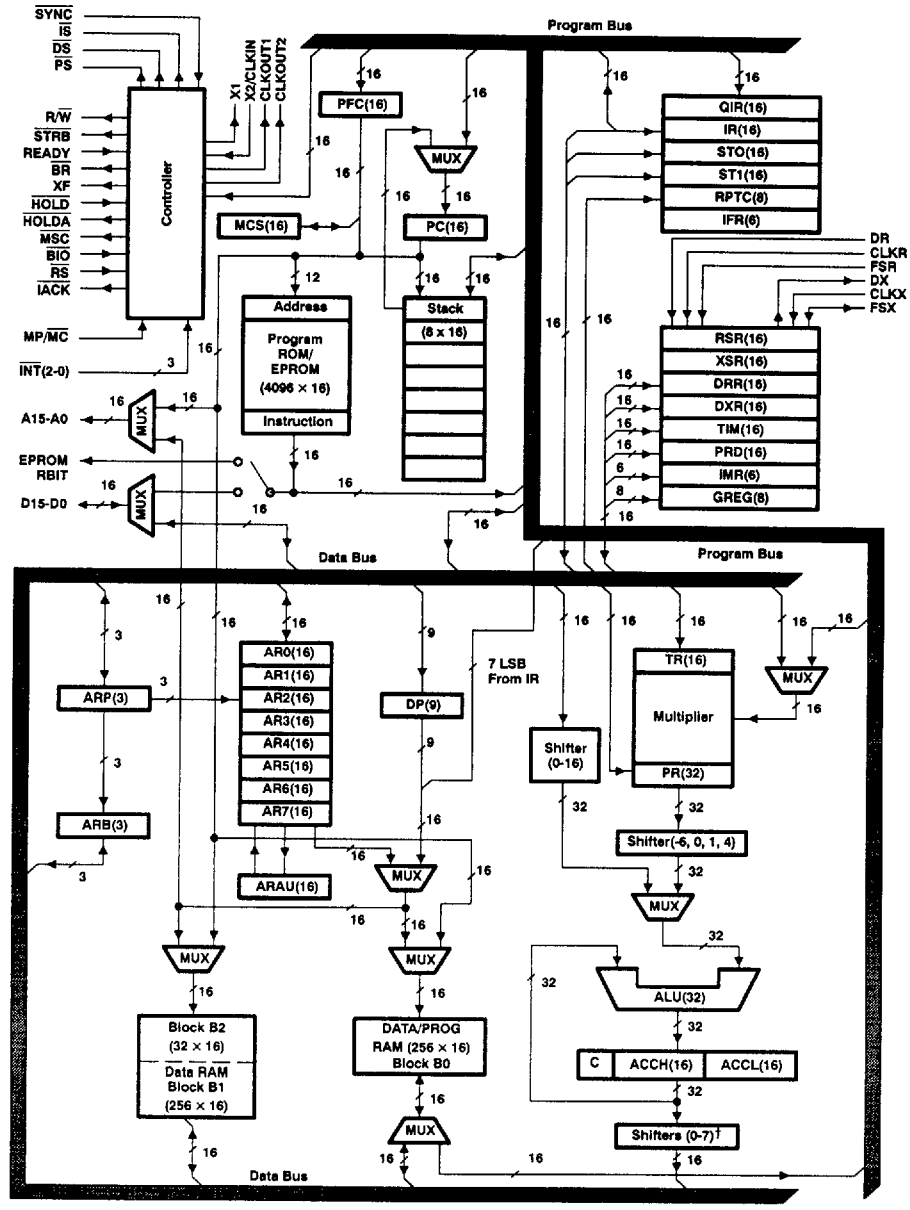
The 32-bit Arithmetic Logic Unit (ALU) and accumulator perform a wide range of arithmetic and logical instructions, the majority of which execute in a single clock cycle. The ALU executes a variety of branch instructions dependent on the status of the ALU or a single bit in a word. These instructions provide the following capabilities:

- Branch to an address specified by the accumulator
- Normalize fixed-point numbers contained in the accumulator
- Test a specified bit of a word in data memory

One input to the ALU is always provided from the accumulator, and the other input may be provided from the Product Register (PR) of the multiplier or the input scaling shifter which has fetched data from the RAM on the data bus. After the ALU has performed the arithmetic or logical operations, the result is stored in the accumulator.

The 32-bit accumulator is split into two 16-bit segments for storage in data memory. Additional shifters at the output of the accumulator perform shifts while the data is being transferred to the data bus for storage. The contents of the accumulator remain unchanged.

functional block diagram (TMS320C2x)



LEGEND

ACCH	= Accumulator high	IFR	= Interrupt flag register	PC	= Program counter
ACCL	= Accumulator low	IMR	= Interrupt mask register	PFC	= Prefetch counter
ALU	= Arithmetic logic unit	IR	= Instruction register	RPTC	= Repeat instruction counter
ARAU	= Auxiliary register arithmetic unit	MCS	= Microcall stack	GREG	= Global memory allocation register
ARB	= Auxiliary register pointer buffer	QIR	= Queue instruction register	RSR	= Serial port receive shift register
ARP	= Auxiliary register pointer	PR	= Product register	XSR	= Serial port transmit shift register
DP	= Data memory page pointer	PRD	= Period register for timer	AR0-AR7	= Auxiliary registers
DRR	= Serial port data receive register	TIM	= Timer	ST0, ST1	= Status registers
DXR	= Serial port data transmit register	TR	= Temporary register	C	= Carry bit

scaling shifter

The TMS320C2x scaling shifter has 16-bit input connected to the data bus and a 32-bit output connected to the ALU. The scaling shifter produces a left shift of 0 to 16 bits on the input data, as programmed in the instruction. The LSBs of the output are filled with zeroes, and the MSBs may be either filled with zeroes or sign-extended, depending upon the status programmed into the SXM (sign-extension mode) bit of status register ST1.

16 × 16-bit parallel multiplier

The 16 × 16-bit hardware multiplier is capable of computing a signed or unsigned 32-bit product in a single machine cycle. The multiplier has the following two associated registers.

- A 16-bit Temporary Register (TR) that holds one of the operands for the multiplier, and
- A 32-bit Product Register (PR) that holds the product.

Incorporated into the instruction set are single-cycle multiply/accumulate instructions that allow both operands to be processed simultaneously. The data for these operations may reside anywhere in internal or external memory, and can be transferred to the multiplier each cycle via the program and data buses.

Four product shift modes are available at the Product Register (PR) output that are useful when performing multiply/accumulate operations, fractional arithmetic, or justifying fractional products.

timer

The TMS320C2x provides a memory-mapped 16-bit timer for control operations. The on-chip timer (TIM) register is a down counter that is continuously clocked by CLKOUT1 on the TMS320C25. A timer interrupt (TINT) is generated every time the timer decrements to zero. The timer is reloaded with the value contained in the period (PRD) register within the next cycle after it reaches zero so that interrupts may be programmed to occur at regular intervals of PRD + 1 cycles of CLKOUT 1 on the TMS320C25.

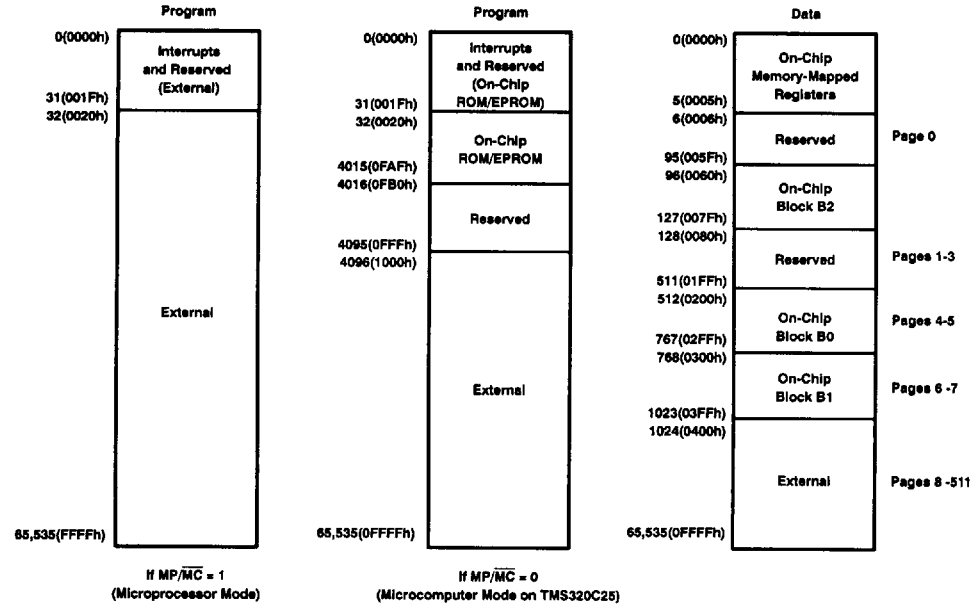
memory control

The TMS320C2x provides a total of 544 16-bit words of on-chip data RAM, divided into three separate blocks (B0, B1, and B2). Of the 544 words, 288 words (blocks B1 and B2) are always data memory, and 256 words (block B0) are programmable as either data or program memory. A data memory size of 544 words allows the TMS320C2x to handle a data array of 512 words (256 words if on-chip RAM is used for program memory), while still leaving 32 locations for intermediate storage. When using block B0 as program memory, instructions can be downloaded from external program memory into on-chip RAM and then executed.

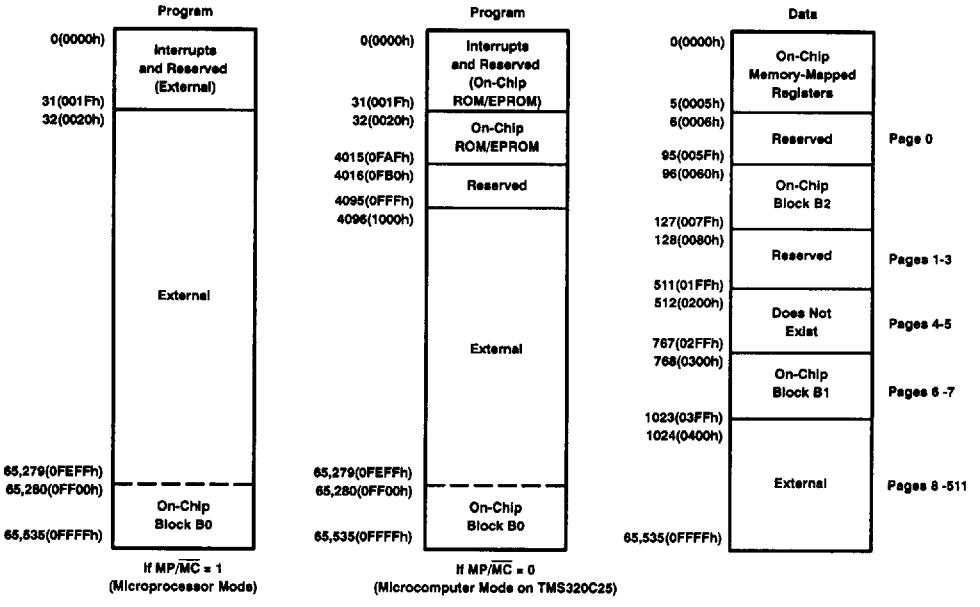
When using on-chip program RAM, ROM, EPROM, or high-speed external program memory, the TMS320C2x runs at full speed without wait states. However, the READY line can be used to interface the TMS320C2x to slower, less-expensive external memory. Downloading programs from slow off-chip memory to on-chip program RAM speeds processing while cutting system costs.

The TMS320C2x provides three separate address spaces for program memory, data memory, and I/O. The on-chip memory is mapped into either the 64K-word data memory or program memory space, depending upon the memory configuration (see Figure 1). The CNFD (configure block B0 as data memory) and CNFP (configure block B0 as program memory) instructions allow dynamic configuration of the memory maps through software. Regardless of the configuration, the user may still execute from external program memory.

The TMS320C2x has six registers that are mapped into the data memory space: a serial port data receive register, serial port data transmit register, timer register, period register, interrupt mask register, and global memory allocation register.



(a) Memory Maps After a CNFD Instruction



(b) Memory Maps After a CNFP Instruction

Figure 1. Memory Maps

Interrupts and subroutines

The TMS320C2x has three external maskable user interrupts $\overline{INT2}$-$\overline{INT0}$, available for external devices that interrupt the processor. Internal interrupts are generated by the serial port (RINT and XINT), by the timer (TINT), and by the software interrupt (TRAP) instruction. Interrupts are prioritized with reset ($\overline{RS}$) having the highest priority and the serial port transmit interrupt (XINT) having the lowest priority. All interrupt locations are on two-word boundaries so that branch instructions can be accommodated in those locations if desired.

A built-in mechanism protects multicycle instructions from interrupts. If an interrupt occurs during a multicycle instruction, the interrupt is not processed until the instruction is completed. This mechanism applies to instructions that are repeated and to instructions that become multicycle due to the READY signal.

external interface

The TMS320C2x supports a wide range of system interfacing requirements. Program, data, and I/O address spaces provide interface to memory and I/O, thus maximizing system throughput. I/O design is simplified by having I/O treated the same way as memory. I/O devices are mapped into the I/O address space using the processor's external address and data buses in the same manner as memory-mapped devices. Interface to memory and I/O devices of varying speeds is accomplished by using the READY line. When transactions are made with slower devices, the TMS320C2x processor waits until the other device completes its function and signals the processor via the READY line. Then, the TMS320C2x continues execution.

A full-duplex serial port provides communication with serial devices, such as codecs, serial A/D converters, and other serial systems. The interface signals are compatible with codecs and many other serial devices with a minimum of external hardware. The serial port may also be used for intercommunication between processors in multiprocessing applications.

The serial port has two memory-mapped registers: the data transmit register (DXR) and the data receive register (DRR). Both registers operate in either the byte mode or 16-bit word mode, and may be accessed in the same manner as any other data memory location. Each register has an external clock, a framing synchronization pulse, and associated shift registers. One method of multiprocessing may be implemented by programming one device to transmit while the others are in the receive mode. The serial port on the TMS320C25 is double-buffered and fully static.

multiprocessing

The flexibility of the TMS320C2x allows configurations to satisfy a wide range of system requirements and can be used as follows:

- A standalone processor
- A multiprocessor with devices in parallel
- A slave/host multiprocessor with global memory space
- A peripheral processor interfaced via processor-controlled signals to another device.

For multiprocessing applications, the TMS320C2x has the capability of allocating global data memory space and communicating with that space via the $\overline{BR}$ (bus request) and READY control signals. Global memory is data memory shared by more than one processor. Global data memory access must be arbitrated. The 8-bit memory-mapped GREG (global memory allocation register) specifies part of the TMS320C2x's data memory as global external memory. The contents of the register determine the size of the global memory space. If the current instruction addresses an operand within that space, $\overline{BR}$ is asserted to request control of the bus. The length of the memory cycle is controlled by the READY line.

The TMS320C2x supports DMA (direct memory access) to its external program/data memory using the $\overline{HOLD}$ and $\overline{HOLDA}$ signals. Another processor can take complete control of the TMS320C2x's external memory by asserting $\overline{HOLD}$ low. This causes the TMS320C2x to place its address data and control lines in a high-impedance state, and assert $\overline{HOLDA}$. On the TMS320C2x, program execution from on-chip ROM may proceed concurrently when the device is in the hold mode.

instruction set

The TMS320C2x microprocessor implements a comprehensive instruction set that supports both numeric-intensive signal processing operations as well as general-purpose applications, such as multiprocessing and high-speed control.

For maximum throughput, the next instruction is prefetched while the current one is being executed. Since the same data lines are used to communicate to external data/program or I/O space, the number of cycles may vary depending upon whether the next data operand fetch is from internal or external memory. Highest throughput is achieved by maintaining data memory on-chip and using either internal or fast external program memory.

addressing modes

The TMS320C2x instruction set provides three memory addressing modes: direct, indirect, and immediate addressing.

Both direct and indirect addressing can be used to access data memory. In direct addressing, seven bits of the instruction word are concatenated with the nine bits of the data memory page pointer to form the 16-bit data memory address. Indirect addressing accesses data memory through the auxiliary registers. In immediate addressing, the data is based on a portion of the instruction word(s).

In direct memory addressing, the instruction word contains the lower seven bits of the data memory address. This field is concatenated with the nine bits of the data memory page pointer to form the full 16-bit address. Thus, memory is paged in the direct addressing mode with a total of 512 pages, each page containing 128 words.

Eight auxiliary registers (AR0-AR7) provide flexible and powerful indirect addressing on the TMS320C25. To select a specific auxiliary register, the Auxiliary Register Pointer (ARP) is loaded with a value from 0 to 7 for AR0 through AR7, respectively.

There are seven types of indirect addressing: auto-increment or auto-decrement, post-indexing by either adding or subtracting the contents of AR0, single indirect addressing with no increment or decrement, and bit-reversal addressing (used in FFTs on the TMS320C25 only) with increment or decrement. All operations are performed on the current auxiliary register in the same cycle as the original instruction, following which the current auxiliary register and ARP may be modified.

repeat feature

A repeat feature, used with instructions such as multiply/accumulates, block moves, I/O transfers, and table read/writes, allows a single instruction to be performed up to 256 times. The repeat counter (RPTC) is loaded with either a data memory value (RPT instruction) or an immediate value (RPTK instruction). The value of this operand is one less than the number of times that the next instruction is executed. Those instructions that are normally multicycle are pipelined when using the repeat feature, and effectively become single-cycle instructions.

instruction set summary

Table 2 lists the symbols and abbreviations used in Table 3, the TMS320C25 instruction set summary. Table 3 consists primarily of single-cycle, single-word instructions. Infrequently used branch, I/O, and CALL instructions are multicycle. The instruction set summary is arranged according to function and alphabetized within each functional grouping. The symbol (†) indicates those instructions that are not included in the TMS320C1x instruction set.

Table 2. Instruction Symbols

SYMBOL	DEFINITION
B	4-bit field specifying a bit code
CM	2-bit field specifying compare mode
D	Data memory address field
FO	Format status bit
M	Addressing mode bit
K	Immediate operand field
PA	Port address (PA0–PA15 are predefined assembler symbols equal to 0–15, respectively.)
PM	2-bit field specifying P register output shift code
AR	3-bit operand field specifying auxiliary register
S	4-bit left-shift code
X	3-bit accumulator left-shift field

Table 3. TMS320C25 Instruction Set Summary

ACCUMULATOR MEMORY REFERENCE INSTRUCTIONS																	
MNEMONIC	DESCRIPTION	NO. WORDS	INSTRUCTION BIT CODE														
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ABS	Absolute value of accumulator	1	1	1	0	0	1	1	1	0	0	0	0	1	1	0	1	1
ADD	Add to accumulator with shift	1	0	0	0	0	←	S	→		M	←		D		→		
ADDC	Add to accumulator with carry	1	0	1	0	0	0	0	1	1	M	←		D		→		
ADDH	Add to high accumulator	1	0	1	0	0	1	0	0	0	M	←		D		→		
ADDK	Add to accumulator short immediate	1	1	1	0	0	1	1	0	0	←			K		→		
ADDS	Add to low accumulator with sign extension suppressed	1	0	1	0	0	1	0	0	1	M	←		D		→		
ADDT	Add to accumulator with shift specified by T register	1	0	1	0	0	1	0	1	0	M	←		D		→		
ADLK†	Add to accumulator long immediate with shift	2	1	1	0	1	←	S	→		0	0	0	0	0	0	1	0
AND	AND with accumulator	1	0	1	0	0	1	1	1	0	M	←		D		→		
ANDK†	AND immediate with accumulator with shift	2	1	1	0	1	←	S	→		0	0	0	0	0	1	0	0
CMPL†	Complement accumulator	1	1	1	0	0	1	1	1	0	0	0	1	0	0	1	1	1
LAC	Load accumulator with shift	1	0	0	1	0	←	S	→		M	←		D		→		
LACK	Load accumulator immediate short	1	1	1	0	0	1	0	1	0	←			K		→		
LACT†	Load accumulator with shift specified by T register	1	0	1	0	0	0	0	1	0	M	←		D		→		
LALK†	Load accumulator long immediate with shift	2	1	1	0	1	←	S	→		0	0	0	0	0	0	0	1
NEG†	Negate accumulator	1	1	1	0	0	1	1	1	0	0	0	1	0	0	0	1	1
NORM†	Normalize contents of accumulator	1	1	1	0	0	1	1	1	0	1	X	X	X	0	0	1	0
OR	OR with accumulator	1	0	1	0	0	1	1	0	1	M	←		D		→		
ORK†	OR immediate with accumulator with shift	2	1	1	0	1	←	S	→		0	0	0	0	0	1	0	1
ROL	Rotate accumulator left	1	1	1	0	0	1	1	1	0	0	0	1	1	0	1	0	0
ROR	Rotate accumulator right	1	1	1	0	0	1	1	1	0	0	0	1	1	0	1	0	1
SACH	Store high accumulator with shift	1	0	1	1	0	1	←	X	→	M	←		D		→		
SACL	Store low-order accumulator with shift	1	0	1	1	0	0	←	X	→	M	←		D		→		
SBLK†	Subtract from accumulator long immediate with shift	2	1	1	0	1	←	S	→		0	0	0	0	0	0	1	1
SFL†	Shift accumulator left	1	1	1	0	0	1	1	1	0	0	0	0	1	1	0	0	0
SFR†	Shift accumulator right	1	1	1	0	0	1	1	1	0	0	0	0	1	1	0	0	1
SUB	Subtract from accumulator with shift	1	0	0	0	1	←	S	→		M	←		D		→		
SUBB	Subtract from accumulator with borrow	1	0	1	0	0	1	1	1	1	M	←		D		→		
SUBC	Conditional subtract	1	0	1	0	0	0	1	1	1	M	←		D		→		
SUBH	Subtract from high accumulator	1	0	1	0	0	0	1	0	0	M	←		D		→		
SUBK	Subtract from accumulator short immediate	1	1	1	0	0	1	1	0	1	←			K		→		
SUBS	Subtract from low accumulator with sign extension suppressed	1	0	1	0	0	0	1	0	1	M	←		D		→		

† These instructions are not included in the TMS320C1x instruction set.

Table 3. TMS320C25 Instruction Set Summary (continued)

ACCUMULATOR MEMORY REFERENCE INSTRUCTIONS																		
MNEMONIC	DESCRIPTION	NO. WORDS	INSTRUCTION BIT CODE															
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUBT†	Subtract from accumulator with shift specified by T register	1	0	1	0	0	0	1	1	0	M	←			D			→
XOR	Exclusive-OR with accumulator	1	0	1	0	0	1	1	0	0	M	←			D			→
XORK†	Exclusive-OR immediate with accumulator with shift	2	1	1	0	1	←	S	→		0	0	0	0	0	1	1	0
ZAC	Zero accumulator	1	1	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0
ZALH	Zero low accumulator and load high accumulator	1	0	1	0	0	0	0	0	0	M	←			D			→
ZALR	Zero low accumulator and load high accumulator with rounding	1	0	1	1	1	1	0	1	1	M	←			D			→
ZALS	Zero accumulator and load low accumulator with sign extension suppressed	1	0	1	0	0	0	0	0	1	M	←			D			→

AUXILIARY REGISTERS AND DATA PAGE POINTER INSTRUCTIONS																		
MNEMONIC	DESCRIPTION	NO. WORDS	INSTRUCTION BIT CODE															
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADRK	Add to auxiliary register short immediate	1	0	1	1	1	1	1	1	0	←				K			→
CMPR†	Compare auxiliary register with auxiliary register AR0	1	1	1	0	0	1	1	1	0	0	1	0	1	0	0	←	CM →
LAR	Load auxiliary register	1	0	0	1	1	0	←	R	→	M	←			D			→
LARK	Load auxiliary register short immediate	1	1	1	0	0	0	←	R	→	←				K			→
LARP	Load auxiliary register pointer	1	0	1	0	1	0	1	0	1	1	0	0	0	1	←	R	→
LDP	Load data memory page pointer	1	0	1	0	1	0	0	1	0	M	←			D			→
LDPK	Load data memory page pointer immediate	1	1	1	0	0	1	0	0	←					DP			→
LRLK†	Load auxiliary register long immediate	2	1	1	0	1	0	←	R	→	0	0	0	0	0	0	0	0
MAR	Modify auxiliary register	1	0	1	0	1	0	1	0	1	M	←			D			→
SAR	Store auxiliary register	1	0	1	1	1	0	←	R	→	M	←			D			→
SBRK	Subtract from auxiliary register short immediate	1	0	1	1	1	1	1	1	1	←				K			→

† These instructions are not included in the TMS320C1x instruction set.

Table 3. TMS320C25 Instruction Set Summary (continued)

T REGISTER, P REGISTER, AND MULTIPLY INSTRUCTIONS																		
MNEMONIC	**DESCRIPTION**	**NO. WORDS**	**INSTRUCTION BIT CODE**															
			15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
APAC	Add P register to accumulator	1	1	1	0	0	1	1	1	0	0	0	0	1	0	1	0	1
LPH†	Load high P register	1	0	1	0	1	0	0	1	1	M	◄			D			►
LT	Load T register	1	0	0	1	1	1	1	0	0	M	◄			D			►
LTA	Load T register and accumulate previous product	1	0	0	1	1	1	1	0	1	M	◄			D			►
LTD	Load T register, accumulate previous product, and move data	1	0	0	1	1	1	1	1	1	M	◄			D			►
LTP†	Load T register and store P register in accumulator	1	0	0	1	1	1	1	1	0	M	◄			D			►
LTS†	Load T register and subtract previous product	1	0	1	0	1	1	0	1	1	M	◄			D			►
MAC†	Multiply and accumulate	2	0	1	0	1	1	1	0	1	M	◄			D			►
MACD†	Multiply and accumulate with data move	2	0	1	0	1	1	1	0	0	M	◄			D			►
MPY	Multiply (with T register, store product in P register)	1	0	0	1	1	1	0	0	0	M	◄			D			►
MPYA	Multiply and accumulate previous product	1	0	0	1	1	1	0	1	0	M	◄			D			►
MPYK	Multiply immediate	1	1	0	1	◄					K							►
MPYS	Multiply and subtract previous product	1	0	0	1	1	1	0	1	1	M	◄			D			►
MPYU	Multiply unsigned	1	1	1	0	0	1	1	1	1	M	◄			D			►
PAC	Load accumulator with P register	1	1	1	0	0	1	1	1	0	0	0	0	1	0	1	0	0
SPAC	Subtract P register from accumulator	1	1	1	0	0	1	1	1	0	0	0	0	1	0	1	1	0
SPH	Store high P register	1	0	1	1	1	1	1	0	1	M	◄			D			►
SPL	Store low P register	1	0	1	1	1	1	1	0	0	M	◄			D			►
SPM†	Set P register output shift mode	1	1	1	0	0	1	1	1	0	0	0	0	0	1	0	◄	PM►
SQRA†	Square and accumulate	1	0	0	1	1	1	0	0	1	M	◄			D			►
SQRS†	Square and subtract previous product	1	0	1	0	1	1	0	1	0	M	◄			D			►

† These instructions are not included in the TMS320C1x instruction set

Table 3. TMS320C25 Instruction Set Summary (continued)

BRANCH/CALL INSTRUCTIONS																		
MNEMONIC	DESCRIPTION	NO. WORDS	INSTRUCTION BIT CODE															
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
B	Branch unconditionally	2	1	1	1	1	1	1	1	1	1	←			D			→
BACC†	Branch to address specified by accumulator	1	1	1	0	0	1	1	1	0	0	0	1	0	0	1	0	1
BANZ	Branch on auxiliary register not zero	2	1	1	1	1	1	0	1	1	1	←			D			→
BBNZ†	Branch if TC bit ≠ 0	2	1	1	1	1	1	0	0	1	1	←			D			→
BBZ†	Branch if TC bit = 0	2	1	1	1	1	1	0	0	0	1	←			D			→
BC	Branch on carry	2	0	1	0	1	1	1	1	0	1	←			D			→
BGEZ	Branch if accumulator ≥ 0	2	1	1	1	1	0	1	0	0	1	←			D			→
BGZ	Branch if accumulator > 0	2	1	1	1	1	0	0	0	1	1	←			D			→
BIOZ	Branch on I/O status = 0	2	1	1	1	1	1	0	1	0	1	←			D			→
BLEZ	Branch if accumulator ≤ 0	2	1	1	1	1	0	0	1	0	1	←			D			→
BLZ	Branch if accumulator < 0	2	1	1	1	1	0	0	1	1	1	←			D			→
BNC	Branch on no carry	2	0	1	0	1	1	1	1	1	1	←			D			→
BNV†	Branch if no overflow	2	1	1	1	1	0	1	1	1	1	←			D			→
BNZ	Branch if accumulator ≠ 0	2	1	1	1	1	0	1	0	1	1	←			D			→
BV	Branch on overflow	2	1	1	1	1	0	0	0	0	1	←			D			→
BZ	Branch if accumulator = 0	2	1	1	1	1	0	1	1	0	1	←			D			→
CALA	Call subroutine indirect	1	1	1	0	0	1	1	1	0	0	0	1	0	0	1	0	0
CALL	Call subroutine	2	1	1	1	1	1	1	1	0	1	←			D			→
RET	Return from subroutine	1	1	1	0	0	1	1	1	0	0	0	1	0	0	1	1	0

I/O AND DATA MEMORY OPERATIONS																		
MNEMONIC	DESCRIPTION	NO. WORDS	INSTRUCTION BIT CODE															
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BLKD†	Block move from data memory to data memory	2	1	1	1	0	1	1	0	1	M	←			D			→
BLKP†	Block move from program memory to data memory	2	1	1	1	1	1	1	0	0	M	←			D			→
DMOV	Data move in data memory	1	0	1	0	1	0	1	1	0	M	←			D			→
FORT†	Format serial port registers	1	1	1	0	0	1	1	1	0	0	0	0	0	1	1	1	FO
IN	Input data from port	1	1	0	0	0	←	PA	→	M		←			D			→
OUT	Output data to port	1	1	1	1	0	←	PA	→	M		←			D			→
RFSM	Reset serial port frame synchronization mode	1	1	1	0	0	1	1	1	0	0	0	1	1	0	1	1	0
RTXM†	Reset serial port transmit mode	1	1	1	0	0	1	1	1	0	0	0	1	0	0	0	0	0
RXF†	Reset external flag	1	1	1	0	0	1	1	1	0	0	0	0	0	1	1	0	0
SFSM	Set serial port frame synchronization mode	1	1	1	0	0	1	1	1	0	0	0	1	1	0	1	1	1
STXM†	Set serial port transmit mode	1	1	1	0	0	1	1	1	0	0	0	1	0	0	0	0	1
SXF†	Set external flag	1	1	1	0	0	1	1	1	0	0	0	0	0	1	1	0	1
TBLR	Table read	1	0	1	0	1	1	0	0	0	M	←			D			→
TBLW	Table write	1	0	1	0	1	1	0	0	1	M	←			D			→

† These instructions are not included in the TMS320C1x instruction set.

Table 3. TMS320C25 Instruction Set Summary (concluded)

CONTROL INSTRUCTIONS																		
MNEMONIC	DESCRIPTION	NO. WORDS	INSTRUCTION BIT CODE															
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIT†	Test bit	1	1	0	0	1	←	B	→		M	←			D			→
BITT†	Test bit specified by T register	1	0	1	0	1	0	1	1	1	M	←			D			→
CNFD†	Configure block as data memory	1	1	1	0	0	1	1	1	0	0	0	0	0	0	1	0	0
CNFP†	Configure block as program memory	1	1	1	0	0	1	1	1	0	0	0	0	0	0	1	0	1
DINT	Disable interrupt	1	1	1	0	0	1	1	1	0	0	0	0	0	0	0	0	1
EINT	Enable interrupt	1	1	1	0	0	1	1	1	0	0	0	0	0	0	0	0	0
IDLE†	Idle until interrupt	1	1	1	0	0	1	1	1	0	0	0	0	1	1	1	1	1
LST	Load status register STO	1	0	1	0	1	0	0	0	0	M	←			D			→
LST1†	Load status register ST1	1	0	1	0	1	0	0	0	1	M	←			D			→
NOP	No operation	1	0	1	0	1	0	1	0	1	0	0	0	0	0	0	0	0
POP	Pop top of stack to low accumulator	1	1	1	0	0	1	1	1	0	0	0	0	1	1	1	0	1
POPD†	Pop top of stack to data memory	1	0	1	1	1	1	0	1	0	M	←			D			→
PSHD†	Push data memory value onto stack	1	0	1	0	1	0	1	0	0	M	←			D			→
PUSH	Push low accumulator onto stack	1	1	1	0	0	1	1	1	0	0	0	0	1	1	1	0	0
RC	Reset carry bit	1	1	1	0	0	1	1	1	0	0	0	1	1	0	0	0	0
RHM	Reset hold mode	1	1	1	0	0	1	1	1	0	0	0	1	1	1	0	0	0
ROVM	Reset overflow mode	1	1	1	0	0	1	1	1	0	0	0	0	0	0	0	1	0
RPT†	Repeat instruction as specified by data memory value	1	0	1	0	0	1	0	1	1	M	←			D			→
RPTK†	Repeat instruction as specified by immediate value	1	1	1	0	0	1	0	1	1	←				K			→
RSXM†	Reset sign-extension mode	1	1	1	0	0	1	1	1	0	0	0	0	0	0	1	1	0
RTC	Reset test/control flag	1	1	1	0	0	1	1	1	0	0	0	1	1	0	0	1	0
SC	Set carry bit	1	1	1	0	0	1	1	1	0	0	0	1	1	0	0	0	1
SHM	Set hold mode	1	1	1	0	0	1	1	1	0	0	0	1	1	1	0	0	1
SOVM	Set overflow mode	1	1	1	0	0	1	1	1	0	0	0	0	0	0	0	1	1
SST	Store status register ST0	1	0	1	1	1	1	0	0	0	M	←			D			→
SST1†	Store status register ST1	1	0	1	1	1	1	0	0	1	M	←			D			→
SSXM†	Set sign-extension mode	1	1	1	0	0	1	1	1	0	0	0	0	0	0	1	1	1
STC	Set test/control flag	1	1	1	0	0	1	1	1	0	0	0	1	1	0	0	1	1
TRAP†	Software interrupt	1	1	1	0	0	1	1	1	0	0	0	0	1	1	1	1	0

† These instructions are not included in the TMS320C1x instruction set.

documentation support

Extensive documentation supports the second-generation TMS320 devices from product announcement through applications development. The types of documentation include data sheets with design specifications, complete user's guides, and 750 pages of application reports published in the book, *Digital Signal Processing Applications with the TMS320 Family* (SPRA012A). An application report, *Hardware Interfacing to the TMS320C25* (SPRA014A), is available for that device.

A series of DSP textbooks is being published by Prentice-Hall and John Wiley & Sons to support digital signal processing research and education. The TMS320 newsletter, *Details on Signal Processing*, is published quarterly and distributed to update TMS320 customers on product information. The TMS320 DSP bulletin board service provides access to large amounts of information pertaining to the TMS320 family.

Refer to the *TMS320 Family Development Support Reference Guide* (SPRU011B) for further information about TMS320 documentation. To receive copies of second-generation TMS320 literature, call the Customer Response Center at 1-800-232-3200.

specification overview

The electrical specifications for the TMS320C25, TMS320E25, and TMS320C25-50 are given in the following pages. Note that the electrical specifications for the TMS320E25 are identical to those for the TMS320C25, with the addition of EPROM-related specifications.

absolute maximum ratings over specified temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}‡ ..... – 0.3 V to 7 V
Input voltage range: TMS320E25 pins 24 and 25 ..... – 0.3 V to 15 V
All other inputs ..... – 0.3 V to 7 V
Output voltage range ..... – 0.3 V to 7 V
Continuous power dissipation ..... 1.5 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 55°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ All voltage values are with respect to V_{SS}.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{SS}	Supply voltage			0		V
V_{IH}	High-level input voltage	All inputs except CLKIN/CLKX/CLKR/$\overline{INT}$ (0-2)	2.35		V_{CC} + 0.3	V
		$\overline{INT}$ (0-2)	2.5		V_{CC} + 0.3	V
		CLKIN/CLKX/CLKR	3.5		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage	All inputs except MP/$\overline{MC}$	– 0.3		0.8	V
		MP/$\overline{MC}$	– 0.3		0.8	V
I_{OH}	High-level output current				300	μA
I_{OL}	Low-level output current				2	mA
T_A	Operating free-air temperature	TMS320C25, TMS320E25	0		70	°C
		TMS320C25GBA	– 40		85	°C

electrical characteristics over specified free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	TMS320C25 TMS320C25-50 TMS320E25			TMS320C25-33			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, I_{OH} = MAX	2.4	3		2.4	3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, I_{OL} = MAX		0.3	0.6		0.3	0.6	V
I_Z	Three-state current		V_{CC} = MAX	–20		20	–20		20	μA
I_I	Input current		V_I = V_{SS} to V_{CC}	–10		10	–10		10	μA
V_{IL}	Low-levelinputvoltage	Normal	T_A = 0°C, V_{CC} = MAX, f_x = MAX		110	185		95	185	mA
		Idle/$\overline{HOLD}$			50	100		40	100	
C_I	Input capacitance				15			15		pF
C_O	Output capacitance				15			15		pF

§ All typical values are at V_{CC} = 5 V, T_A = 25°.

Caution. This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields. These circuits have been qualified to protect this device against electrostatic discharges (ESD) of up to 2 kV according to MIL-STD-883C, Method 3015; however, it is advised that precautions to be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits. During storage or handling, the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground. Specific guidelines for handling devices of this type are contained in the publication "Guidelines for Handling Electrostatic-Discharge Sensitive (ESDS) Devices and Assemblies" available from Texas Instruments

CLOCK CHARACTERISTICS AND TIMING

The TMS32025 can use either its internal oscillator or an external frequency source for a clock.

internal clock option

The internal oscillator is enabled by connecting a crystal across X1 and X2/CLKIN (see Figure 2). The frequency of CLKOUT1 is one-fourth the crystal fundamental frequency. The crystal should be either fundamental or overtone mode, and parallel resonant, with an effective series resistance of 30 Ω, a power dissipation of 1 mW, and be specified at a load capacitance of 20 pF. Note that overtone crystals require an additional tuned LC circuit.

PARAMETER		TEST CONDITIONS	TMS320C25 TMS320E25			TMS320C25-33			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f_X	Input clock frequency	T_A = 0°C to 70°C	6.7		40.96	6.7		33.0	MHz
f_{XS}	Serial port frequency	T_A = 0°C to 70°C	0†		5.12	0†		4.125	MHz
C1, C2		T_A = 0°C to 70°C		10			10		pF

† The serial port was tested at a minimum frequency of 1.25 MHz. However, the serial port was fully static but will properly function down to f_{SX} = 0 Hz.

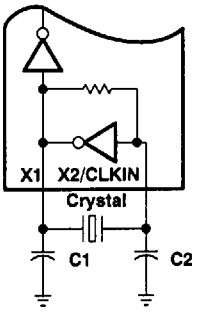


Figure 2. Internal Clock Option

external clock option

An external frequency source can be used by injecting the frequency directly into X2/CLKIN with X1 left unconnected. The external frequency injected must conform to the specifications listed in the following table.

switching characteristics over recommended operating conditions (see Note 1)

PARAMETER		TMS320C25 TMS320E25			TMS320C25-33			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
$t_{c(C)}$	CLKOUT1/CLKOUT2 cycle time	97.7		597	121.2		597	ns
$t_{c(CIH-C)}$	CLKIN high to CLKOUT1/CLKOUT2/$\overline{STRB}$ high/low	5		30	5		30	ns
$t_{f(C)}$	CLKOUT1/CLKOUT2/$\overline{STRB}$ fall time			5			5	ns
$t_{r(C)}$	CLKOUT1/CLKOUT2/$\overline{STRB}$ rise time			5			5	ns
$t_{w(CL)}$	CLKOUT1/CLKOUT2 low pulse duration	2Q – 8	2Q	2Q + 8	2Q – 8	2Q	2Q + 8	ns
$t_{w(CH)}$	CLKOUT1/CLKOUT2 high pulse duration	2Q – 8	2Q	2Q + 8	2Q – 8	2Q	2Q + 8	ns
$t_{d(C1-C2)}$	CLKOUT1 high to CLKOUT2 low; CLKOUT2 high to CLKOUT1 high; etc.	Q – 5	Q	Q + 5	Q – 5	Q	Q + 5	ns

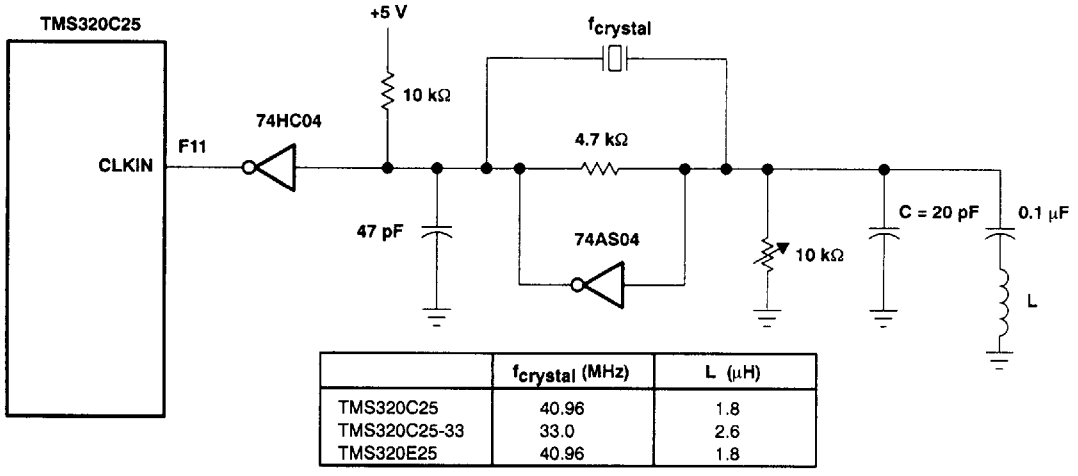
NOTE 1: $Q = 1/4t_{c(C)}$.

timing requirements over recommended operating conditions (see Note 1)

		TMS320C25 TMS320E25			TMS320C25-33			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$t_{c(CI)}$	CLKIN cycle time	24.4		150	30.3		150	ns
$t_{f(CI)}$	CLKIN fall time			5†			5†	ns
$t_{r(CI)}$	CLKIN rise time			5†			5†	ns
$t_{w(CIL)}$	CLKIN low pulse duration, $t_{c(CI)}$ = 50 ns (see Note 2)	20			20			ns
$t_{w(CIH)}$	CLKIN high pulse duration, $t_{c(CI)}$ = 50 ns (see Note 2)	20			20			ns
$t_{su(S)}$	$\overline{SYNC}$ setup time before CLKIN low	5		Q – 8	5		Q – 8	ns
$t_{h(S)}$	$\overline{SYNC}$ hold time from CLKIN low	8			8			ns

† Value derived from characterization data and not tested.

NOTES: 1. $Q = 1/4t_{c(C)}$.
2. CLKIN duty cycle $[t_{r(CI)} + t_{w(CIH)}]/t_{c(CI)}$ must be within 40-60%.



	$f_{crystal}$ (MHz)	L (µH)
TMS320C25	40.96	1.8
TMS320C25-33	33.0	2.6
TMS320E25	40.96	1.8

Figure 3. External Clock Option

Shown above is a crystal oscillator circuit suitable for providing the input clock signal to the TMS320C25, TMS320E25, and TMS320C25-33. Please refer to "Hardware Interfacing to the TMS320C2x", in *Digital Signal Processing Applications with the TMS320 Family, Volume 2* (document number SPRA016) for details on circuit operation.

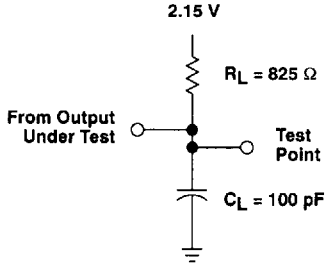
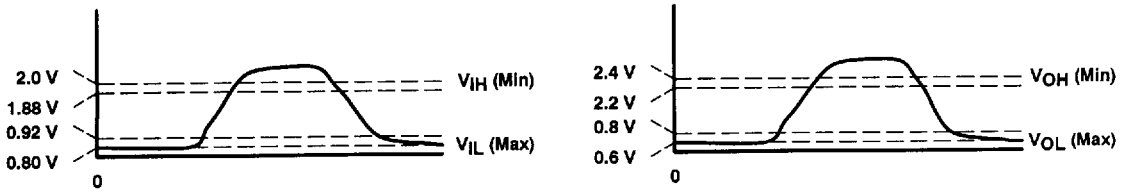


Figure 4. Test Load Circuit



(a) Input (b) Output

Figure 5. Voltage Reference Levels

MEMORY AND PERIPHERAL INTERFACE TIMING

switching characteristics over recommended operating conditions (see Note 1)

	PARAMETER	MIN	TYP	MAX	UNIT
$t_{d(C1-S)}$	$\overline{STRB}$ from CLKOUT1 (if $\overline{STRB}$ is present)	Q – 6	Q	Q + 6	ns
$t_{d(C2-S)}$	CLKOUT2 to $\overline{STRB}$ (if $\overline{STRB}$ is present)	– 6	0	6	ns
$t_{su(A)}$	Address setup time before $\overline{STRB}$ low (see Note 3)	Q – 12			ns
$t_{h(A)}$	Address hold time after $\overline{STRB}$ high (see Note 3)	Q – 8			ns
$t_{w(SL)}$	$\overline{STRB}$ low pulse duration (no wait states, see Note 4)	2Q – 5		2Q + 5	ns
$t_{w(SH)}$	$\overline{STRB}$ high pulse duration (between consecutive cycles, see Note 4)	2Q – 5		2Q + 5	ns
$t_{su(D)W}$	Data write setup time before $\overline{STRB}$ high (no wait states)	2Q – 20			ns
$t_{h(D)W}$	Data write hold time from $\overline{STRB}$ high	Q – 10	Q		ns
$t_{en(D)}$	Data bus starts being driven after $\overline{STRB}$ low (write cycle)	0†			ns
$t_{dis(D)}$	Data bus three-state after $\overline{STRB}$ high (write cycle)		Q	Q + 15†	ns
$t_{d(MSC)}$	$\overline{MSC}$ valid from CLKOUT1	– 12	0	12	ns

† Value derived from characterization data and not tested.

NOTES: 1. $Q = 1/4t_{c(C)}$.
3. A15-A0, $\overline{PS}$, $\overline{DS}$, $\overline{IS}$, R/$\overline{W}$, and $\overline{BR}$ timings are all included in timings referenced as "address"
4. Delays between CLKOUT1/CLKOUT2 edges and $\overline{STRB}$ edges track each other, resulting in $t_{w(SL)}$ and $t_{w(SH)}$ being 2Q with no wait states.

timing requirements over recommended operating conditions (see Note 1)

		MIN	NOM	MAX	UNIT
$t_{a(A)}$	Read data access time from address time (read cycle, see Notes 3 and 5)			3Q – 35	ns
$t_{su(D)R}$	Data read setup time before $\overline{STRB}$ high	23			ns
$t_{h(D)R}$	Data read hold time from $\overline{STRB}$ high	0			ns
$t_{d(SL-R)}$	READY valid after $\overline{STRB}$ low (no wait states)			Q – 20	ns
$t_{d(C2H-R)}$	READY valid after CLKOUT2 high			Q – 20	ns
$t_{h(SL-R)}$	READY hold time after $\overline{STRB}$ low (no wait states)	Q + 3			ns
$t_{h(C2H-R)}$	READY hold after CLKOUT2 high	Q + 3			ns
$t_{d(M-R)}$	READY valid after $\overline{MSC}$ valid			2Q – 25	ns
$t_{h(M-R)}$	READY hold time after $\overline{MSC}$ valid	0			ns

NOTES: 1. $Q = 1/4t_{c(C)}$.
3. A15-A0, $\overline{PS}$, $\overline{DS}$, $\overline{IS}$, R/$\overline{W}$, and $\overline{BR}$ timings are all included in timings referenced as "address".
5. Read data access time is defines as $t_{a(A)} = t_{su(A)} + t_{w(SL)} - t_{su(D)R}$.

$\overline{RS}$, $\overline{INT}$, $\overline{BIO}$, AND XF TIMING

switching characteristics over recommended operating conditions (see Notes 1 and 6)

	PARAMETER	MIN	TYP	MAX	UNIT
$t_{d(RS)}$	CLKOUT1 low to reset state entered			22†	ns
$t_{d(IACK)}$	CLKOUT1 to $\overline{IACK}$ valid	– 6	0	12	ns
$t_{d(XF)}$	XF valid before falling edge of $\overline{STRB}$	Q – 15			ns

NOTES: 1 $Q = 1/4t_{c(C)}$.
6. $\overline{RS}$, $\overline{INT}$, and $\overline{BIO}$ are asynchronous inputs and can occur at any time during a clock cycle However, if the specified setup time is met, the exact sequence shown in the timing diagrams will occur.

timing requirements over recommended operating conditions (see Notes 1 and 6)

		MIN	NOM	MAX	UNIT
$t_{su(IN)}$	$\overline{INT}/\overline{BIO}/\overline{RS}$ setup before CLKOUT1 high	32			ns
$t_{h(IN)}$	$\overline{INT}/\overline{BIO}/\overline{RS}$ hold after CLKOUT1 high	0			ns
$t_{f(IN)}$	$\overline{INT}/\overline{BIO}$ fall time			8†	ns
$t_{w(IN)}$	$\overline{INT}/\overline{BIO}$ low pulse duration	$t_{c(C)}$			ns
$t_{w(RS)}$	$\overline{RS}$ low pulse duration	$3t_{c(C)}$			ns

† Value derived from characterization data and not tested.

NOTES: 1. $Q = 1/4t_{c(C)}$.
6. $\overline{RS}$, $\overline{INT}$, and $\overline{BIO}$ are asynchronous inputs and can occur at any time during a clock cycle. However, if the specified setup time is met, the exact sequence shown in the timing diagrams will occur.

$\overline{HOLD}$ TIMING

switching characteristics over recommended operating conditions (see Note 1)

	PARAMETER	MIN	TYP	MAX	UNIT
$t_{d(C1L-AL)}$	$\overline{HOLDA}$ low after CLKOUT1 low	0		10	ns
$t_{dis(AL-A)}$	$\overline{HOLDA}$ low to address three-state		0†		ns
$t_{dis(C1L-A)}$	Address three-state after CLKOUT1 low ($\overline{HOLD}$ mode, see Note 7)			20†	ns
$t_{d(HH-AH)}$	$\overline{HOLD}$ high to $\overline{HOLDA}$ high			25	ns
$t_{en(A-C1L)}$	Address driven before CLKOUT1 low ($\overline{HOLD}$ mode, see Note 7)			8†	ns

† Value derived from characterization data and not tested.

NOTES: 1. $Q = 1/4t_{c(C)}$.
7. A15-A0, $\overline{PS}$, $\overline{DS}$, $\overline{IS}$, $\overline{STRB}$, and R/$\overline{W}$ timings are all included in timings referenced as "address "

timing requirements over recommended operating conditions (see Note 1)

		MIN	NOM	MAX	UNIT
$t_{d(C2H-H)}$	$\overline{HOLD}$ valid after CLKOUT2 high			Q – 24	ns

NOTES: 1. $Q = 1/4t_{c(C)}$.

SERIAL PORT TIMING

switching characteristics over recommended operating conditions (see Note 1)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{d(CH-DX)}$	DX valid after CLKX rising edge (see Note 8)			75	ns
$t_{d(FL-DX)}$	DX valid after FSX falling edge (TXM = 0, see Note 8)			40	ns
$t_{d(CH-FS)}$	FSX valid after CLKX rising edge (TXM = 1)			40	ns

NOTES: 1. $Q = 1/4t_{c(C)}$.
8. The last occurrence of FSX falling and CLKX rising.

timing requirements over recommended operating conditions (see Note 1)

		TMS320C25 TMS320E25			TMS320C25-33			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$t_{c(SCK)}$	Serial port clock (CLKX/CLKR) cycle time†	200			242			ns
$t_{f(SCK)}$	Serial port clock (CLKX/CLKR) fall time			25‡			25‡	ns
$t_{r(SCK)}$	Serial port clock (CLKX/CLKR) rise time			25‡			25‡	ns
$t_{w(SCK)}$	Serial port clock (CLKX/CLKR) low pulse duration (see Note 9)	80			97			ns
$t_{w(SCK)}$	Serial port clock (CLKX/CLKR) high pulse duration (see Note 9)	80			97			ns
$t_{su(FS)}$	FSX/FSR setup time before CLKX/CLKR falling edge (TXM = 0)	18			18			ns
$t_{h(FS)}$	FSX/FSR hold time after CLKX/CLKR falling edge (TXM = 0)	20			20			ns
$t_{su(DR)}$	DR setup time before CLKR falling edge	10			10			ns
$t_{h(DR)}$	DR hold time after CLKR falling edge	20			20			ns

† The serial port was tested at a minimum frequency of 1.25 MHz. However, the serial port was fully static but will properly function down to f_{SX} = 0 Hz.
‡ Value derived from characterization data and not tested.
NOTES: 1. $Q = 1/4t_{c(C)}$.
9. The duty cycle of the serial port clock must be within 40-60%.

EPROM PROGRAMMING

absolute maximum ratings over specified temperature range (unless otherwise noted)†

Supply voltage range, V_{PP}‡ . . . . . – 0.6 V to 15 V
Input voltage range on pins 24 and 25 . . . . . – 0.3 V to 15 V

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ All voltage values are with respect to GND.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Programming mode supply voltage (see Note 11)		6		V
V_{CC}	Read mode supply voltage	4.75	5	5.25	V
V_{PP}	Programming mode supply voltage	12	12.5	13	V
V_{PP}	Read mode supply voltage (see Note 10)		V_{CC}		V

NOTES: 10. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be $I_{CC} + I_{PP}$. During programming, V_{PP} must be maintained at 12.5 V (± 0.25 V).
11. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. This device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.

electrical characteristics over specified temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP§	MAX	UNIT
I_{PP1}	V_{PP} supply current	$V_{PP} = V_{CC} = 5.25$ V			100	µA
I_{PP2}	V_{PP} supply current (during program pulse)	$V_{PP} = 13$ V		30	50	mA

§ All typical values for I_{CC} are at $V_{CC} = 5$ V, $T_A = 25°C$.

recommended timing requirements for programming, $T_A = 25°C$, $V_{CC} = 6$ V, $V_{PP} = 12.5$ V (see Notes 12 and 13)

		MIN	NOM	MAX	UNIT
$t_{w(IPGM)}$	Initial program pulse duration	0.95	1	1.05	ms
$t_{w(FPGM)}$	Final pulse duration	2.85		78.75	ms
$t_{su(A)}$	Address setup time	2			µs
$t_{su(E)}$	$\overline{E}$ setup time	2			µs
$t_{su(G)}$	$\overline{G}$ setup time	2			µs
$t_{dis(G)}$	Output disable time from $\overline{G}$	0		130¶	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			150¶	ns
$t_{su(D)}$	Data setup time	2			µs
$t_{su(VPP)}$	V_{PP} setup time	2			µs
$t_{su(VCC)}$	V_{CC} setup time	2			µs
$t_{h(A)}$	Address hold time	0			µs
$t_{h(D)}$	Data hold time	2			µs

¶ Value derived from characterization data and not tested.

NOTES: 12. For all switching characteristics and timing measurements, input pulse levels are 0.4 V to 2.4 V and V_{PP} = 12.5 V ± 0.5 V during programming.
13. Common test conditions apply for $t_{dis(G)}$ except during programming.

absolute maximum ratings over specified temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}‡ ..... –0.3 V to 7 V
Input voltage range ..... –0.3 V to 7 V
Output voltage range ..... –0.3 V to 7 V
Continuous power dissipation ..... 1.5 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... –55°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ All voltage values are with respect to V_{SS}.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{SS}	Supply voltage			0		V
V_{IH}	High-level input voltage	$\overline{INT0}$-$\overline{INT2}$	2.5			V
		CLKIN, CLKX, CLKR	3.5			V
		Other inputs	2.35			V
V_{IL}	Low-level input voltage	MP/$\overline{MC}$			0.8	V
		CLKIN			0.8	V
		Other inputs			0.8	V
I_{OH}	High-level output current				300	μA
I_{OL}	Low-level output current				2	mA
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over specified free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP§	MAX	UNIT
V_{OH}	High-level output voltage		V_{CC} = MIN, I_{OH} = MAX	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, I_{OL} = MAX			0.6	V
I_Z	High-impedance current		V_{CC} = MAX	–20		20	μA
I_I	Input current		V_I = V_{SS} to V_{CC}	–10		10	μA
I_{CC}	Supply current	Normal	T_A = 0°C, V_{CC} = MAX, F_x = MAX		110	185	mA
		Idle, $\overline{HOLD}$			50	100	
C_I	Input capacitance				15		pF
C_O	Output capacitance				15		pF

§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

CLOCK CHARACTERISTICS AND TIMING

The TMS320C25-50 can use either its internal oscillator or an external frequency source for a clock.

internal clock option

The internal oscillator is enabled by connecting a crystal across X1 and X2, CLKIN. The frequency of CLKOUT1 is one-fourth the crystal fundamental frequency. The crystal should be in either fundamental or overtone mode, and parallel resonant, with an effective series resistance of 30 Ω, a power dissipation of 1 mW, and be specified at a load capacitance of 20 pF. Note that overtone crystals require an additional tuned LC circuit.

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
f_X	Input clock frequency	T_A = 0°C to 70°C	6.7		51.2	MHz
f_{SX}	Serial port frequency	T_A = 0°C to 70°C	0		6.4	MHz
C1, C2		T_A = 0°C to 70°C		10		pF

† The serial port was tested at a minimum frequency of 1.25 MHz. However, the serial port was fully static but will properly function down to f_{SX} = 0 Hz.

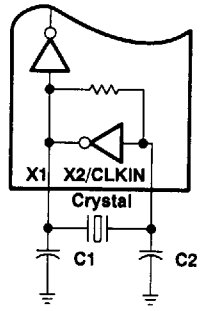


Figure 6. Internal Clock Option

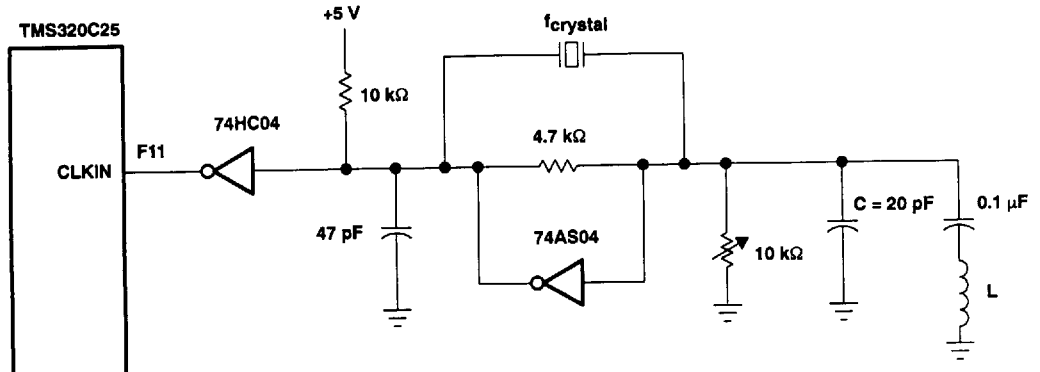
external clock option

An external frequency source can be used by injecting the frequency directly into X2/CLK, with X1 left unconnected. The external frequency injected must conform to specifications listed in the following table.

switching characteristics over recommended operating conditions (see Note 1)

		MIN	NOM	MAX	UNIT
$t_{c(C)}$	CLKOUT1, CLKOUT2 cycle time	78 13		597	ns
$t_{d(CIH-C)}$	CLKIN high to CLKOUT1, CLKOUT2, $\overline{STRB}$ high, low	5		27	ns
$t_{f(C)}$	CLKOUT1, CLKOUT2, $\overline{STRB}$ fall time			4	ns
$t_{r(C)}$	CLKOUT1, CLKOUT2, $\overline{STRB}$ rise time			4	ns
$t_{w(CL)}$	CLKOUT1, CLKOUT2, $\overline{STRB}$ low pulse duration	2Q – 7		2Q + 3	ns
$t_{w(CH)}$	CLKOUT1, CLKOUT2, $\overline{STRB}$ high pulse duration	2Q – 3		2Q + 7	ns
$t_{d(C1-C2)}$	CLKOUT1 high to CLKOUT2 low, CLKOUT2 high to CLKOUT1 high, etc.	Q – 5		Q + 5	ns

NOTE 1: Q = 1/4 $t_{c(C)}$



	$f_{crystal}$ (MHz)	L (µH)
TMS320C25	40.96	1.8
TMS320C25-50	51.20	1.0
TMS320E25	40.96	1.8

Figure 7. External Clock Option

timing requirements over recommended operating conditions (see Note 1)

		MIN	NOM	MAX	UNIT
$t_{c(CI)}$	CLKIN cycle time	19.53		150	ns
$t_{f(CI)}$	CLKIN fall time			5†	ns
$t_{r(CI)}$	CLKIN rise time			5†	ns
$t_{w(CIL)}$	CLKIN low pulse duration, $t_{c(CI)}$ = 50 ns (see Note 2)	20			ns
$t_{w(CIH)}$	CLKIN high pulse duration, $t_{c(CI)}$ = 50 ns (see Note 2)	20			ns
$t_{su(S)}$	$\overline{SYNC}$ setup time before CLKIN low	4		Q – 4	ns
$t_{h(S)}$	$\overline{SYNC}$ hold time from CLKIN low	4			ns

† Value derived from characterization data and not tested.

NOTES: 1. Q = 1/4 $t_{c(C)}$
2. CLKIN duty cycle $[t_{r(CI)} + t_{w(CIH)}]/t_{c(CI)}$ must be within 40-60%.

MEMORY AND PERIPHERAL INTERFACE TIMING

switching characteristics over recommended operating conditions (see Note 1)

	PARAMETER	MIN	TYP	MAX	UNIT
$t_{d(C1-S)}$	$\overline{STRB}$ from CLKOUT (if $\overline{STRB}$ is present)	Q – 5		Q + 3	ns
$t_{d(C2-S)}$	CLKOUT2 to $\overline{STRB}$ (if $\overline{STRB}$ is present)	– 2		5	ns
$t_{su(A)}$	Address setup time before $\overline{STRB}$ low (see Note 3)	Q – 11			ns
$t_{h(A)}$	Address hold time after $\overline{STRB}$ high (see Note 3)	Q – 4			ns
$t_{w(SL)}$	$\overline{STRB}$ low pulse duration (no wait states, see Note 4)	2Q – 5		2Q + 2	ns
$t_{w(SH)}$	$\overline{STRB}$ high pulse duration (between consecutive cycles, see Note 4)	2Q – 2		2Q + 5†	ns
$t_{su(D)W}$	Data write setup time before $\overline{STRB}$ high (no wait)	2Q – 17			ns
$t_{h(D)W}$	Data write hold time from $\overline{STRB}$ high	Q – 5			ns
$t_{en(D)}$	Data bus starts being driven after $\overline{STRB}$ low (write)	0†			ns
$t_{dis(D)}$	Data bus high-impedance state after $\overline{STRB}$ high, (write)		Q	Q + 15†	ns
$t_{d(MSC)}$	$\overline{MSC}$ valid from CLKOUT1	– 2		9	ns

† Value derived from characterization data and not tested.

NOTES: 1. $Q = 1/4t_{c(C)}$.

3. A15-A0, $\overline{PS}$, $\overline{DS}$, $\overline{IS}$, R/$\overline{W}$, and $\overline{BR}$ timings are all included in timings referenced as "address"
4. Delay between CLKOUT1, CLKOUT2, and $\overline{STRB}$ edges track each other, resulting in $t_{w(SL)}$ and $t_{w(SH)}$ being 2Q with no wait state

timing requirements over recommended operating conditions (see Note 1)

		MIN	NOM	MAX	UNIT
$t_{a(A)}$	Read data access time from address time (see Notes 3 and 5)			3Q – 30	ns
$t_{su(D)R}$	Data read setup time before $\overline{STRB}$ high	19			ns
$t_{h(D)R}$	Data read hold time from $\overline{STRB}$ high	0			ns
$t_{d(SL-R)}$	READY valid after $\overline{STRB}$ low (no wait states)			Q – 21	ns
$t_{d(C2H-R)}$	READY valid after CLKOUT2 high			Q – 21	ns
$t_{h(SL-R)}$	READY hold time after $\overline{STRB}$ low (no wait states)	Q – 1			ns
$t_{h(C2H-R)}$	READY valid after CLKOUT2 high	Q – 1			ns
$t_{d(M-R)}$	READY valid after $\overline{MSC}$ valid			2Q – 24	ns
$t_{h(M-R)}$	READY hold time after $\overline{MSC}$ valid	0			ns

NOTES: 1. $Q = 1/4t_{c(C)}$.

3. A15-A0, $\overline{PS}$, $\overline{DS}$, $\overline{IS}$, R/$\overline{W}$, and $\overline{BR}$ timings are all included in timings referenced as "address".
5. Read data access time is defined as $t_{a(A)} = t_{su(A)} + t_{w(SL)} - t_{su(D)R}$.

$\overline{RS}$, $\overline{INT}$, $\overline{BIO}$, AND XF TIMING

switching characteristics over recommended operating conditions (see Notes 1 and 14)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{d(RS)}$	CLKOUT1 low to reset state entered			22†	ns
$t_{d(IACK)}$	CLKOUT1 to $\overline{IACK}$ valid	−5		7	ns
$t_{d(XF)}$	XF valid before falling edge of $\overline{STRB}$	Q − 8			ns

† Value derived from characterization data and not tested.

NOTES: 1. $Q = 1/4\ t_{c(C)}$

14. $\overline{RS}$, $\overline{INT}$, $\overline{BIO}$ are asynchronous inputs and can occur at any time during a clock cycle.

timing requirements over recommended operating conditions (see Notes 1 and 14)

		MIN	NOM	MAX	UNIT
$t_{su(IN)}$	$\overline{INT}$, $\overline{BIO}$, $\overline{RS}$ setup before CLKOUT1 high	25			ns
$t_{h(IN)}$	$\overline{INT}$, $\overline{BIO}$, $\overline{RS}$ hold after CLKOUT1 high	0			ns
$t_{f(IN)}$	$\overline{INT}$, $\overline{BIO}$ fall time			8†	ns
$t_{w(IN)}$	$\overline{INT}$, $\overline{BIO}$ low pulse duration	$t_{c(C)}$			ns
$t_{w(RS)}$	$\overline{RS}$ low pulse duration	$3t_{c(C)}$			ns

† Value derived from characterization data and not tested.

NOTES: 1. $Q = 1/4\ t_{c(C)}$

15. $\overline{RS}$, $\overline{INT}$, $\overline{BIO}$ are asynchronous inputs and can occur at any time during a clock cycle.

$\overline{HOLD}$ TIMING

switching characteristics over recommended operating conditions (see Note 1)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{d(CIL-AL)}$	$\overline{HOLDA}$ low after CLKOUT1 low	1†		11	ns
$t_{dis(AL-A)}$	$\overline{HOLDA}$ low to address high-impedance		0†		ns
$t_{dis(CIL-A)}$	Address high-impedance after CLKOUT1 low ($\overline{HOLD}$ mode, see Note 7)			20†	ns
$t_{d(HH-AH)}$	$\overline{HOLD}$ high to $\overline{HOLDA}$ high			19	ns
$t_{en(A-CIL)}$	Address driven before CLKOUT1 low ($\overline{HOLD}$ mode, see Note 7)			8†	ns

† Value derived from characterization data and not tested.

NOTES: 1. $Q = 1/4\ t_{c(C)}$

7. A15-A0, $\overline{PS}$, $\overline{DS}$, $\overline{IS}$, $\overline{STRB}$, and R/$\overline{W}$ timings are all included in timings referenced as "address"

timing requirements over recommended operating conditions (see Note 1)

		MIN	NOM	MAX	UNIT
$t_{d(C2H-H)}$	$\overline{HOLD}$ valid after CLKOUT2 high			Q − 19	ns

NOTE 1: $Q = 1/4\ t_{c(C)}$

SERIAL PORT TIMING

switching characteristics over recommended operating conditions (see Note 1)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{d(CH-DX)}$	DX valid after CLKX rising edge (see Note 8)			75	ns
$t_{d(FL-DX)}$	DX valid after falling edge (TXM = 0, see Note 8)			40	ns
$t_{d(CH-FS)}$	FSX valid after CLKX raising edge (TXM = 1)			40	ns

NOTES: 1. $Q = 1/4\ t_{c(C)}$
8. The last occurrence of FSX falling and CLKX rising.

timing requirements over recommended operating conditions (see Note 1)

		MIN	NOM	MAX	UNIT
$t_{c(SCK)}$	Serial port clock (CLKX/CLKR) cycle time†	160			ns
$t_{f(SCK)}$	Serial port clock (CLKX/CLKR) fall time			25‡	ns
$t_{r(SCK)}$	Serial port clock (CLKX/CLKR) rise time			25‡	ns
$t_{w(SCK)}$	Serial port clock (CLKX/CLKR) low or high pulse duration (see Note 9)	64			ns
$t_{su(FS)}$	FSX or FSR setup time before CLKX, CLKR falling edge (TXM = 0)	5			ns
$t_{h(FS)}$	FSX or FSR hold time before CLKX, CLKR falling edge (TXM = 0)	10			ns
$t_{su(DR)}$	DR setup time before CLKR falling edge	5			ns
$t_{h(DR)}$	DR hold time after CLKR falling edge	10			ns

† The serial port was tested at a minimum frequency of 1.25 MHz. However, the serial port was fully static but will properly function down to $f_{SX} = 0$ Hz.
‡ Value derived from characterization data and not tested.
NOTES: 1. $Q = 1/4\ t_{c(C)}$
9. The cycle of the serial port must be within 40%-60%.

PARAMETER MEASUREMENT INFORMATION

This section contains all the timing diagrams for the TMS320 second-generation devices. Refer to the top corner of page for the specific device.

Timing measurements are referenced to and from a low voltage of 0.8 voltage and a high voltage of 2 volts, unless otherwise noted.

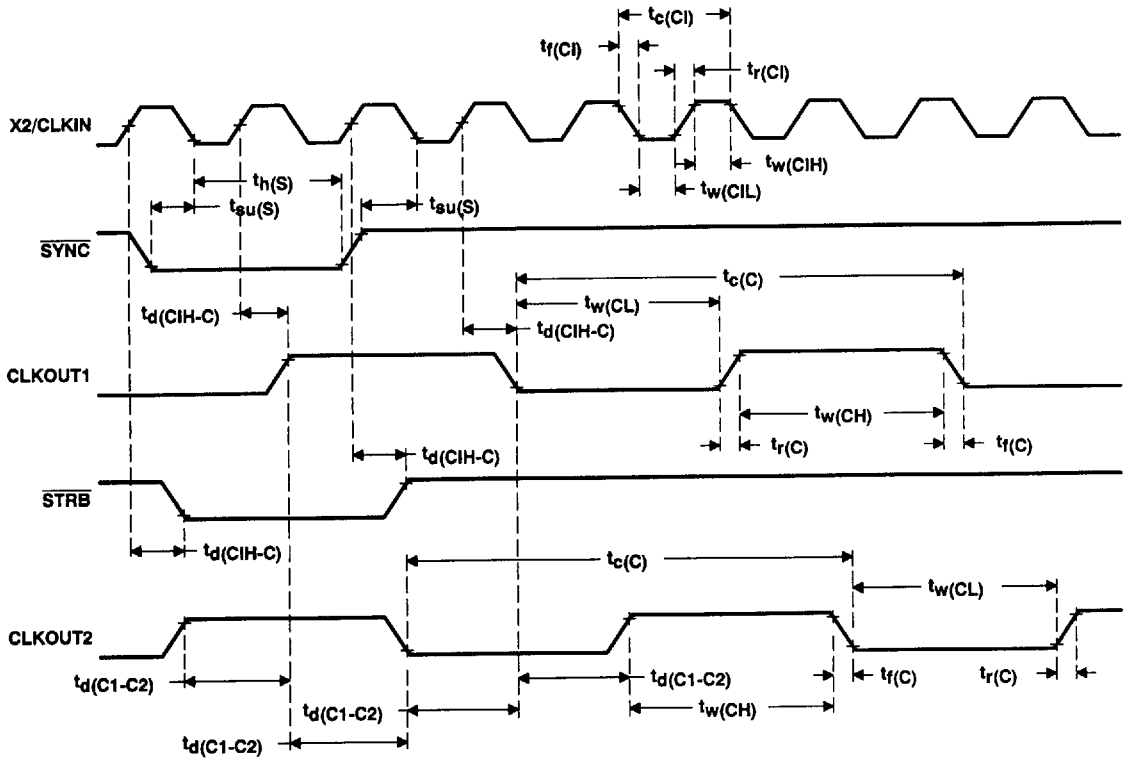


Figure 8. Clock Timing

PARAMETER MEASUREMENT INFORMATION

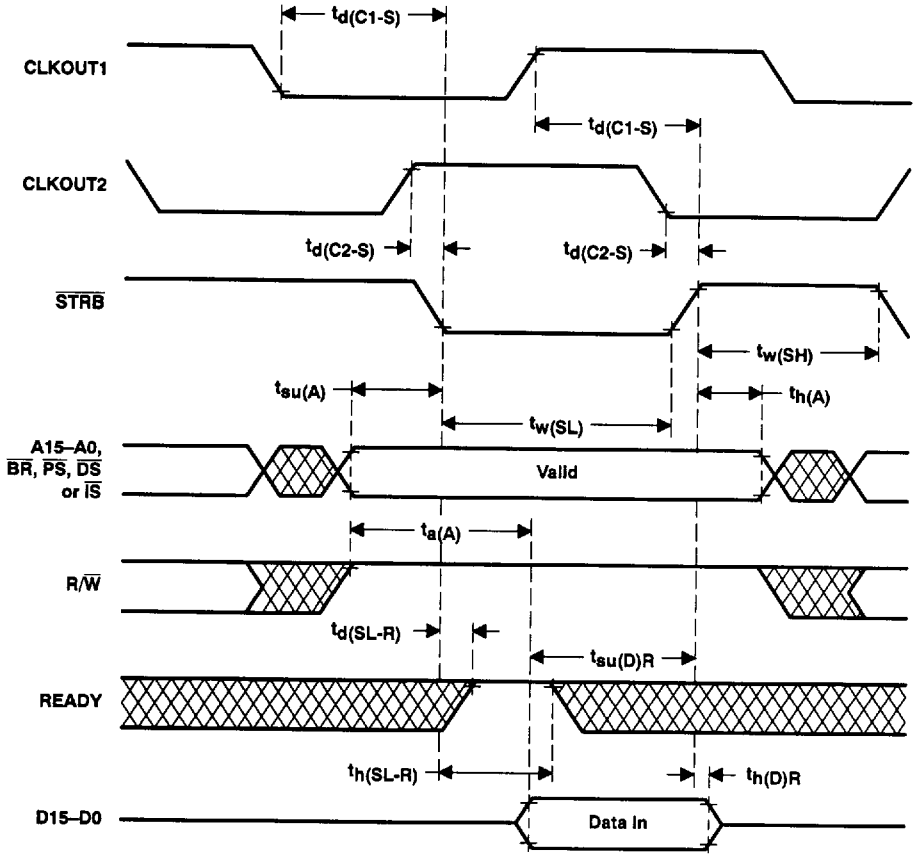


Figure 9. Memory Read Timing

PARAMETER MEASUREMENT INFORMATION

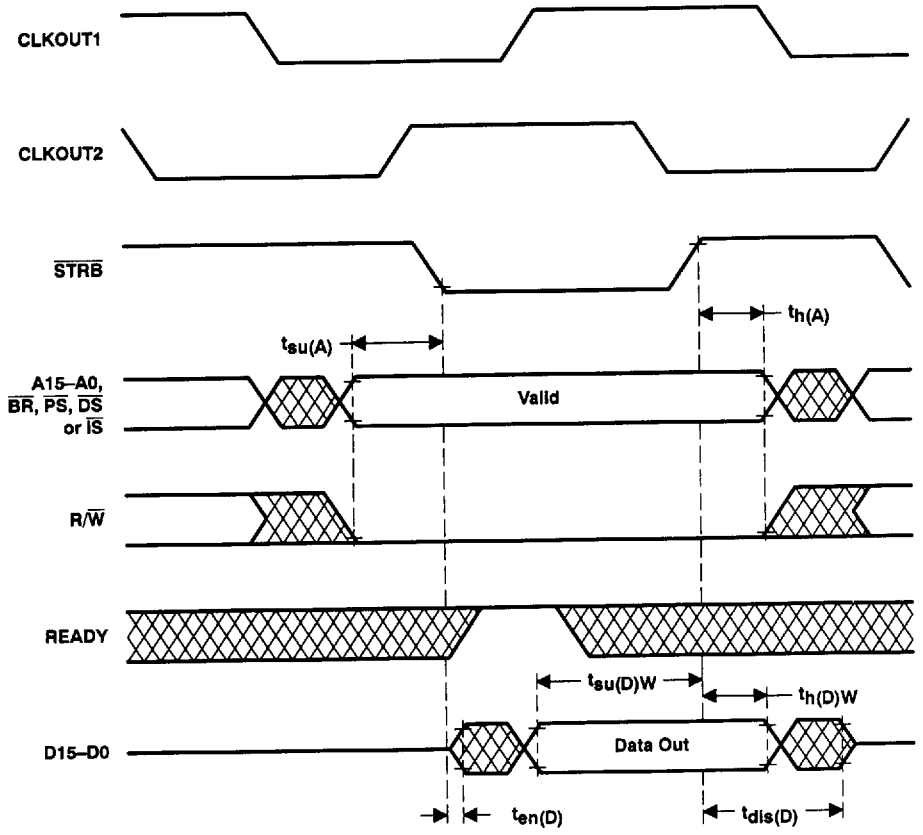


Figure 10. Memory Write Timing

PARAMETER MEASUREMENT INFORMATION

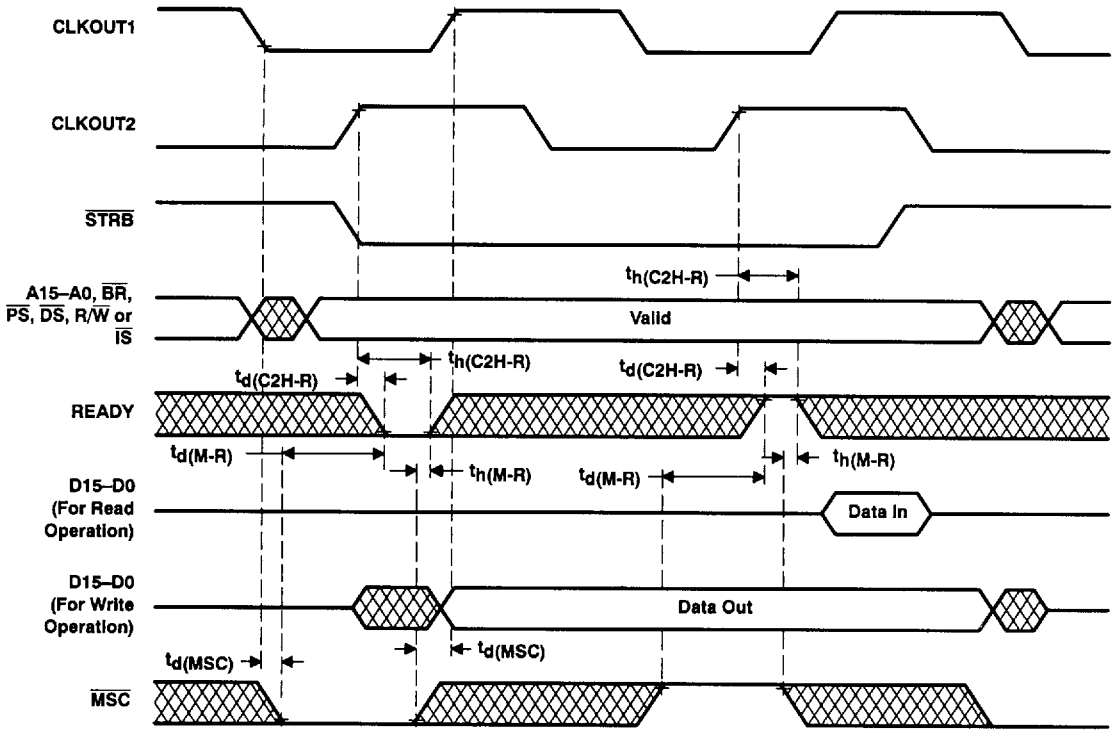
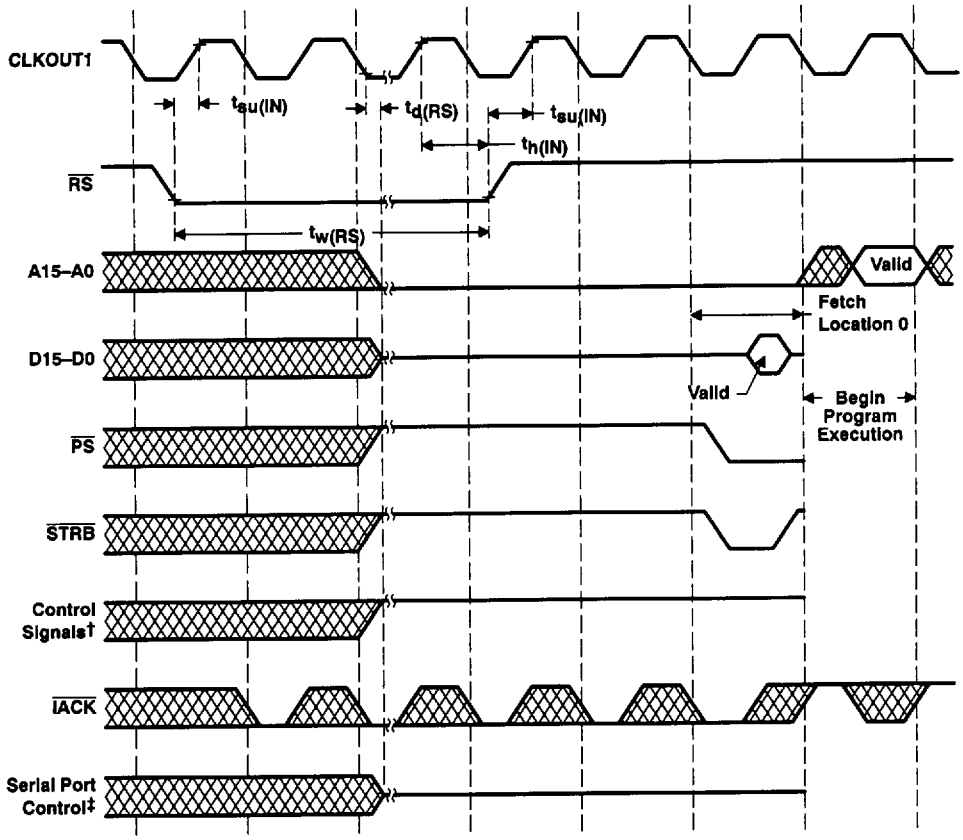


Figure 11. One Wait-State Memory Access Timing

PARAMETER MEASUREMENT INFORMATION



† Control signals are $\overline{DS}$, $\overline{IS}$, R/$\overline{W}$, and XF.
‡ Serial port controls are DX and FSX.

Figure 12. Reset Timing

PARAMETER MEASUREMENT INFORMATION

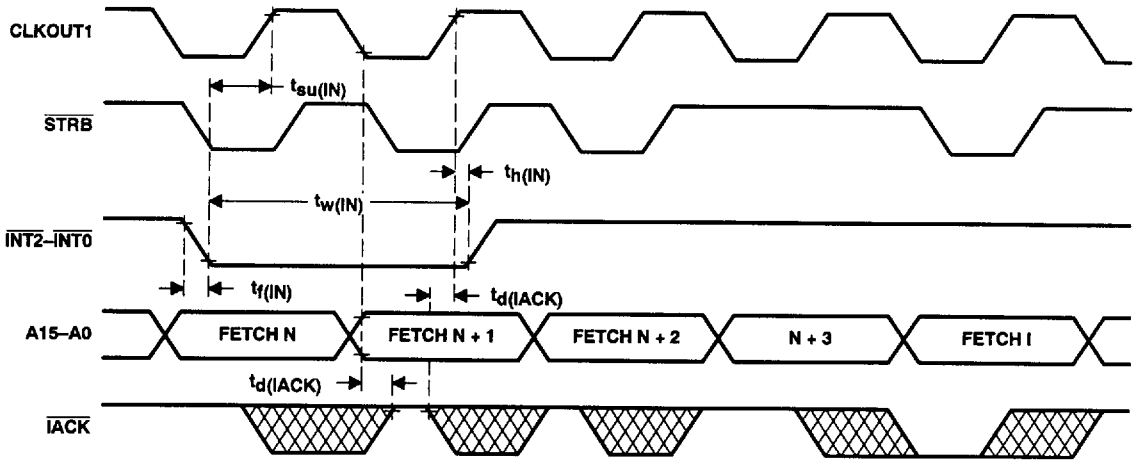


Figure 13. Interrupt Timing

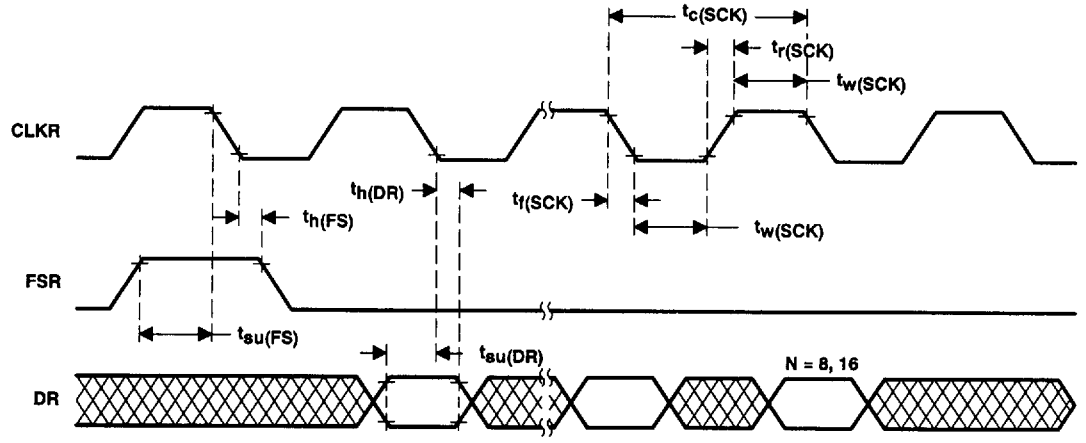


Figure 14. Serial Port Receive Timing

PARAMETER MEASUREMENT INFORMATION

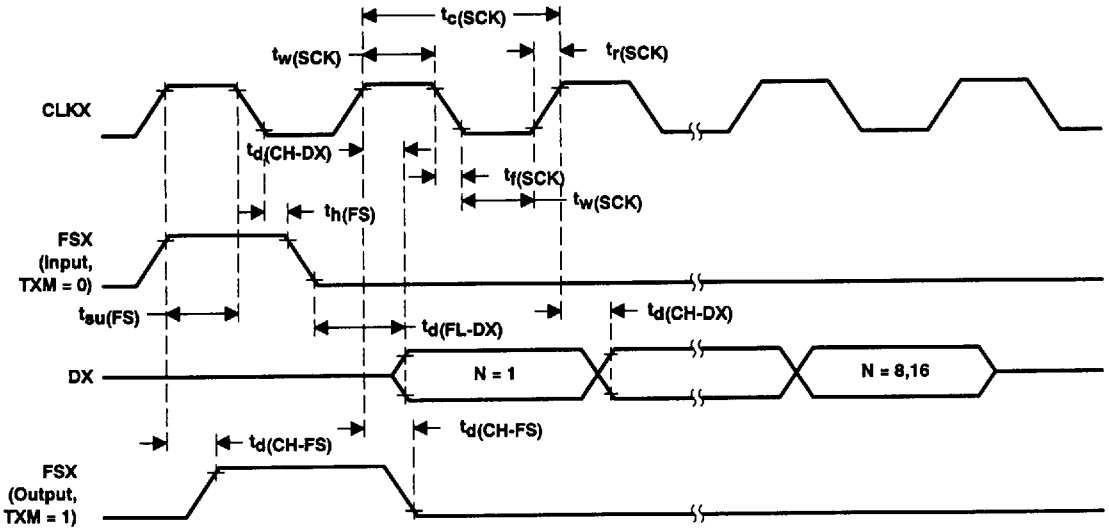


Figure 15. Serial Port Transmit Timing

PARAMETER MEASUREMENT INFORMATION

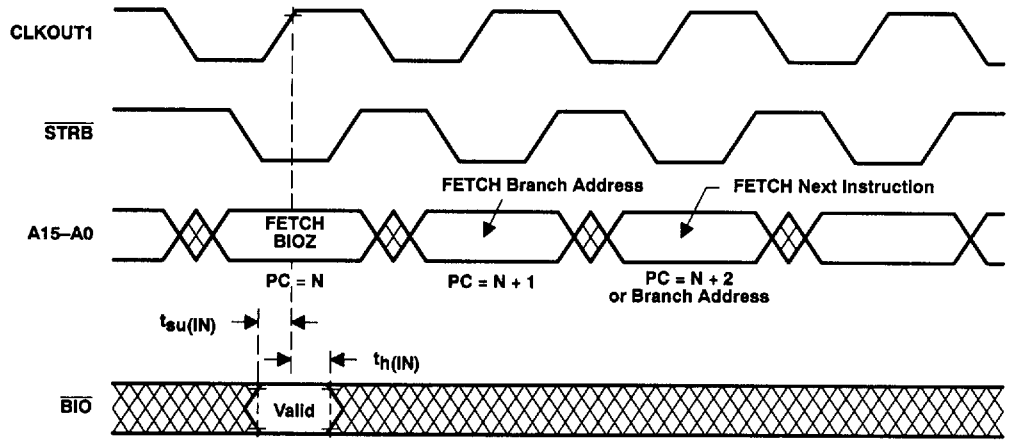


Figure 16. $\overline{BIO}$ Timing

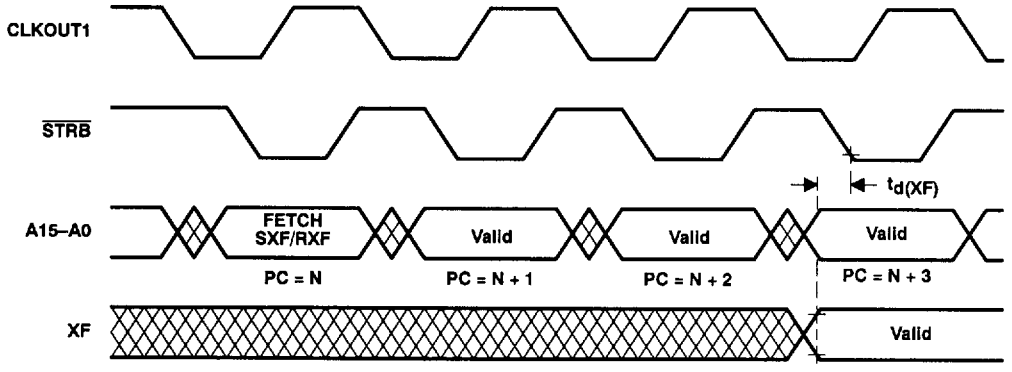
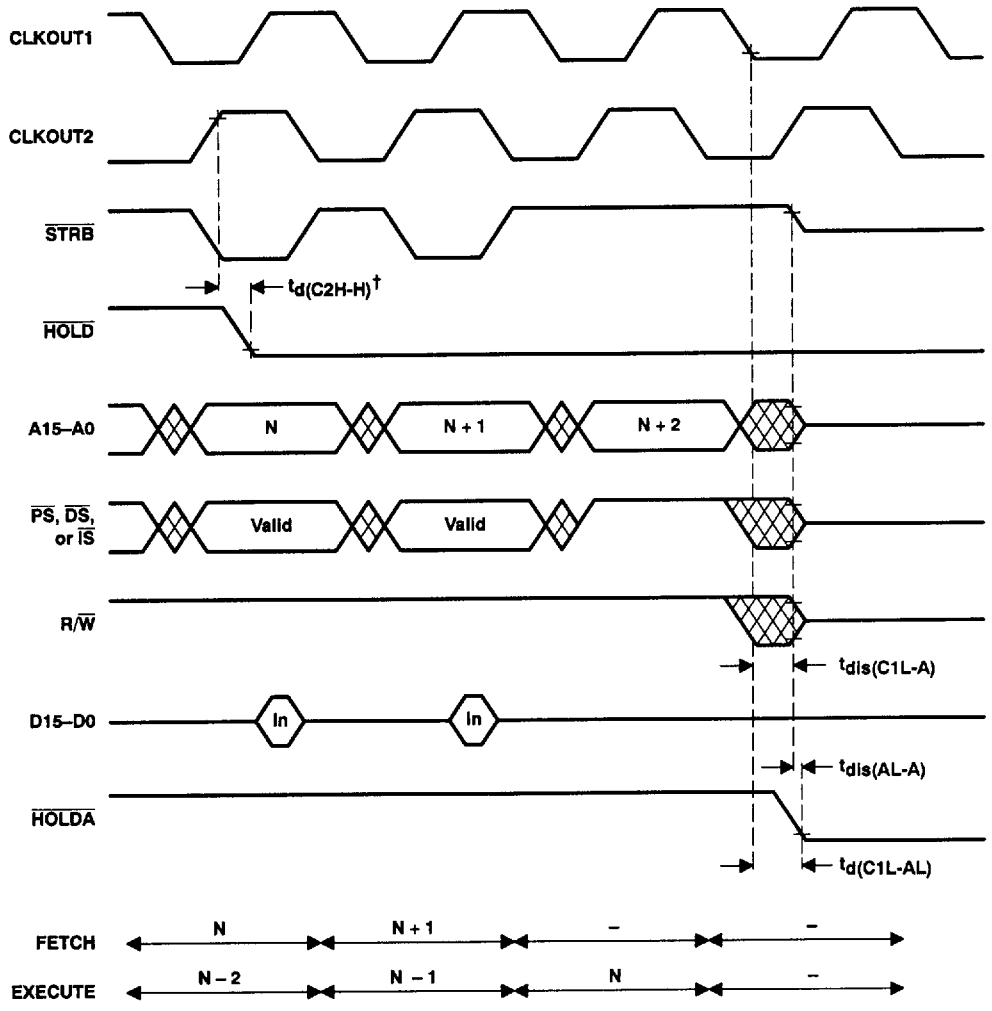


Figure 17. External Flag Timing

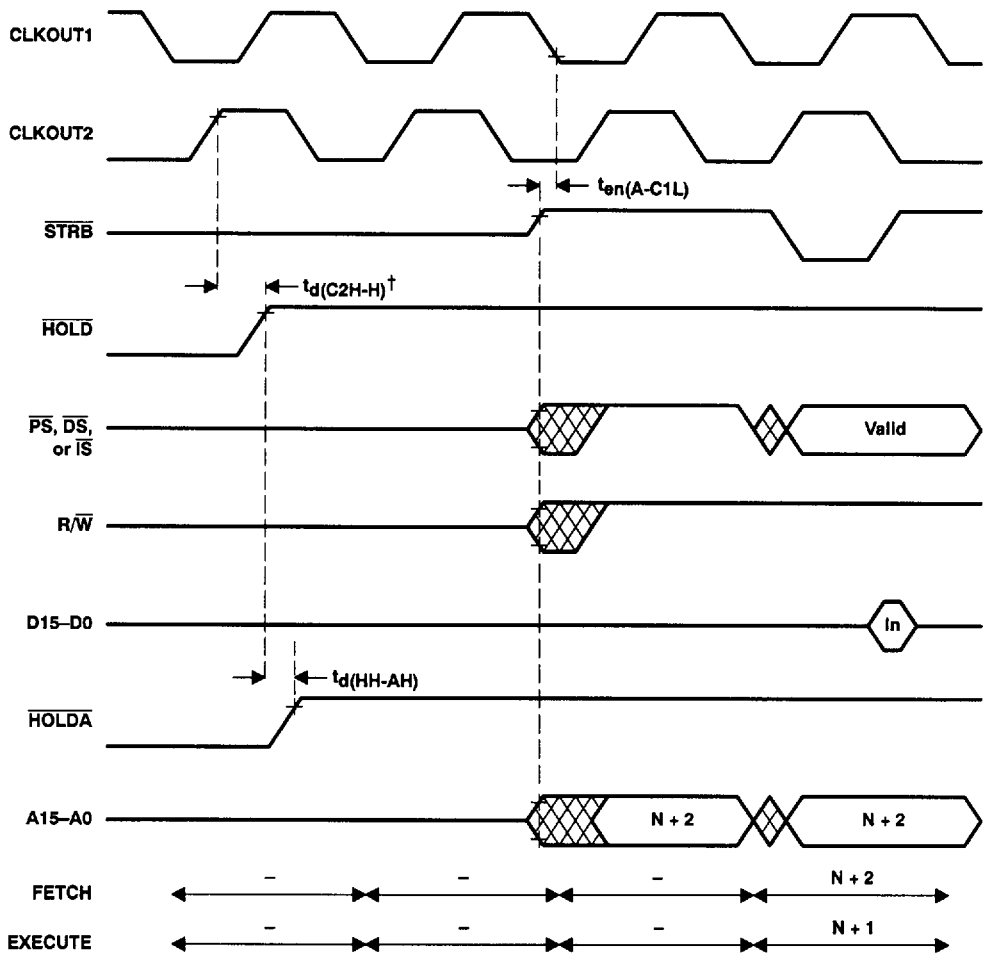
PARAMETER MEASUREMENT INFORMATION



† $\overline{\text{HOLD}}$ is an asynchronous input and can occur at any time during a clock cycle. If the specified timing is met, the exact sequence shown will occur; otherwise, a delay of one CLKOUT2 cycle will occur.

Figure 18. $\overline{\text{HOLD}}$ Timing (Part A)

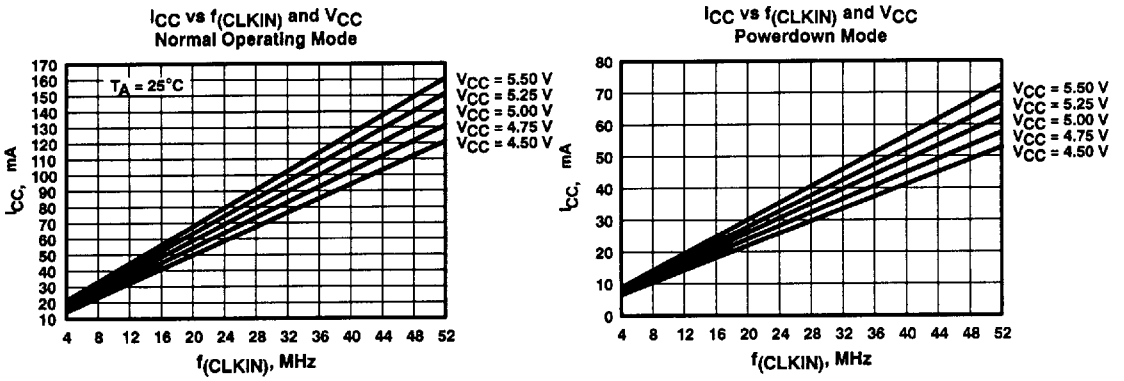
PARAMETER MEASUREMENT INFORMATION



† $\overline{\text{HOLD}}$ is an asynchronous input and can occur at any time during a clock cycle. If the specified timing is met, the exact sequence shown will occur; otherwise, a delay of one CLKOUT2 cycle will occur.

Figure 19. $\overline{\text{HOLD}}$ Timing (Part B)

TYPICAL SUPPLY CURRENT CHARACTERISTICS FOR TMS320C25



TMS320C25FNL (PLCC) reflow soldering precautions

Recent tests have identified an industry-wide problem experienced by surface mounted devices exposed to reflow soldering temperatures. This problem involves a package cracking phenomenon sometimes experienced by large (e.g., 68-lead) plastic leaded chip carrier (PLCC) packages during surface mount manufacturing. This phenomenon occur if the TMS320C25FNL is exposed to uncontrolled levels of humidity prior to reflow solder. This moisture can flash to steam during solder reflow, causing sufficient stress to crack the package and compromise device integrity. If the TMS320C25FNL is being socketed, *no* special handling precautions are required. In addition, once the device is soldered into the board, *no* special handling precautions are required.

In order to minimize moisture absorption, TI ships the TMS320C25FNL in "dry pack" shipping bags with a RH indicator card and moisture-absorbing desiccant. These moisture-barrier shipping bags will adequately block moisture transmission to allow shelf storage for 12 months from date of seal when stored at less than 60% relative humidity (RH) and less than 30°C. Devices may be stored outside the sealed bags indefinitely if stored at less than 25% RH and 30°C.

Once the bag seal is broken, the devices should be stored at less than 60% RH and 30°C as well as reflow soldered within two days of removal. In the event that either of the above conditions is not met, TI recommends these devices be baked in a clean oven at 125°C and 10% maximum RH for 24 hours. This restores the devices to their "dry packed" moisture level.

NOTE

Shipping tubes will not withstand the 125°C baking process. Devices should be transferred to a metal tray or tube before baking. Standard ESD precautions should be followed.

In addition, TI recommends that the reflow process not exceed two solder cycles and the temperature not exceed 220°C.

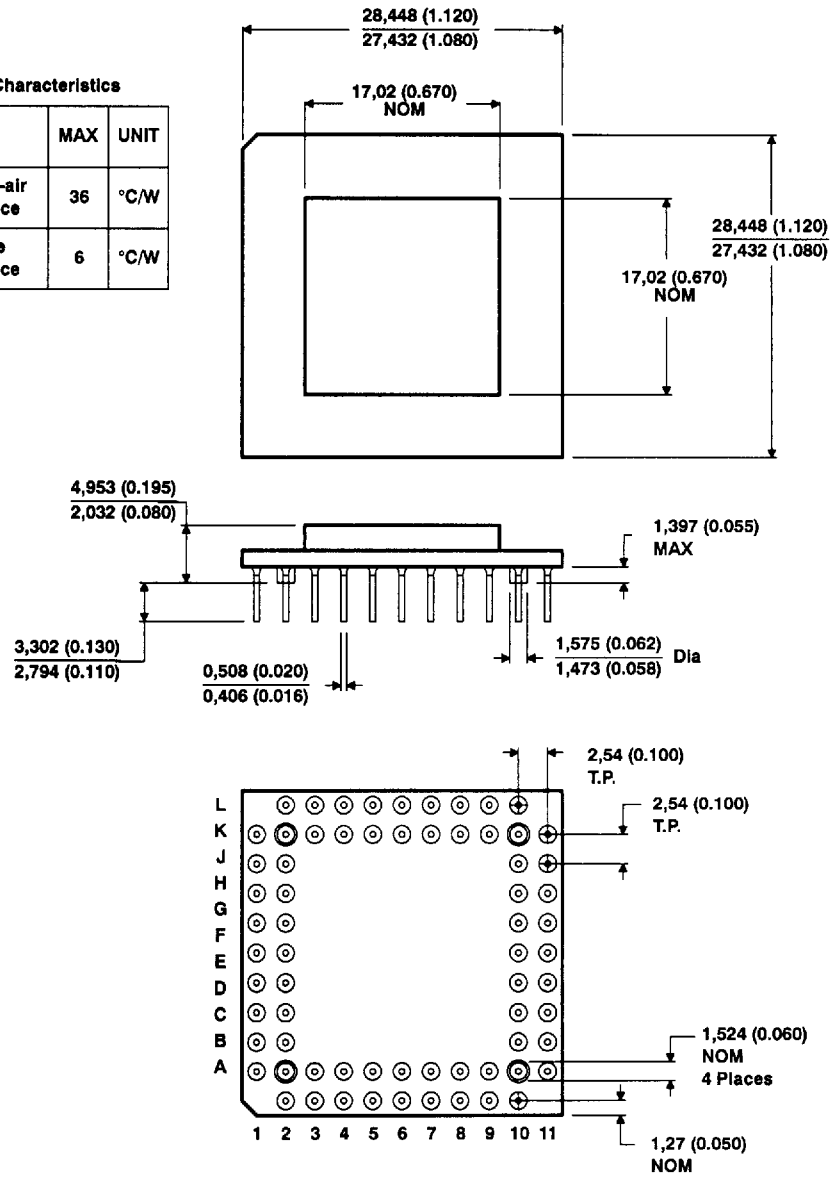
If you have any additional questions or concerns, please contact your local TI representative.

MECHANICAL DATA

68-pin GB grid array ceramic package (TMS320C25)

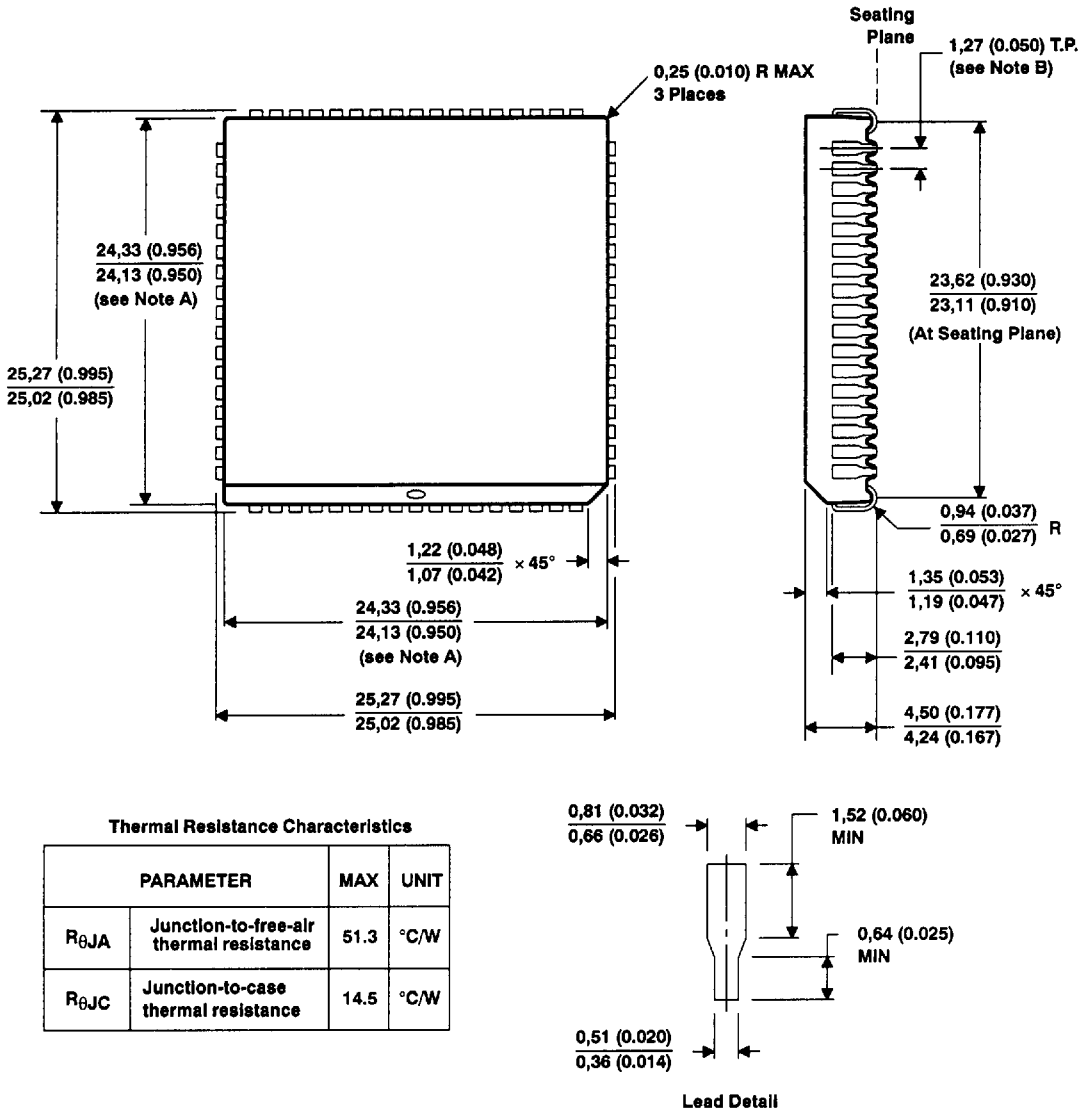
Thermal Resistance Characteristics

PARAMETER		MAX	UNIT
$R_{\theta JA}$	Junction-to-free-air thermal resistance	36	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance	6	°C/W



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

68-lead plastic leaded chip carrier package (TMS320C25, TMS320C25-33, and TMS320C25-50)



Thermal Resistance Characteristics

PARAMETER		MAX	UNIT
$R_{\theta JA}$	Junction-to-free-air thermal resistance	51.3	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance	14.5	°C/W

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Centerline of center pin, each side, is within 0,10 (0.004) of package centerline as determined by this dimension.
B. Location of each pin is within 0,127 (0.005) of true position with respect to center pin on each side.

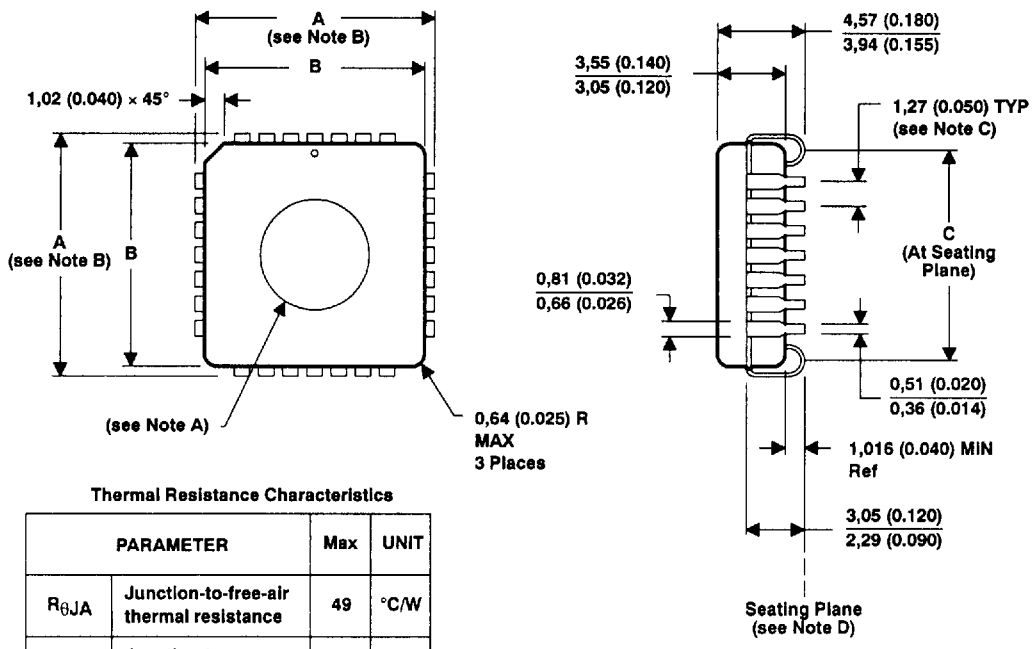
WARNING

When reflow soldering is required, refer to page 42 for special handling instructions.

MECHANICAL DATA

68-lead FZ CER-QUAD, ceramic leaded chip carrier package (TMS320E25 only)

This hermetically-sealed chip carrier package consists of a ceramic base, ceramic cap, and a 68-lead frame. Hermetic sealing is accomplished with glass. The FZ package is intended for both socket- or surface-mounting. Having a Sn/Pb ratio of 60/40, the tin/lead-coated leads do not require special cleaning or processing when being surface-mounted. The 28-pin package is shown in the illustration; refer to the table below for 68-pin package dimensions.



Thermal Resistance Characteristics

PARAMETER		Max	UNIT
$R_{\theta JA}$	Junction-to-free-air thermal resistance	49	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance	8	°C/W

JEDEC OUTLINE	NO. OF TERMINALS	A		B		C	
		MIN	MAX	MIN	MAX	MIN	MAX
MO-087AA	28	12,32 (0.485)	12,57 (0.495)	10,92 (0.430)	11,56 (0.455)	10,41 (0.410)	10,92 (0.430)
MO-087AB	44	17,40 (0.685)	17,65 (0.695)	16,00 (0.630)	16,64 (0.655)	15,49 (0.610)	16,00 (0.630)
—	68	25,02 (0.985)	25,27 (0.995)	23,62 (0.930)	24,26 (0.955)	23,11 (0.910)	23,62 (0.930)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Glass is optional, and the diameter is dependent on device application.
B Centerline of center pin, each side, is within 0,10 (0.004) of package centerline as determined by dimension B.
C. Location of each pin is within 0,127 (0.005) of true position with respect to center pin on each side.
D. The lead contact points are within 0,15 (0.006) of being planar.

programming the TMS320E25 EPROM cell

The TMS320E25 includes a 4K × 16-bit EPROM, implemented from an industry-standard EPROM cell, to perform prototyping and early field testing and to achieve low-volume production. When used with a 4K-word masked-ROM TMS320C25, the TMS320E25 yields a high-volume, low-cost production as a result of more migration paths for data. An EPROM adapter socket (part # TMDX3270120), shown in Figure 20, is available to provide 68-pin to 28-pin conversion for programming the TMS320E25.

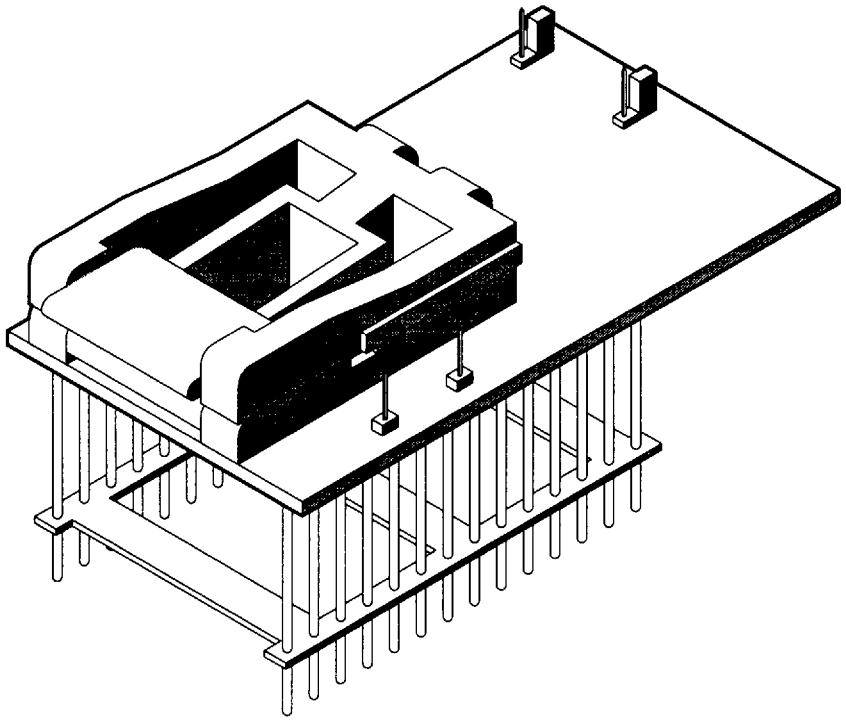


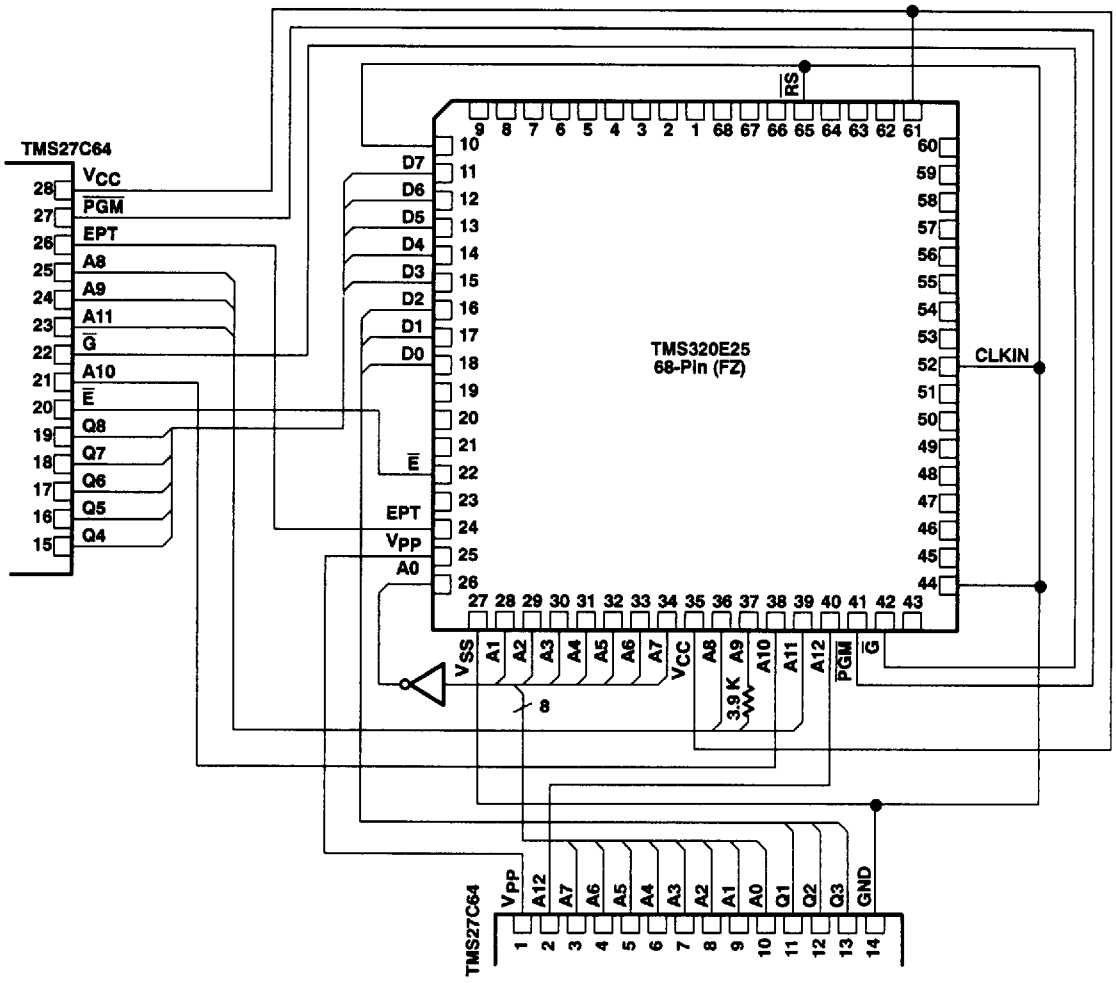
Figure 20. EPROM Adapter Socket

Key features of the EPROM cell include standard programming and verification. For security against copyright violations, the EPROM cell features an internal protection mechanism to prevent proprietary code from being read. The protection feature can be used to protect reading the EPROM contents. This section describes erasure, fast programming and verification, and EPROM protection and verification.

fast programming and verification

The TMS320E25 EPROM cell is programmed using the same family and device codes as the TMS27C64 8K × 8-bit EPROM. The TMS27C64 EPROM series are ultraviolet-light erasable, electrically programmable read-only memories, fabricated using HVCMOS technology. The TMS27C64 is pin-compatible with existing 28-pin ROMs and EPROMs. The TMS320E25, like the TMS27C64, operates from a single 5-V supply in the read mode; however, a 12.5-V supply is needed for programming. All programming signals are TTL level. For programming outside the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random. When programmed in blocks, the data is loaded into the EPROM cell one byte at a time, the high byte first and the low byte second.

Figure 21 shows the wiring conversion to program the TMS320E25 using the 28-pin pinout of the TMS27C64. The pin nomenclature table provides a description of the TMS27C64 pins. The code to be programmed into the device should be serial mode. The TMS320E25 uses 13 address lines to address the 4K-word memory in byte format.



Pin Nomenclature (TMS320E25)

SIGNALS	I/O	DEFINITION
A12 (MSB)–A0 (LSB)	I	On-chip EPROM programming address lines
CLIN	I	Clock oscillator input
$\overline{E}$	I	EPROM chip select
EPT	I	EPROM test mode select
$\overline{G}$	I	EPROM read/verify select
GND	I	Ground
$\overline{PGM}$	I	EPROM write/program select
Q8 (MSB)–Q1 (LSB)	I/O	Data lines for byte-wide programming of on-chip 8K bytes of EPROM
$\overline{RS}$	I	Reset for initializing the device
V_{CC}	I	5-V power supply
V_{PP}	I	12.5-V power supply

Figure 21. TMS320E25 EPROM Conversion to TMS27C64 EPROM Pinout

Table 4 shows the programming levels required for programming, verifying and reading the EPROM cell. The paragraphs following the table describe the function of each programming level.

Table 4. TMS320E25 Programming Mode Levels

SIGNAL NAME†	TMS320E25 PIN	TMS27C64 PIN	PROGRAM	PROGRAM VERIFY	PROGRAM INHIBIT	READ	OUTPUT DISABLE
$\overline{E}$	22	20	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}
$\overline{G}$	42	22	V_{IH}	$\overline{PULSE}$	X	$\overline{PULSE}$	V_{IH}
$\overline{PGM}$	41	27	$\overline{PULSE}$	V_{IH}	X	V_{IH}	V_{IH}
V_{PP}	25	1	V_{PP}	V_{PP}	V_{PP}	V_{CC}	V_{CC}
V_{CC}	61,35	28	$V_{CC}+1$	$V_{CC}+1$	$V_{CC}+1$	V_{CC}	V_{CC}
V_{SS}	27,44,10	14	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
CLKIN	52	14	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
$\overline{RS}$	65	14	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
EPT	24	26	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
Q1-Q8	18-11	11-13,15-19	D_{IN}	Q_{OUT}	HI-Z	Q_{OUT}	HI-Z
A12-A10	40-38	2,23,21,	ADDR	ADDR	X	ADDR	X
A9-A7	37,36,34	24,25,3	ADDR	ADDR	X	ADDR	X
A6	33	4	ADDR	ADDR	X	ADDR	X
A5	32	5	ADDR	ADDR	X	ADDR	X
A4	31	6	ADDR	ADDR	X	ADDR	X
A3-A0	30-28,26	7-10	ADDR	ADDR	X	ADDR	X

† In accordance with TMS27C64.

LEGEND:

V_{IH} = TTL high level; V_{IL} = TTL low level; ADDR = byte address bit
V_{PP} = 12.5 V ± 0.5 V; V_{CC} = 5 ± 0.25 V; X = don't care
$\overline{PULSE}$ = low-going TTL level pulse; D_{IN} = byte to be programmed at ADDR
Q_{OUT} = byte stored at ADDR; RBIT = ROM protect bit.

erasure

Before programming, the device is erased by exposing the chip through the transparent lid to high-intensity ultraviolet light (wavelength 2537 Å). The recommended minimum exposure dose (UV-intensity × exposure-time) is 15 W•s/cm^2. A typical 12 mW/cm^2, filterless UV lamp will erase the device in 21 minutes. The lamp should be located approximately 2.5 cm above the chip during erasure. After erasure, all bits are in the high state. Note that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS320E25, the window should be covered with an opaque label.

fast programming

After erasure (all memory bits in the cell are logic one), logic zeroes are programmed into the desired locations. The fast programming algorithm, shown in Figure 22, is normally used to program the entire EPROM contents, although individual locations may be programmed separately. A programmed logic zero can be erased only by ultraviolet light. Data is presented in parallel (eight bits) on pins Q8-Q1. Once addresses and data are stable, $\overline{PGM}$ is pulsed. The programming mode is achieved when V_{PP} = 12.5 V, $\overline{PGM}$ = V_{IL}, V_{CC} = 6 V, $\overline{G}$ = V_{IH}, and $\overline{E}$ = V_{IL} More than one TMS320E25 can be programmed when the devices are connected in parallel. Locations can be programmed in any order.

Programming uses two types of programming pulses: prime and final. The length of the prime pulse is 1 ms. After each prime pulse, the byte being programmed is verified. If correct data is read, the final programming pulse is applied; if correct data is not read, an additional 1-ms prime pulse is applied up to a maximum of 15 times. The final programming pulse is 4 ms times the number of prime programming pulses applied. This sequence of programming and verification is performed at V_{CC} = 6 V, and V_{PP} = 12.5 V. When the full fast programming routine is complete, all bits are verified with V_{CC} = V_{PP} = 5 V.

program verify

Programmed bits may be verified with V_{PP} = 12.5 V when $\overline{G} = V_{IL}$, $\overline{E} = V_{IL}$, and $\overline{PGM} = V_{IH}$. Figure 22 shows the timing for the program and verify operation.

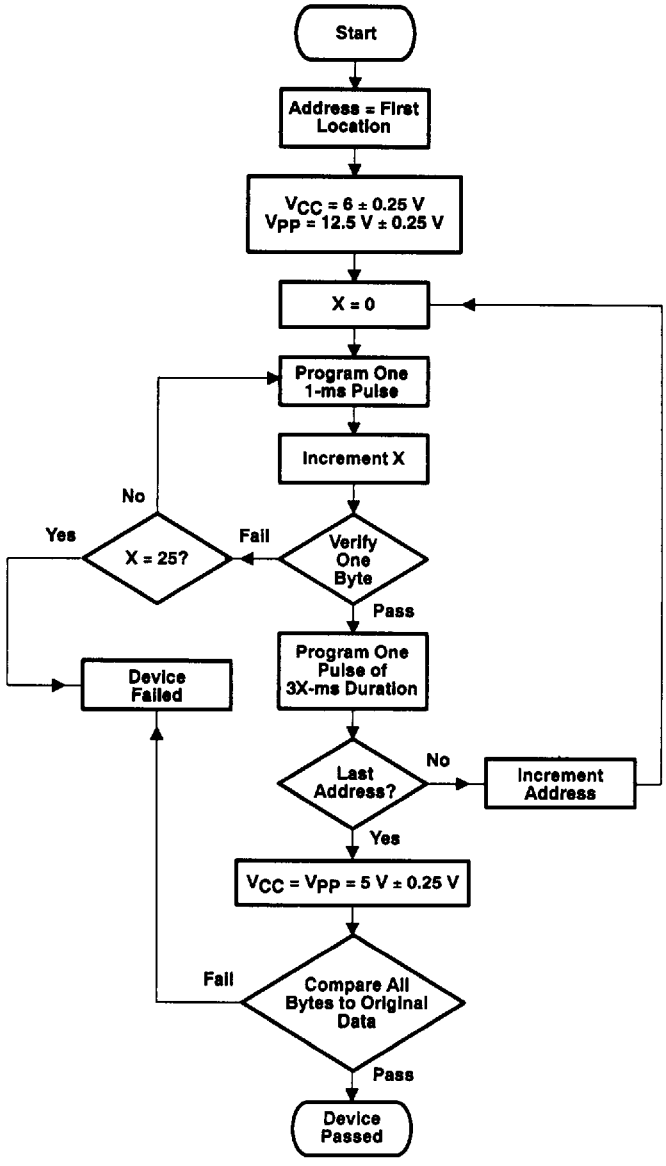


Figure 22. Fast Programming Flowchart

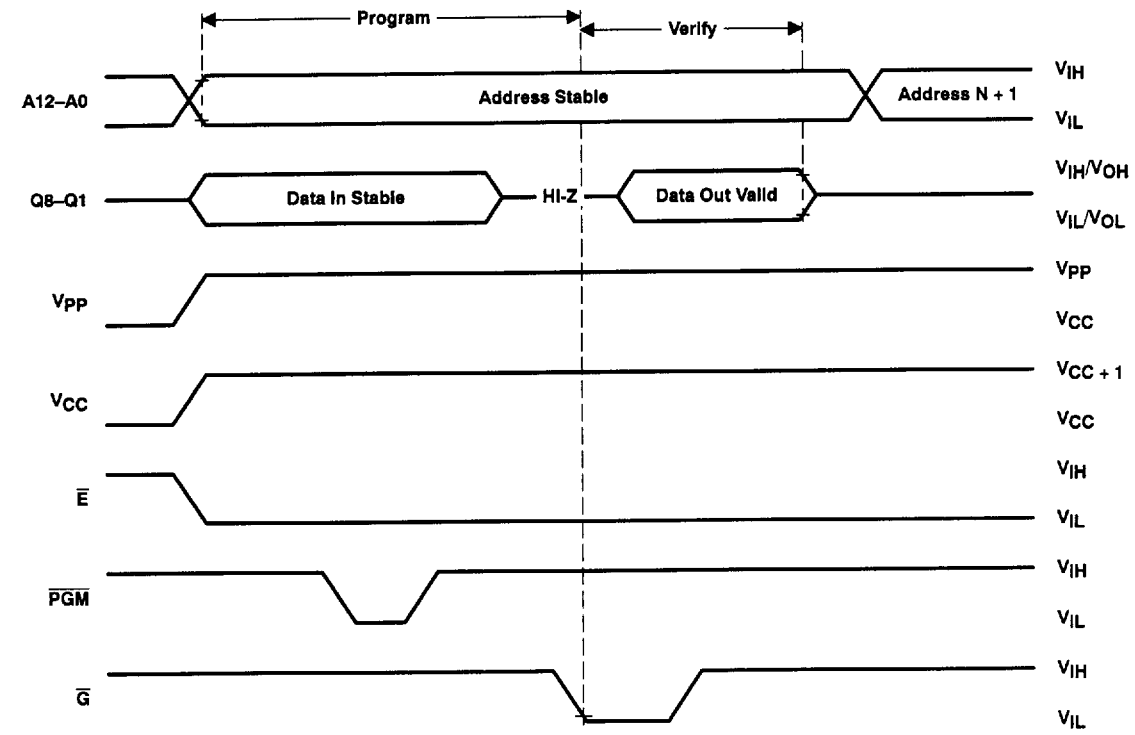


Figure 23. Fast Programming Timing

program inhibit

Programming may be inhibited by maintaining a high level input on the $\overline{E}$ pin or $\overline{PGM}$ pin.

read

The EPROM contents may be read independent of the programming cycle, provided the RBIT (ROM protect bit) has not been programmed. The read is accomplished by setting $\overline{E}$ to zero and pulsing $\overline{G}$ low. The contents of the EPROM location selected by the value on the address inputs appear on Q8-Q1.

output disable

During the EPROM programming process, the EPROM data outputs may be disabled, if desired, by establishing the output disable state. This state is selected by setting the $\overline{G}$ and $\overline{PGM}$ pins high. While output disable is selected, Q8-Q1 are placed in the high-impedance state.

ROM protection and verification

This section describes the code protection feature included in the EPROM cell, which protects code against copyright violations. Table 6 shows the programming levels required for protecting and verifying the EPROM. The paragraphs following the table describe the protect and verify functions.

Table 5. TMS320E25 Protect and Verify EPROM Mode Levels

SIGNAL†	TMS320E25 PIN	TMS27C64 PIN	ROM PROTECT	PROTECT VERIFY
$\overline{E}$	22	20	V_{IH}	V_{IL}
$\overline{G}$	42	22	V_{IH}	V_{IL}
$\overline{PGM}$	41	27	V_{IH}	V_{IH}
V_{PP}	25	1	V_{PP}	V_{CC}
V_{CC}	61,35	28	V_{CC} + 1	V_{CC}
V_{SS}	10, 27, 44	14	V_{SS}	V_{SS}
CLKIN	52	14	V_{SS}	V_{SS}
$\overline{RS}$	65	14	V_{SS}	V_{SS}
EPT	24	26	V_{PP}	V_{PP}
Q8-Q1	18-11	11-13, 15-19	Q8 = $\overline{PULSE}$	Q8 = RBIT
A12-A10	40-38	2, 23, 21,	X	X
A9-A7	37, 36, 34	24, 25, 3	X	X
A6	33	4	X	V_{IL}
A5	32	5	X	X
A4	31	6	V_{IH}	X
A3-A0	30-28, 26	7-10	X	X

† In accordance with TMS27C64.

LEGEND:

V_{IH} = TTL high level; V_{IL} = TTL low level; V_{CC} = 5 V ± 0.25 V

V_{PP} = 12.5 V ± 0.5 V; X = don't care

$\overline{PULSE}$ = low-going TTL level pulse; RBIT = ROM protect bit.

EPROM protect

The EPROM protect facility is used to completely disable reading of the EPROM contents to guarantee security of proprietary algorithms. This facility is implemented through a unique EPROM cell called the RBIT (EPROM protect bit) cell. Once the contents to be protected are programmed into the EPROM, the RBIT is programmed, disabling access to the EPROM contents and disabling the microprocessor mode on the device. Once programmed, the RBIT can be cleared only by erasing the entire EPROM array with ultraviolet light, thereby maintaining security of the propietary algorithm. Programming the RBIT is accomplished using the EPROM protect cycle, which consists of setting the $\overline{E}$, $\overline{G}$, $\overline{PGM}$, and A4 pins high, V_{PP} and EPT to 2.5 V ± 0.5 V, and pulsing Q8 low. The complete sequence of operations involved in programming the RBIT is shown in the flowchart of Figure 24. The required setups in the figure are detailed in Table 5.

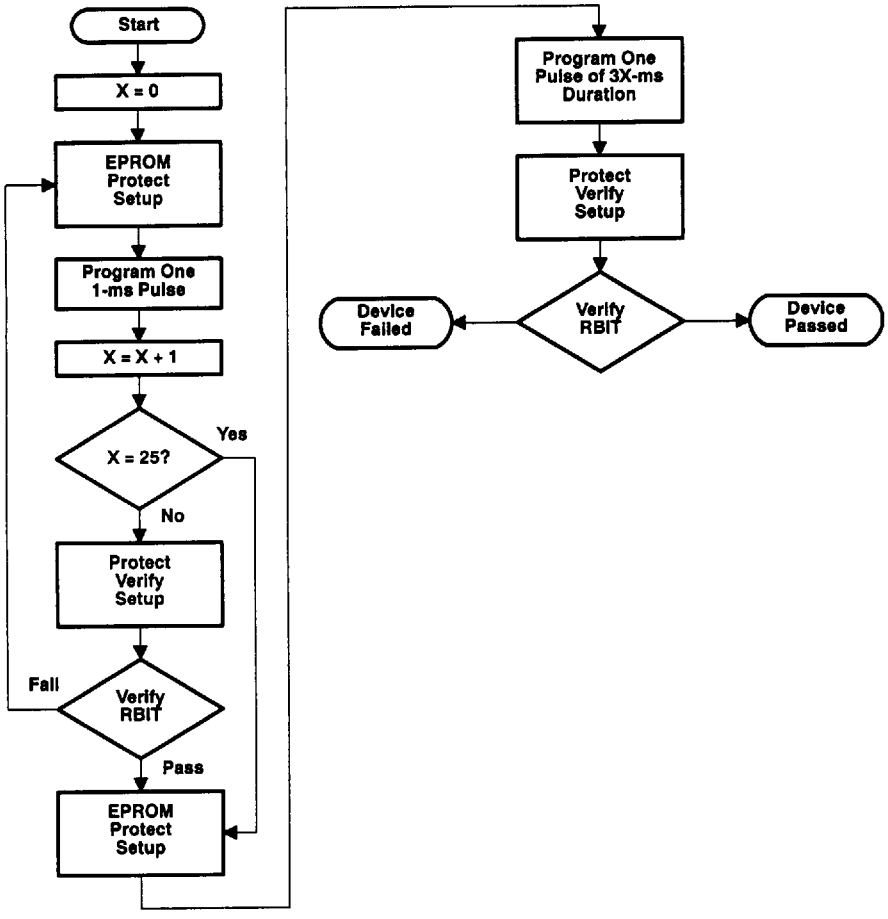


Figure 24. EPROM Protect Flowchart

protect verify

Protect verify is used following the EPROM protect to verify correct programming of the RBIT (see Figure 24). When using protect verify, Q8 outputs the state of the RBIT. When RBIT = 1, the EPROM is unprotected; when RBIT = 0, the EPROM is protected. The EPROM protect and verify timings are shown in Figure 25.

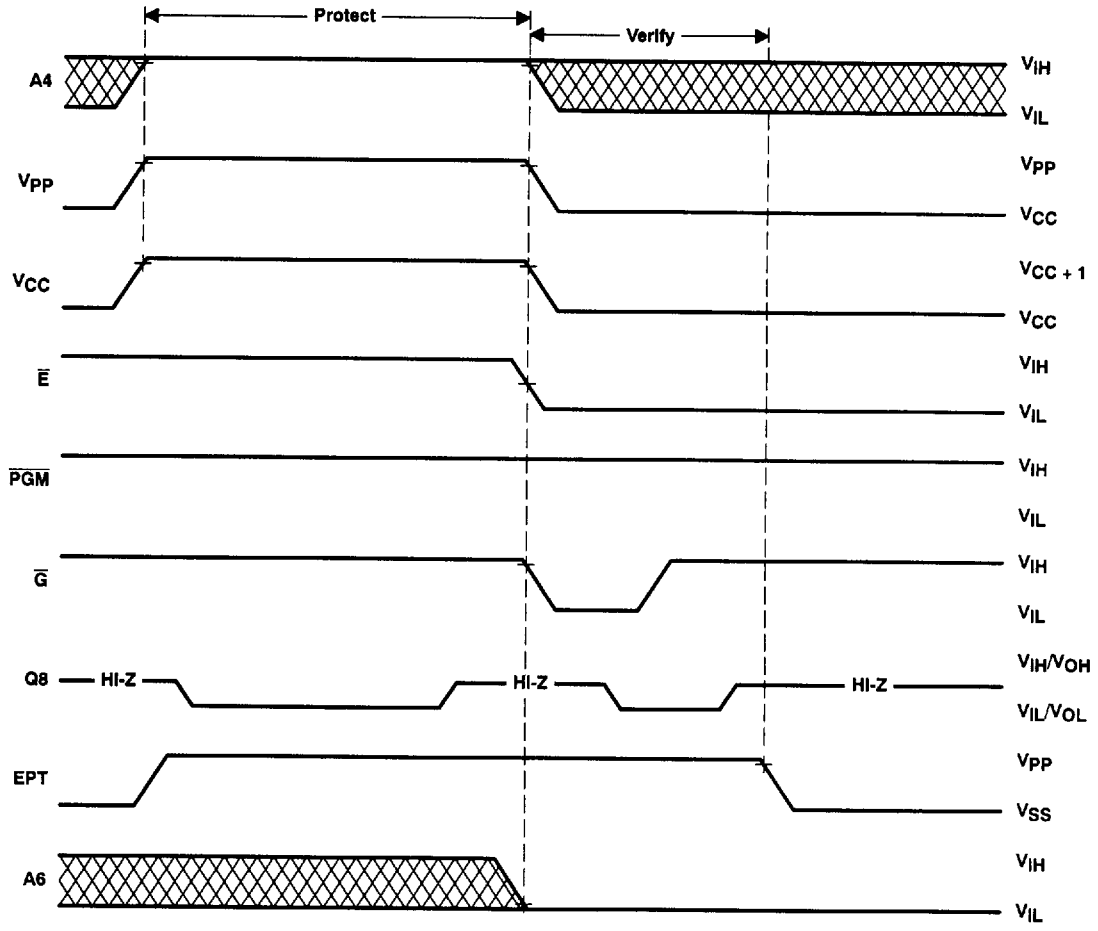


Figure 25. EPROM Protect Timing