

ADS5545

SLWS180-SEPTEMBER 2005

14-BITS, 170 MSPS ADC WITH LVDS/CMOS OUTPUTS

FEATURES

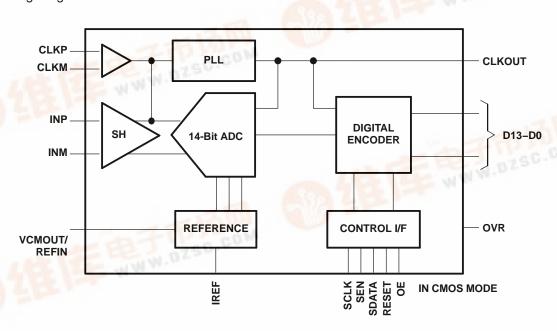
- Maximum Sample Rate: 170 MSPS
- 14-Bit Resolution
- No Missing Codes
- Power Dissipation
 - Core Power: 1 W
 - Total Power: 1.22 W
- Internal Sample and Hold
- 73.5-dBFS SNR at 70-MHz IF
- 85-dBc SFDR at 70-MHz IF
- Parallel CMOS and LVDS Output Options
- Internal Reference, External Reference Support
- 3.3-V Analog and Digital Supply
- 48-Pin QFN Package (7 mm × 7 mm)

APPLICATIONS

- Wireless Communication
- Software Defined Radio
- Power Amplifier Linearization
- 802.16d/e
- Test and Measurement Instrumentation
- High Definition Video
- Medical Imaging
- Radar Systems

DESCRIPTION

The ADS5545 is a high performance 14-bit 170-MSPS ADC. Using an internal sample and hold and low jitter clock buffer this ADC supports high SNR and high SFDR at high IF. With programmable options for parallel CMOS and LVDS outputs, this device is available in a compact 48-pin QFN package. The device provides internal references or can optionally be driven with an external reference. The device is specified over a -40°C to 85°C operating range.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



PACKAG/ORDERING INFORMATION(1)

PRODUCT	PACKAGE- LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS5545	48-QFN	RGZ	–40°C to 85°C	ADS5545IRGZ		

⁽¹⁾ $\theta_{JA} = TBD$, $\theta_{JC} = TBD$

ABSOLUTE MAXIMUM RATINGS(1)

		VALUE	UNIT
AVDD	Supply voltage range	-0.3 V to 3.9	V
DRVDD	Supply voltage range	-0.3 V to 3.9	V
	Voltage between AGND and DRGND	-0.3 to 0.3	V
	Voltage between AVDD to DRVDD	-0.3 to 3.3	V
CM	Voltage applied to external pin	-0.3 to 2	V
	Voltage applied to analog input pins	-0.3 V to minimum (3.6, AVDD + 0.3 V)	V
T _A	Operating free-air temperature range	-40 to 85	°C
T _J	Operating junction temperature range	125	°C
T _{stg}	Storage temperature range	-65 to 150	°C
	Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds	220	°C

⁽¹⁾ Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
SUPPLIE	S AND REFERENCES				
AVDD	Analog supply voltage	3	3.3	3.6	V
DRVDD	Digital supply voltage	3	3.3	3.6	V
CLOCK II	NPUT				
	Input clock sample rate	1		170	MSPS
	Input clock amplitude, differential				Vpp
	Input clock duty cycle		50%		
	Operating free-air temperature	-40		85	°C

ELECTRICAL CHARACTERISTICS

Typical values at 25°C, min, max values are across the full temperature range $T_{MIN} = -40$ °C to $T_{MAX} = 85$ °C, AVDD = DRVDD = 3.3 V, sampling rate = 170 MSPS, 50% clock duty cycle, -1 dBFS differential analog input, internal reference mode, LVDS data output (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT			
DC AC	DC ACCURACY								
	Resolution			14		bits			
	No missing codes			Assured					
DNL	Differential non-linearity		-0.9	0.5	TBD	LSB			
INL	Integral non-linearity			±3		LSB			
	Offset error			±10		mV			
	Offset temperature coefficient			TBD		ppm/°C			
	Gain error			±1		%FS			
	Gain temperature coefficient			TBD		Δ/°C			



ELECTRICAL CHARACTERISTICS (continued)

Typical values at 25°C, min, max values are across the full temperature range $T_{MIN} = -40$ °C to $T_{MAX} = 85$ °C, AVDD = DRVDD = 3.3 V, sampling rate = 170 MSPS, 50% clock duty cycle, -1 dBFS differential analog input, internal reference mode, LVDS data output (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN TYP	MAX	UNIT
POWER :	SUPPLY				
ICC	Total supply current	F _{IN} = TBD	369		mA
IAVDD	Analog supply current	F _{IN} = TBD	315		mA
IDRVDD	Digital aupply aurrent	LVDS mode, F _{IN} = TBD, C _L = 5 pF	54		mA
טטעאטו	Digital supply current	CMOS mode, $F_{IN} = TBD$, $C_L = 5 pF$	70		mA
	Total power dissipation	LVDS mode, F _{IN} = TBD	1.22		W
	Power down dissipation	Clock running	TBD		mW
REFERE	NCE VOLTAGES				
VREFB	Reference bottom		0.5		V
VREFT	Reference top		2.5		V
VCM	Common mode voltage (internal)		1.5		V
	VCM output current		±4		mA
ANALOG	INPUT				
	Differential input capacitance		7		pF
	Analog input common mode range		VCM ± 0.1		V
	Differential input voltage range		2		Vpp
	Analog input bandwidth	-3 dB, source impedance 50 Ω	400		MHz
DYNAMIC	C AC CHARACTERISTICS				
		F _{IN} = 10 MHz	90		
SFDR	Spurious free dynamic range	F _{IN} = 70 MHz	85		dBc
		F _{IN} = 150 MHz	84		
		F _{IN} = 10 MHz	74		
SNR	Signal-to-noise ratio	F _{IN} = 70 MHz	73.5		dBFS
		F _{IN} = 150 MHz	72		



DIGITAL CHARACTERISTICS

The dc specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level 0 or 1 AVDD = DRVDD = 3.3 V, I_O = 3.5 mA, R_L = 100 Ω . (1)

All LVDS and CMOS specifications are characterized, but not tested at production.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS				,	
High-level input voltage		2.4			V
Low-level input voltage				0.8	V
High-level input current			10		μΑ
Low-level input current			10		μΑ
Input capacitance			4		pF
DIGITAL OUTPUTS - CMOS MODE					
High-level output voltage			3.3		V
Low-level output voltage			0		V
Output capacitance	Output capacitance inside the device, from either output to ground		4		pF
DIGITAL OUTPUTS – LVDS MODE		<u> </u>		,	
High-level output voltage			1375		mV
Low-level output voltage			1025		mV
Output differential voltage, V _{OD}			350		mV
V _{OS} Output offset voltage ⁽¹⁾	Common-mode voltage of OUTP and OUTM		1200		mV
Output capacitance	Output capacitance inside the device, from either output to ground		4		pF
Change in $ V_{OD} $, $ \Delta V_{OD} $			25		mV
Change in $ V_{OS} $, $ \Delta V_{OS} $			25		mV

(1) I_O refers to the LVDS buffer current setting, R_L is the differential load resistance between the LVDS output pair.

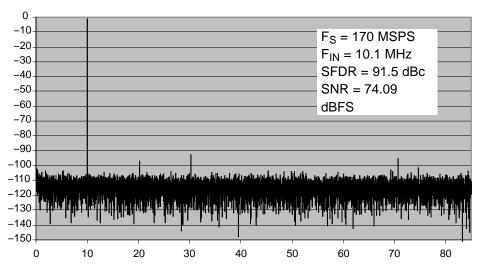


Figure 1. ADS5545 FFT Plot at 170 MSPS and 10-MHz Input



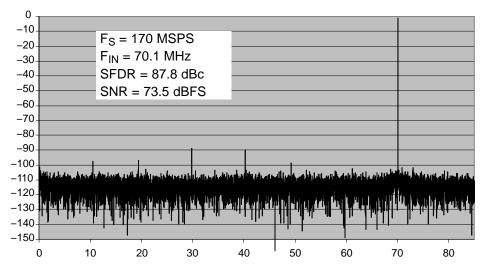


Figure 2. ADS5545 FFT Plot at 170 MSPS and 70-MHz Input



PACKAGE OPTION ADDENDUM

21-Sep-2005

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing		kage Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
ADS5545IRGZ	PREVIEW	QFN	RGZ	48 2	250	TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in

a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

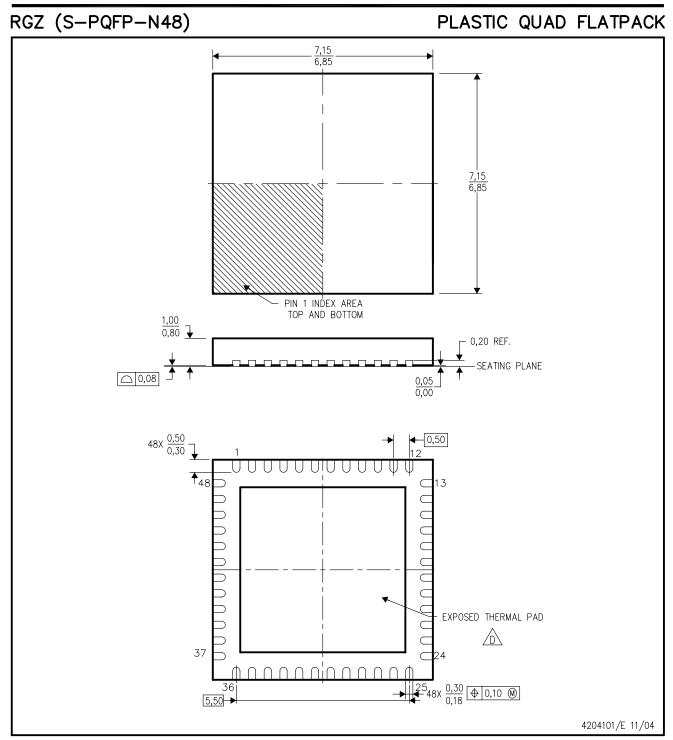
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

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(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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- NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
 - B. This drawing is subject to change without notice.
 - C. Quad Flatpack, No-leads (QFN) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.

 See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
 - E. Falls within JEDEC MO-220.



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