STRUCTURE	Silicon Monolithic integrated circuit
PRODUCTS	Input switching interface LSI for the DVD recorder
TYPE	BH7625KS2
PACKAGE	Figure-1 SQFP−T52 (Plastic Mold)
BLOCK DIAGRAM	Figure-2

Features
1) Built-in-5 input Video switch, Y switch and 5-input C switch
2) Input terminal of the S2 standard suitability
3) I^2C BUS control (High impedance when power source off)
4) 0/3dB switch AMP built-in (CVBS OUT, C OUT)
5) 0/6dB switch AMP built-in (Y/CVBS OUT)
6) Synchronization isolation circuit built-in (2 circuits SYNC OUT, V SYNC OUT)
7) Synchronization detection circuit built-in (2 circuits)
8) 3LPF circuits built-in (4 order + TRAP)

Absolute maximum ratings (Ta=25℃)

Item	Symbol	Rating	Unit
Power supply voltage	V	7.0	V
Power dissipation	Pd	※1 1300	mW
Operating temperature range	Topr	−25 ~ +75	℃
Storage temperature range	Tstg	−55 ~ +125	℃

※1 When absolute temperature exceeds Ta=25℃, the rated value is reduced at unit of 14mW/℃.

Operation range (Ta=25℃)

Item	Symbol	Rating	Unit
Supply Voltage	VCC1,VCC2, VCC3,DVCC, SYNC,VCC,VCC	4.5~5.5	V

※ This product is not designed for protection against radioactive rays.
※ VCC1、VCC2、VCC3、DVCC、SYNC VCC、VCC should use the same power source.
※ Improper operation will result if the input and/ or output terminal is connected either to the supply

Application example
The application circuit is recommended for use. Make sure to confirm the adequacy of the characteristics.
When using the circuit with changes to the external circuit constants, make sure to leave an adequate margin for external components including static and transitional characteristics as well as dispersion of the IC.
Note that ROHM cannot provide adequate confirmation of patents.

The product described in this specification is designed to be used with ordinary electronic equipment or devices (such as audio-visual equipment, office-automatic equipment, communications devices, electrical appliance, and electronic toys). Should you intend to use this product with equipment or devices which require an extremely high level of reliability and the malfunction of which would directly endanger human life (such as medical instruments, transportation equipment, aerospace machinery, nuclear-reactor controllers, fuel controllers and other safety devices), please be sure to consult with our sales representative in advance.

ROHM assumes no responsibility for use of any circuits described herein, conveys no license under any patent or other right, and makes no representations that the circuits are free from patent infringement.

■ Electrical characteristics （Unless otherwise specified, VCC=5.0V, Ta=25℃）

Item	Symbol	Limit			Unit	Conditions
		MIN.	TYP.	MAX.		
<All Circuits>						
VCC Circuit Current	I_{CC}	71	95	128	mA	Normal Condition
VCC STBY Circuit Current	I_{CCST}	9.38	12.5	16.9	mA	Standby Condition
VCC PD Circuit Current	I_{CCPD}	—	0	10	μA	Power Down Condition
<SW Part>						
CVBS OUT Cb OUT Voltage Gain H	G_{V1H}	2.4	2.9	3.4	dB	Vin=1.0Vpp , f=100kHz, LPF OFF
CVBS OUT Cb OUT Voltage Gain L	G_{V1L}	−0.7	−0.2	0.3	dB	Vin=1.0Vpp , f=100kHz, LPF OFF
Y/CVBS OUT Cy OUT Voltage Gain H	G_{V2H}	5.5	6.0	6.5	dB	Vin=1.0Vpp , f=100kHz, LPF OFF
Y/CVBS OUT Cy OUT Voltage Gain L	G_{V2L}	−0.7	−0.2	0.3	dB	Vin=1.0Vpp , f=100kHz, LPF OFF
C OUT Cr OUT Voltage Gain H	G_{V3H}	2.4	2.9	3.4	dB	Vin=1.0Vpp , f=100kHz, LPF OFF
C OUT Cr OUT Voltage Gain L	G_{V3L}	−0.7	−0.2	0.3	dB	Vin=1.0Vpp , f=100kHz, LPF OFF
CVBS OUT Cb OUT Voltage Gain H	G_{V4H}	2.2	2.7	3.2	dB	Vin=1.0Vpp , f=100kHz, LPF ON
CVBS OUT Cb OUT Voltage Gain L	G_{V4L}	−0.9	−0.4	0.1	dB	Vin=1.0Vpp , f=100kHz, LPF ON
Y/CVBS OUT Cy OUT Voltage Gain H	G_{V5H}	5.3	5.8	6.3	dB	Vin=1.0Vpp , f=100kHz, LPF ON
Y/CVBS OUT Cy OUT Voltage Gain L	G_{V5L}	−0.9	−0.4	0.1	dB	Vin=1.0Vpp , f=100kHz, LPF ON
C OUT Cr OUT Voltage Gain H	G_{V6H}	2.2	2.7	3.2	dB	Vin=1.0Vpp , f=100kHz, LPF ON
C OUT Cr OUT Voltage Gain L	G_{V6L}	−0.9	−0.4	0.1	dB	Vin=1.0Vpp , f=100kHz, LPF ON
CVBS OUT Cb OUT Maximum Output Level	V_{OM1}	2.6	3.0	—	Vpp	f=100kHz(10kHz), THD=1%
Y/CVBS OUT Cy OUT Maximum Output Level	V_{OM2}	2.6	3.0	—	Vpp	f=100kHz(10kHz), THD=1%
C OUT Cr OUT Maximum Output Level	V_{OM3}	2.6	3.0	—	Vpp	f=100kHz(10kHz), THD=1%
<SW Part>						
CVBS OUT Cb OUT Frequency Characteristics 1	G_{F11}	−1.5	−0.5	0.5	dB	Vin=1.0Vpp Gain=3dB Vin=2.0Vpp Gain=0dB f=6.75MHz/100kHz (LPF ON)
CVBS OUT Cb OUT Frequency Characteristics 2	G_{F12}	—	−38	−27	dB	Vin=1.0Vpp Gain=3dB Vin=2.0Vpp Gain=0dB f=27MHz/100kHz (LPF ON)
CVBS OUT Cb OUT Frequency Characteristics 3	G_{F13}	−1.0	0	1.0	dB	Vin=1.0Vpp Gain=3dB Vin=2.0Vpp Gain=0dB f=7MHz/100kHz (Through)
Y/CVBS OUT Cy OUT Frequency Characteristics 1	G_{F21}	−1.5	−0.5	0.5	dB	Vin=1.0Vpp Gain=6dB Vin=2.0Vpp Gain=0dB f=6.75MHz/100kHz (LPF ON)
Y/CVBS OUT Cy OUT Frequency Characteristics 2	G_{F22}	—	−38	−27	dB	Vin=1.0Vpp Gain=6dB Vin=2.0Vpp Gain=0dB f=27MHz/100kHz (LPF ON)
Y/CVBS OUT Cy OUT Frequency Characteristics 3	G_{F23}	−1.0	0	1.0	dB	Vin=1.0Vpp Gain=6dB Vin=2.0Vpp Gain=0dB f=7MHz/100kHz (Through)
C OUT Cr OUT Frequency Characteristics 1	G_{F31}	−1.5	−0.5	0.5	dB	Vin=1.0Vpp Gain=3dB Vin=2.0Vpp Gain=0dB f=6.75MHz/100kHz (LPF ON)
C OUT Cr OUT Frequency Characteristics 2	G_{F32}	—	−38	−27	dB	Vin=1.0Vpp Gain=3dB Vin=2.0Vpp Gain=0dB f=27MHz/100kHz (LPF ON)
C OUT Cr OUT Frequency Characteristics 3	G_{F33}	−1.0	0	1.0	dB	Vin=1.0Vpp Gain=3dB Vin=2.0Vpp Gain=0dB f=7MHz/100kHz (Through)
C IN Input Impedance	Z_{CIN}	12.5	18.0	23.5	kΩ	
<SYNC DETECTOR Part>						
Min Synchronization Isolation Level	SL_{MIN}	—	0.08	0.12	Vpp	LPF Condition "000"
C、V SYNC、SYNC DET OUT Output Voltage H	V_{VCH}	Vcc- 0.5	Vcc - 0.1	Vcc	V	No Load
C、V SYNC、SYNC DET OUT Output Voltage L	V_{VCL}	—	0.1	0.5	V	No Load
<I2C-BUS Control>						
S1/S2 DET Detection Level H	DL_H	3.4	—	Vcc	V	16:9 Squeeze Signal
S1/S2 DET Detection Level M	DL_M	1.3	1.9	2.5	V	4:3 Letter Box Signal
S1/S2 DET Detection Level L	DL_L	0.0	—	0.7	V	4:3 Video Signal, No Signal

■Electrical Characteristics （Unless otherwise specified, Vcc=5.0V, Ta=25℃）

Item	Symbol	Limit			Unit	Conditions
		MIN.	TYP.	MAX.		
<SCL、SDA、ADR>						
Input Voltage H	V_{IHIIC}	2.0	—	Vcc	V	
Input Voltage L	V_{ILIIC}	0.0	—	1.0	V	
Input Bias Current (SCL、SDA)	I_{BIIC}	0	−1	−10	μA	
Input Impedance (ADR)	Z_{INADR}	65	100	135	kΩ	Pull Down Resistance
<PD>						
Input Voltage H	V_{IHPD}	2.0	—	Vcc	V	
Input Voltage L	V_{ILPD}	0.0	—	0.7	V	
Input Impedance	Z_{INPD}	65	100	135	kΩ	Pull Down Resistance
<PD>						
Input Voltage H	V_{IHPD}	2.0	—	Vcc	V	
Input Voltage L	V_{ILPD}	0.0	—	0.7	V	
Input Impedance	Z_{INPD}	65	100	135	kΩ	Pull Down Resistance

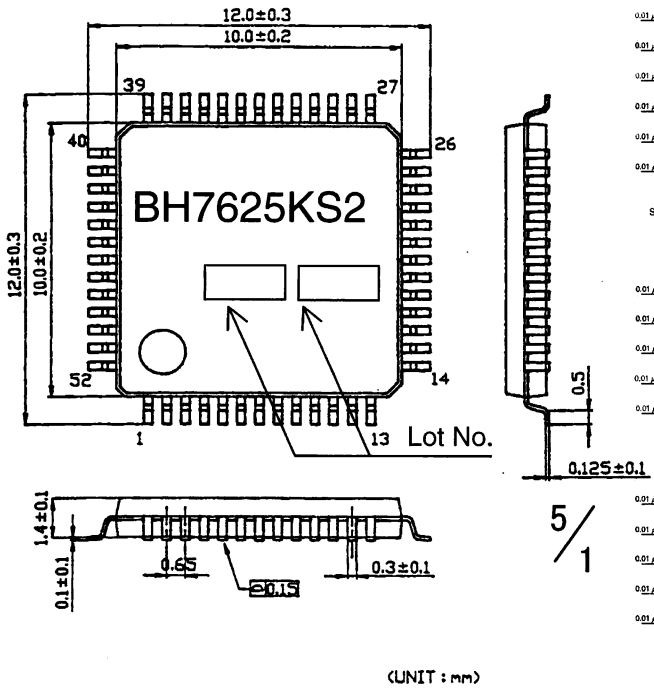

Figure - 1 PACKAGE
（S Q F P − T 5 2）

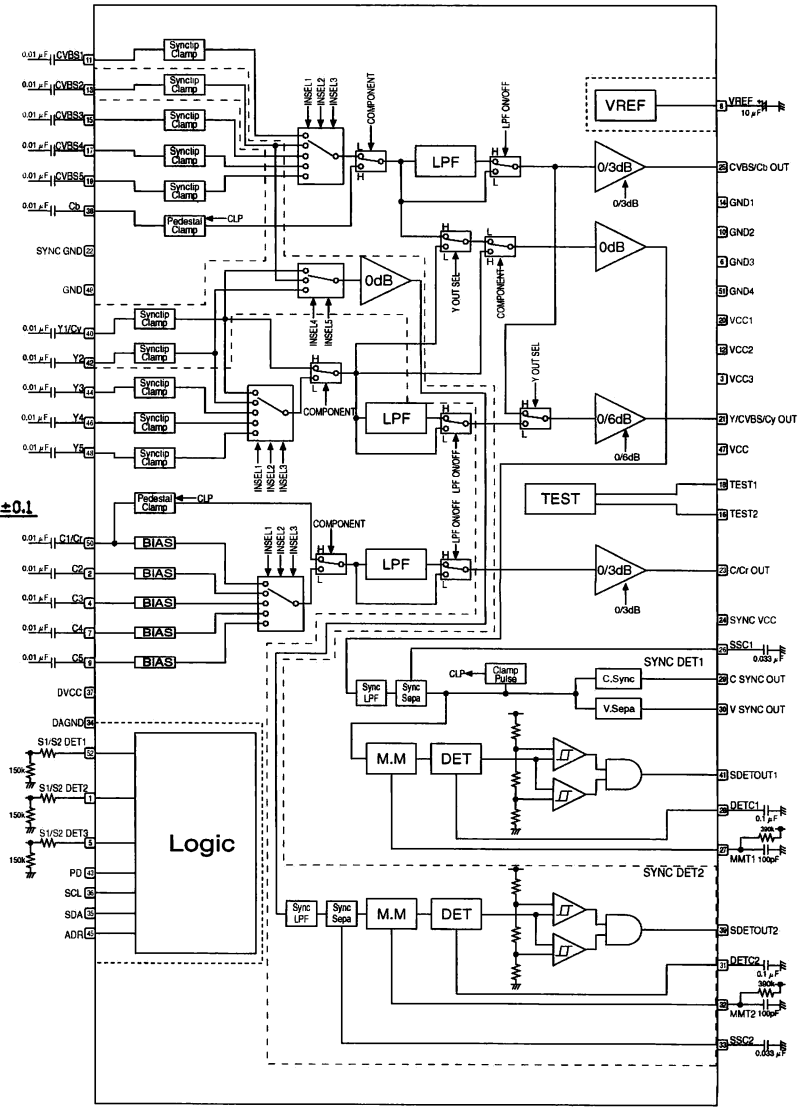

Figure - 2 . BLOCK Diagram

■PIN Assignment

PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME
1	S1_S2_DET2	14	GND1_2	27	MMT1	40	Y1_Cy
2	C2	15	CVBS3	28	DETC1	41	SDETOUT2
3	VCC3_1	16	TEST2	29	C_SYNC_OUT	42	Y2
4	C3	17	CVBS4	30	V_SYNC_OUT	43	PD
5	S1_S2_DET3	18	TEST1	31	DETC2	44	Y3
6	GND3_1	19	CVBS5	32	MMT2	45	ADR
7	C4	20	VCC1_2	33	SSC2	46	Y4
8	VREF	21	Y_CVBS_Cy_OUT	34	DAGND_1	47	VCC4_1
9	C5	22	SYNC_GND	35	SDA	48	Y5
10	GND2_1	23	C_Cr_OUT	36	SCL	49	GND4_1
11	CVBS1	24	SYNC_VCC	37	DVCC_1	50	C1_Cr
12	VCC2_1	25	CVBS_Cb_OUT	38	Cb	51	SYNC_GND
13	CVBS2	26	SSC1	39	SDETOUT1	52	S1_S2_DET1

■ Cautions on use

(1) Numbers and data in entries are representative design values and are not guaranteed values of items.

(2) Although we are confident in recommending the sample application circuits, carefully check their characteristics further when using them. When modifying externally attached component constants before use, determine them so that they have sufficient margins by taking into account variations in externally attached components and the Rohm LSI, not only for static characteristics but also including transient characteristics.

(3) Absolute maximum ratings

If applied voltage, operating temperature range, or other absolute maximum ratings are exceeded, the LSI may be damaged. Do not apply voltages or temperatures that exceed the absolute maximum ratings. If you think of a case in which absolute maximum ratings are exceeded, enforce fuses or other physical safety measures and investigate how not to apply the conditions under which absolute maximum ratings are exceeded to the LSI.

(4) GND potential

Make the GND pin voltage such that it is the lowest voltage even when operating below it. Actually confirm that the voltage of each pin does not become a lower voltage than the GND pin, including transient phenomena.

(5) Thermal design

Perform thermal design in which there are adequate margins by taking into account the allowable power dissipation in actual states of use.

(6) Shorts between pins and misinstallation

When mounting the LSI on a board, pay adequate attention to orientation and placement discrepancies of the LSI. If it is misinstalled and the power is turned on, the LSI may be damaged. It also may be damaged if it is shorted by a foreign substance coming between pins of the LSI or between a pin and power supply or a pin a GND.

(7) Operation in strong magnetic fields

Adequately evaluate use in a strong magnetic field, since there is a possibility of malfunction.

(8) Supply voltage of operation

Although basic circuit function is guaranteed within the limits of supply voltage (4.5V～5.5V) of operation.

(9) Please lay out outside parts nearest IC, and set lines from output amplifier short.

(10) Please lay out the coupling capacitor nearest IC and each pin.

(11) VCC for this IC should use the same power source. And impedance should connect as well as possible for each VCC pin, for each GND pin.

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As of 18th. April 2005