

HIGH-SPEED 1K x 8 DUAL-PORT STATIC RAM

IDT7130SA/LA IDT7140SA/LA

FEATURES

- · High-speed access
 - —Military: 25/35/55/100ns (max.)—Commercial: 25/35/55/100ns (max.)
 - -Commercial: 20ns 7130 in PLCC and TQFP
- Low-power operation
 - —IDT7130/IDT7140SA
 Active: 550mW (typ.)
 Standby: 5mW (typ.)
 —IDT7130/IDT7140LA
 - Active: 550mW (typ.)
 Standby: 1mW (typ.)
- MASTER IDT7130 easily expands data bus width to 16-or-more-bits using SLAVE IDT7140
- On-chip port arbitration logic (IDT7130 Only)
- BUSY output flag on IDT7130; BUSY input on IDT7140
- Interrupt flags for port-to-port communication
- Fully asynchronous operation from either port
- Battery backup operation—2V data retention (LA only)
- TTL-compatible, single 5V ±10% power supply
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing #5962-86875
- Industrial temperature range (-40°C to +85°C) is available, tested to military electrical specifications

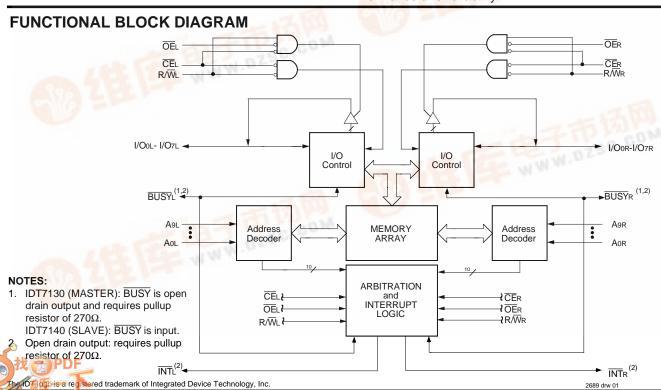
DESCRIPTION

The IDT7130/IDT7140 are high-speed 1K x 8 Dual-Port Static RAMs. The IDT7130 is designed to be used as a stand-alone 8-bit Dual-Port RAM or as a "MASTER" Dual-Port RAM together with the IDT7140 "SLAVE" Dual-Port in 16-bit-or-more word width systems. Using the IDT MASTER/SLAVE Dual-Port RAM approach in 16-or-more-bit memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

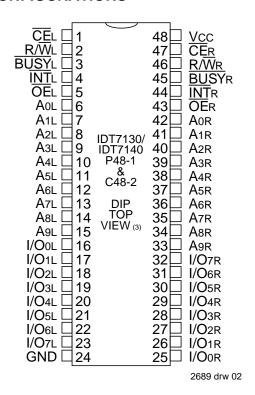
Both devices provide two independent ports with separate control, address, and I/O pins that permit independent asynchronous access for reads or writes to any location in memory. An automatic power down feature, controlled by \overline{CE} , permits the on chip circuitry of each port to enter a very low standby power mode.

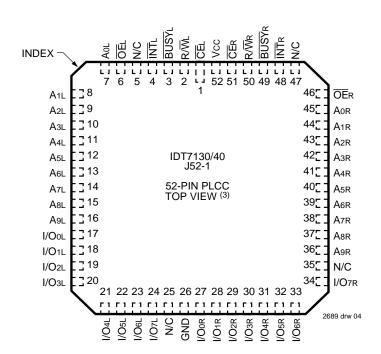
Fabricated using IDT's CMOS high-performance technology, these devices typically operate on only 550mW of power. Low-power (LA) versions offer battery backup data retention capability, with each Dual-Port typically consuming 200µW from a 2V battery.

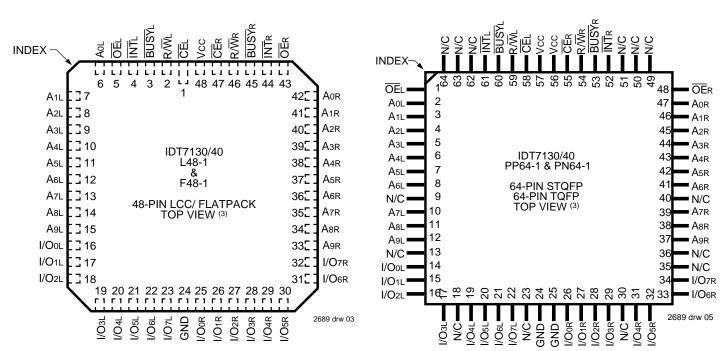
The IDT7130/IDT7140 devices are packaged in 48-pin sidebraze or plastic DIPs, LCCs, or flatpacks, 52-pin PLCC, and 64-pin TQFP and STQFP. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.



PIN CONFIGURATIONS (1,2)







- 1. All Vcc pins must be connected to the power supply.
- All GND pins must be connected to the ground supply.
- 3. This text does not indicate orientation of the actual part-marking.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
Та	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
Tstg	Storage Temperature	-55 to +125	-65 to +150	°C
Іоит	DC Output Current	50	50	mA

NOTES: 2689 tbl 01

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS
 may cause permanent damage to the device. This is a stress rating only
 and functional operation of the device at these or any other conditions
 above those indicated in the operational sections of the specification is not
 implied. Exposure to absolute maximum rating conditions for extended
 periods may affect reliability.
- 2. VTERM must not exceed Vcc + 0.5 for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of VTERM ≥ Vcc + 0.5V.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Тур.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2		6.0 ⁽²⁾	V
VIL	Input Low Voltage	$-0.5^{(1)}$	_	0.8	V

NOTES:

- 1. VIL (min.) \geq -1.5V for pulse width less than 10ns.
- 2. VTERM must not exceed Vcc + 0.5V.

2689 tbl 02

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Grade Temperature		Vcc
Military	−55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2689 tbl 03

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (VCc = $5.0V \pm 10\%$)

			7130	OSA	713	0LA	
			7140	OSA	714	0LA	
Symbol	Parameter	Test Conditions	Min.	Max.	Max.	Max.	Unit
I⊔	Input Leakage Current ⁽¹⁾	VCC = 5.5V, VIN = 0V to VCC	_	10	-	5	μА
llo	Output Leakage Current ⁽¹⁾	Vcc = 5.5V, \overline{CE} = ViH, Vout = 0V to Vcc	_	10	l	5	μА
Vol	Output Low Voltage (I/O0-I/O7)	IOL = 4mA	_	0.4		0.4	V
Vol	Open Drain Output Low Voltage (BUSY, INT)	IoL = 16mA	_	0.5	1	0.5	V
Vон	Output High Voltage	Iон = -4mA	2.4	_	2.4	_	V

NOTE:

2689 tbl 04

CAPACITANCE⁽¹⁾

 $(TA = +25^{\circ}C, f = 1.0MHz) TQFP ONLY^{(3)}$

Symbol	Parameter	Conditions ⁽²⁾	Max.	Unit
CIN	Input Capacitance	VIN = 3dV	9	рF
Соит	Output Capacitance	VIN = 3dV	10	pF

NOTES:

2689 tbl 05

- This parameter is determined by device characterization but is not production tested.
- 3dv references the interpolated capacitance when the input and output signals switch from 0V to 3V or from 3V to 0V.
- 3. 11pF max. for other packages.

^{1.} At Vcc ≤ 2.0V leakages are undefined.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE^(1,6) (VCC = $5.0V \pm 10\%$)

								7130X25 ⁽³⁾ 7140X25 ⁽³⁾		7130X35 7140X35		7130X55 7140X55		5 7140X100		
Symbol	Parameter	Test Conditions	Vers	ion	Тур.	Max.	Тур.	Max.	Тур.	Max.	Тур.	Мах.	Тур.	Max.	Unit	
Icc	Dynamic Operating Current (Both Ports	$\overline{\text{CE}}$ L and $\overline{\text{CE}}$ R = VIL, Outputs open,		SA LA	_	_	110 110	280 220	110 110	230 170	110	190 140	110 110	190 140	mA	
	Active)	$f = fMAX^{(4)}$	COM'L.	SA LA	110 110	250 200	110 110	220 170	110 110	165 120		155 110	110 110	155 110		
ISB1	Standby Current (Both Ports - TTL	$\overline{\text{CE}}\text{L}$ and $\overline{\text{CE}}\text{R} = \text{ViH}$, $f = \text{fMAX}^{(4)}$		SA LA	_	_	30 30	80 60	25 25	80 60	20 20	65 45	20 20	65 45	mA	
	Level Inputs)		COM'L.	SA LA	30 30	65 45	30 30	65 45	25 25	65 45	20 20	65 35	20 20	55 35		
ISB2	Standby Current (One Port - TTL	\overline{CE} "A" = VIL and \overline{CE} "B" = VIH $^{(7)}$	MIL.	SA LA	_ _	_	65 65	160 125	50 50	150 115	40 40	125 90	40 40	125 90	mA	
	Level Inputs)	Active Port Outputs Open, $f = fMAX^{(4)}$	COM'L.	SA LA	65 65	165 125	65 65	150 115	50 50	125 90	40 40	110 75	40 40	110 75		
ISB3	Full Standby Current (Both Ports - All	CEL and CER ≥ Vcc -0.2V,	MIL.	SA LA	_	_	1.0 0.2	30 10	1.0 0.2	30 10	1.0 0.2	30 10	1.0 0.2	30 10	mA	
	CMOS Level Inputs	$VIN \ge VCC -0.2V \text{ or}$ $VIN \le 0.2V, f = 0^{(5)}$	COM'L.	SA LA	1.0 0.2	15 5	1.0 0.2	15 5	1.0 0.2	15 4	1.0 0.2	15 4	1.0 0.2	15 4		
ISB4	Full Standby Current (One Port - All	\overline{CE} "A" $\leq 0.2V$ and \overline{CE} "B" $\geq VCC -0.2V^{(7)}$	MIL.	SA LA	_	_	60 60	155 115	45 45	145 105	40 40	110 85	40 40	110 80	mA	
	CMOS Level Inputs)	$\begin{split} &\text{VIN} \geq \text{VCC -0.2V or} \\ &\text{VIN} \leq 0.2\text{V}, \\ &\text{Active Port Outputs} \\ &\text{Open, } f = \text{fMAX}^{(4)} \end{split}$	COM'L.	SA LA	60 60	155 115	60 60	145 105	45 45	110 85	40 40	100 70	40 40	95 70		

NOTES:

- 'X' in part numbers indicates power rating (SA or LA).
- 2. Com'l Only, 0°C to +70°C temperature range. PLCC and TQFP packages.
- 3. Not available in DIP packages.
- 4. At f = fMax, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/tRc, and using "AC TEST CONDITIONS" of input levels of GND to 3V.
- 5. f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.
- 6. Vcc = 5V, $TA=+25^{\circ}C$ for Typ and is not production tested. Vcc DC = 100 mA (Typ.)
- 7. Port "A" may be either left or right port. Port "B" is opposite from port "A".

DATA RETENTION CHARACTERISTICS (LA Version Only)

Parameter	Test Conditions	Min.	0LA/IDT714 Typ. ⁽¹⁾	Unit		
Vcc for Data Retention			2.0	_	_	V
Data Retention Current		Mil.	_	100	4000	μΑ
	Vcc = 2.0V, CE ≥ Vcc -0.2V	Com'l.	_	100	1500	μΑ
Chip Deselect to Data	\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\		0	_	_	ns
Retention Time	$ VIN \ge VCC - 0.2V \text{ Of } VIN \le 0.2V$					
Operation Recovery			tRC ⁽²⁾	_	_	ns
Time						
	Vcc for Data Retention Data Retention Current Chip Deselect to Data Retention Time Operation Recovery	Vcc for Data RetentionData Retention CurrentVcc = $2.0V$, $\overline{CE} \ge Vcc -0.2V$ Chip Deselect to Data Retention TimeOperation Recovery $Vcc = 2.0V$, $\overline{CE} \ge Vcc -0.2V$ $VIN \ge Vcc -0.2V$ or $VIN \le 0.2V$		$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$

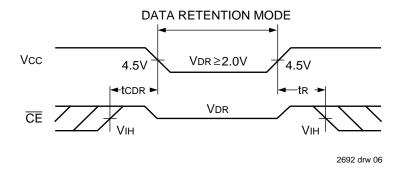
NOTES:

- 1. Vcc = 2V, TA = +25°C, and is not production tested.
- 2. trc = Read Cycle Time
- 3. This parameter is guaranteed but not production tested.

2689 tbl 07

2689 tbl 06

DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels Input Rise/Fall Times Input Timing Reference Levels Output Reference Levels Output Load	GND to 3.0V 5ns 1.5V 1.5V Figures 1, 2, and 3	
1 .	1	

2689 tbl 08

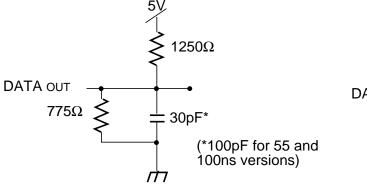


Figure 1. Output Test Load

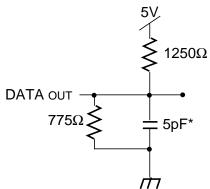


Figure 2. Output Test Load (for thz, tLz, twz, and tow)
* including scope and jig

2689 drw 07

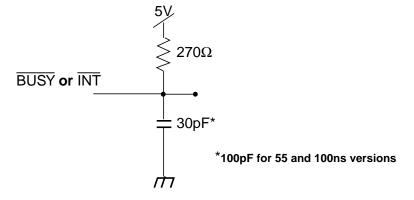


Figure 3. BUSY and INT AC Output Test Load

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE⁽³⁾

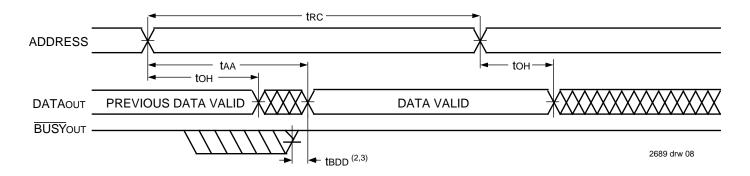
				7130X25 ⁽⁵⁾ 7140X25 ⁽⁵⁾				7130X55 7140X55		7130X100 7140X100		
Symbol	Parameter	Min.	Max.		Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cy	cle											
trc	Read Cycle Time	20	_	25	_	35	_	55	_	100	_	ns
tAA	Address Access Time	_	20		25	_	35	_	55		100	ns
tACE	Chip Enable Access Time	_	20	_	25		35	_	55		100	ns
tAOE	Output Enable Access Time		11	_	12	_	20		25	_	40	ns
tон	Output Hold From Address Change	3	_	3	_	3	_	3	_	10	_	ns
tLZ	Output Low-Z Time ^(1,4)	0	_	0	_	0	_	5	_	5	_	ns
tHZ	Output High-Z Time ^(1,4)	_	10		10	_	15	_	25		40	ns
tpu	Chip Enable to Power Up Time ⁽⁴⁾	0	_	0	_	0	_	0	_	0	_	ns
tPD	Chip Disable to Power Down Time ⁽⁴⁾	_	20		25	_	35	_	50		50	ns

NOTES:

2689 tbl 09

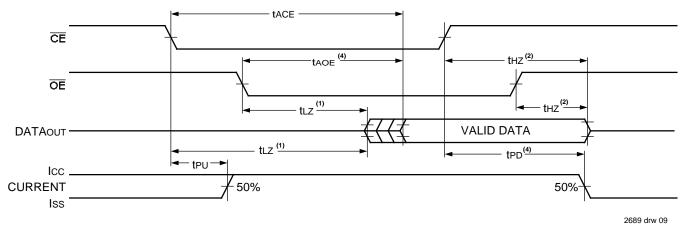
- 1. Transition is measured ±500mV from Low or High-impedance voltage Output Test Load (Figure 2).
- 2. Com'l Only, 0°C to +70°C temperature range. PLCC and TQFP package.
- 3. "X" in part numbers indicates power rating (SA or LA).
- 4. This parameter is guaranteed by device characterization, but is not production tested.
- 5. Not available in DIP packages.

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE(1)



- 1. $R\overline{W} = V_{IH}$, $\overline{CE} = V_{IL}$, and is $\overline{OE} = V_{IL}$. Address is valid prior to the coincidental with \overline{CE} transition Low.
- 2. tbdd delay is required only in the case where the opposite port is completing a write operation to the same the address location. For simultaneous read operations, BUSY has no relationship to valid output data.
- 3. Start of valid data depends on which timing becomes effective last tAOE, tACE, tAA, and tBDD.

TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE(3)



NOTES:

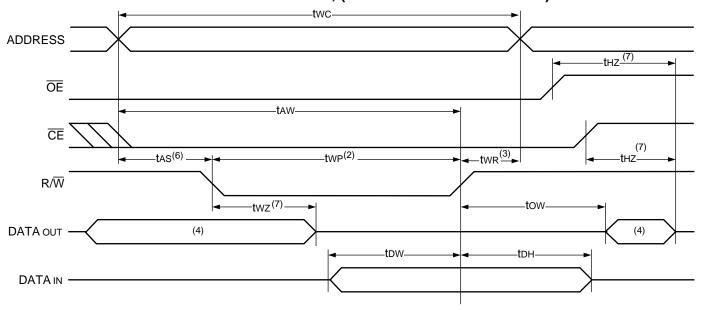
- 1. Timing depends on which signal is asserted last, $\overline{\text{OE}}$ or $\overline{\text{CE}}$.
- 2. Timing depends on which signal is deaserted first, $\overline{\text{OE}}$ or $\overline{\text{CE}}$.
- 3. $R/\overline{W} = VIH$ and the address is valid prior to or coincidental with \overline{CE} transition Low.
- 4. Start of valid data depends on which timing becomes effective last tAOE, tACE, tAA, and tBDD.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE⁽⁵⁾

		7130	1		(25 ⁽⁶⁾	7130)X35	7130	0X55	7130	X100	
				7140X25 ⁽⁶⁾		7140X35		7140X55		7140X100		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Write Cycle												
twc	Write Cycle Time ⁽³⁾	20	_	25	_	35	_	55	_	100	_	ns
tew	Chip Enable to End-of-Write	15	_	20	_	30	_	40	_	90	_	ns
taw	Address Valid to End-of-Write	15	_	20	_	30	_	40	_	90	_	ns
tas	Address Set-up Time	0	_	0	_	0	_	0	_	0	_	ns
twp	Write Pulse Width ⁽⁴⁾	15	_	15	_	25	_	30	_	55	_	ns
twr	Write Recovery Time	0	_	0	_	0		0	_	0	_	ns
tow	Data Valid to End-of-Write	10	_	12	_	15	_	20	_	40	_	ns
tHZ	Output High-Z Time ⁽¹⁾	I —	10		10	_	15		25	_	40	ns
tDH	Data Hold Time	0	_	0	_	0	_	0	_	0	_	ns
twz	Write Enabled to Output in High-Z ⁽¹⁾		10		10	_	15		25	_	40	ns
tow	Output Active From End-of-Write ⁽¹⁾	0	_	0	_	0		0		0	_	ns

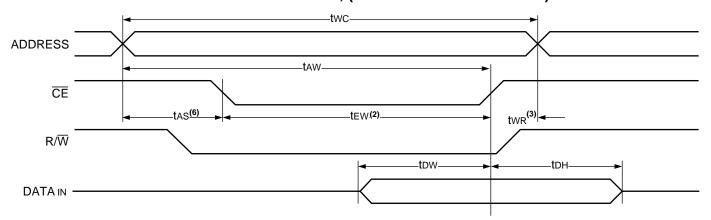
- 2689 tbl 10
- 1. Transition is measured ±500mV from Low or High-impedance voltage with Output Test Load (Figure 2). This parameter is guaranteed by device characterization but is not production tested.
- 2. 0°C to +70°C temperature range only, PLCC and TQFP packages.
- 3. For MASTER/SLAVE combination, two = tbaa + twp, since $R/\overline{W} = VIL$ must occur after tbaa.
- 4. If \overline{OE} is low during a $R\overline{W}$ controlled write cycle, the write pulse width must be the larger of twp or (twz + tpw) to allow the I/O drivers to turn off data to be placed on the bus for the required tpw. If \overline{OE} is High during a $R\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified twp.
- 5. "X" in part numbers indicates power rating (SA or LA).
- 6. Not available in DIP packages.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, (R/W CONTROLLED TIMING)(1,5,8)



2689 drw 10

TIMING WAVEFORM OF WRITE CYCLE NO. 2, (CE CONTROLLED TIMING)(1,5)



2689 drw 11

- 1. R/\overline{W} or \overline{CE} must be High during all address transitions.
- 2. A write occurs during the overlap (tew or twp) of $\overline{CE} = VIL$ and $R/\overline{W} = VIL$.
- 3. twn is measured from the earlier of \overline{CE} or R/\overline{W} going High to the end of the write cycle.
- 4. During this period, the I/O pins are in the output state and input signals must not be applied.
- 5. If the CE Low transition occurs simultaneously with or after the R/W Low transition, the outputs remain in the High-impedance state.
- 6. Timing depends on which enable signal (\overline{CE} or R/\overline{W}) is asserted last.
- 7. This parameter is determined be device characterization, but is not production tested. Transition is measured +/- 500mV from steady state with the Output Test Load (Figure 2).
- 8. If \overline{OE} is low during a R/W controlled write cycle, the write pulse width must be the larger of twp or (twz + tow) to allow the I/O drivers to turn off and data to be placed on the bus for the required tow. If \overline{OE} is High during a R/W controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified twp.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE⁽⁷⁾

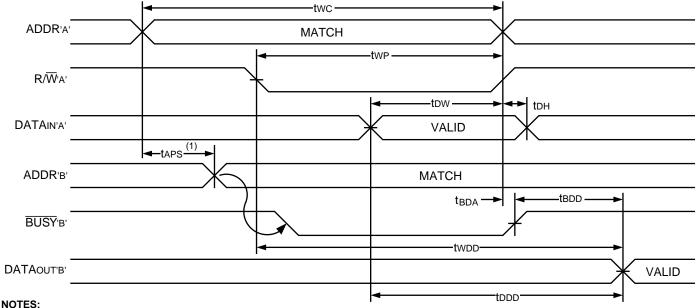
		7130	X20 ⁽¹⁾	7130	X25 ⁽⁹⁾	7130)X35	7130	X55	7130	X100	
				7140	X25 ⁽⁹⁾	7140	X35	7140	X55	7140	X100	
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Busy T	iming (For Master IDT7130 Only)											
t BAA	BUSY Access Time from Address	_	20	_	20	_	20	_	30	_	50	ns
tBDA	BUSY Disable Time from Address	_	20	_	20	_	20	_	30	_	50	ns
tBAC	BUSY Access Time from Chip Enable		20	_	20	_	20		30	_	50	ns
tBDC	BUSY Disable Time from Chip Enable	_	20	_	20	_	20	_	30	_	50	ns
twH	Write Hold After BUSY ⁽⁶⁾	12	_	15	_	20	_	20	_	20	_	ns
twdd	Write Pulse to Data Delay ⁽²⁾	_	40	_	50	_	60	_	80	_	120	ns
tDDD	Write Data Valid to Read Data Delay(2)		30	_	35	_	35	_	55	_	100	ns
taps	Arbitration Priority Set-up Time ⁽³⁾	5	_	5	_	5	_	5	_	5	_	ns
tBDD	BUSY Disable to Valid Data ⁽⁴⁾	_	25	_	35	_	35		50	_	65	ns
Busy T	iming (For Slave IDT7140 Only)	_										
twB	Write to BUSY Input ⁽⁵⁾	0	_	0	_	0		0	_	0	_	ns
twH	Write Hold After BUSY ⁽⁶⁾	12	_	15	_	20	_	20	_	20	_	ns
twdd	Write Pulse to Data Delay ⁽²⁾	_	40	_	50	_	60	_	80	_	120	ns
tDDD	Write Data Valid to Read Data Delay(2)	_	30	-	35	_	35		55	_	100	ns

NOTES:

2689 tbl 11

- 1. Com'l Only, 0°C to +70°C temperature range. PLCC and TQFP packages only.
- 2. Port-to-port delay through RAM cells from the writing port to the reading port, refer to "Timing Waveform of Write with Port-to-Port Read and BUSY."
- 3. To ensure that the earlier of the two ports wins.
- 4. tbdd is a calculated parameter and is the greater of 0, twdd twp (actual), or tddd tdw (actual).
- 5. To ensure that a write cycle is inhibited on port 'B' during contention on port 'A'.
- 6. To ensure that a write cycle is completed on port 'B' after contention on port 'A'.
- 7. "X" in part numbers indicates power rating (SA or LA).
- 8. Not available in DIP packages.

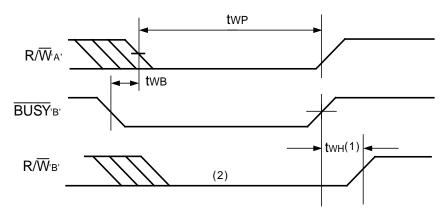
TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT READ AND BUSY (2.3.4)



- 1. To ensure that the earlier of the two ports wins. tBDD is ignored for slave (IDT7140).
- 2. $\overline{CE}L = \overline{CE}R = VIL$
- 3. $OE = V_{IL}$ for the reading port.
- 4. All timing is the same for the left and right ports. Port 'A' may be either the left or right port. Port "B" is opposite from port "A".

2689 drw 12

TIMING WAVEFORM OF WRITE WITH BUSY(3)

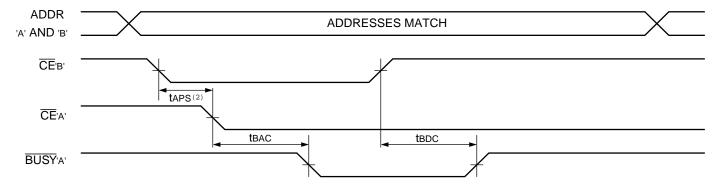


2689 drw 13

NOTES:

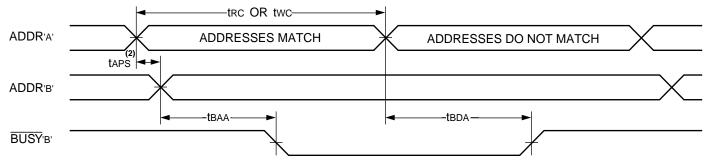
- 1. twn must be met for both BUSY Input (IDT7140, slave) or Output (IDT7130 master).
- 2. BUSY is asserted on port 'B' blocking R/W'B', until BUSY'B' goes High.
- 3. All timing is the same for the left and right ports. Port 'A' may be either the left or right port. Port "B" is opposite from port "A".

TIMING WAVEFORM OF BUSY ARBITRATION CONTROLLED BY $\overline{\text{CE}}$ TIMING (1)



2689 drw 14

TIMING WAVEFORM OF BUSY ARBITRATION CONTROLLED BY ADDRESS MATCH TIMING (1)



2689 drw 15

- 1. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
- 2. If taps is not satisified, the BUSY will be asserted on one side or the other, but there is no guarantee on which side BUSY will be asserted (7130 only).

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE⁽²⁾

		7130>	(20 ⁽¹⁾	7130X25 ⁽³⁾ 7140X25 ⁽³⁾		7130X35 7140X35		7130X55 7140X55		7130X100 7140X100		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Interrup	t Timing											
tas	Address Set-up Time	0		0	_	0	_	0	_	0	_	ns
twr	Write Recovery Time	0		0	_	0	_	0	_	0	_	ns
tins	Interrupt Set Time	_	20	_	25	_	25		45	_	60	ns
tinr	Interrupt Reset Time	_	20	_	25	_	25	_	45	_	60	ns

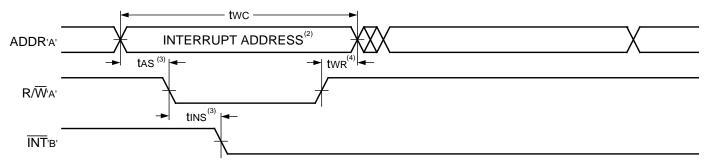
NOTES:

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- 1. 0°C to +70°C temperature range only, PLCC and TQFP packages.
- 2. "X" in part numbers indicates power rating (SA or LA).
- 3. Not available in DIP packages.

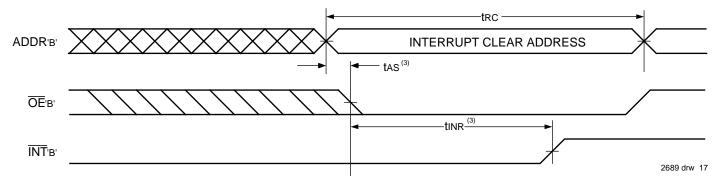
TIMING WAVEFORM OF INTERRUPT MODE

INT SET:



INT CLEAR:

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- 1. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
- 2. See Interrupt Truth Table.
- 3. Timing depends on which enable signal ($\overline{\text{CE}}$ or R/\overline{W}) is asserted last.
- 4. Timing depends on which enable signal (CE or R/W) is de-asserted first.

TRUTH TABLES

TABLE I — NON-CONTENTION READ/WRITE CONTROL⁽⁴⁾

Left or Right Port(1)				
R/W	CE	ŌĒ	D0-7	Function
Х	Н	Х	Z	Port Disabled and in Power- Down Mode, ISB2 or ISB4
Х	Н	Х	Z	CER = CEL = VIH, Power-Down Mode, ISB1 or ISB3
L	L	Х	DATAIN	Data on Port Written Into Memory (2)
Н	L	L	DATAout	Data in Memory Output on Port ⁽³⁾
Н	L	Н	Z	High Impedance Outputs

NOTES:

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- 1. $A0L A10L \neq A0R A10R$. 2. If $\overline{BUSY} = L$, data is not written.
- 3. If $\overline{\text{BUSY}} = \text{L}$, data may not be valid, see two and too timing.
- 4. 'H' = VIH, 'L' = VIL, 'X' = DON'T CARE, 'Z' = HIGH IMPEDANCE

TABLE II — INTERRUPT FLAG^(1,4)

Left Port				Right Port						
R/WL	CEL	ŌĒL	A9L - A0L	ĪNT∟	R/W R	CER	OE R	A9L - A0R	INT R	Function
L	L	Х	3FF	Х	Х	Х	Х	Χ	L ⁽²⁾	Set Right INTR Flag
Х	Х	Х	Х	Х	Х	L	L	3FF	H ⁽³⁾	Reset Right INTR Flag
X	Х	Χ	Х	L ⁽³⁾	L	L	Х	3FE	Х	Set Left INTL Flag
Х	L	L	3FE	H ⁽²⁾	Х	Х	Х	Х	Х	Reset Left INTL Flag

NOTES:

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- 1. Assumes $\overline{BUSY}L = \overline{BUSY}R = VIH$
- 2. If $\overline{BUSY}L = VIL$, then No Change.
- 3. If BUSYR = VIL, then No Change.
- 4. 'H' = HIGH,' L' = LOW,' X' = DON'T CARE

TABLE III — ADDRESS BUSY ARBITRATION

	Inp	uts	Out	puts	
CEL	<u>CE</u> R	A0L-A9L A0R-A9R	BUSY _L (1)	BUSYR ⁽¹⁾	Function
Х	Х	NO MATCH	Н	Н	Normal
Н	Х	MATCH	Н	Н	Normal
Х	Н	MATCH	Н	Н	Normal
L	L	MATCH	(2)	(2)	Write Inhibit ⁽³⁾

NOTES:

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- 1. Pins BUSYL and BUSYR are both outputs for IDT7130 (master). Both are inputs for IDT7140 (slave). BUSYx outputs on the IDT7130 are open drain, not push-pull outputs. On slaves the BUSYx input internally inhibits writes.
- 2. 'L' if the inputs to the opposite port were stable prior to the address and enable inputs of this port. 'H' if the inputs to the opposite port became stable after the address and enable inputs of this port. If tAPS is not met, either BUSYL or BUSYR = Low will result. BUSYL and BUSYR outputs can not be low simultaneously.
- 3. Writes to the left port are internally ignored when BUSYL outputs are driving Low regardless of actual logic level on the pin. Writes to the right port are internally ignored when BUSYR outputs are driving Low regardless of actual logic level on the pin.

FUNCTIONAL DESCRIPTION

The IDT7130/IDT7140 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT7130/IDT7140 has an automatic power down feature controlled by $\overline{\text{CE}}$. The $\overline{\text{CE}}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{\text{CE}} = \text{V}_{\text{IH}}$). When a port is enabled, access to the entire memory array is permitted.

INTERRUPTS

If the user chooses to use the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag (\overline{INTL}) is asserted when the right port writes to memory location 3FE (HEX), where a write is defined as the $\overline{CE} = R/\overline{W} = V_{IL}$ per the Truth Table. The left port clears the interrupt by access address location 3FE access when $\overline{CER} = \overline{OER} = V_{IL}$, R/\overline{W} is a "don't care". Likewise, the right port interrupt flag (\overline{INTR}) is asserted when the left port writes to memory location 3FF (HEX) and to clear the interrupt flag (\overline{INTR}), the right port must access the memory location 3FF. The message (8 bits) at 3FE or 3FF is user-defined, since it is an addressable SRAM location. If the interrupt function is not used, address locations 3FE and 3FF are not used as mail boxes, but as part of the random access memory. Refer to Table II for the interrupt operation.

BUSY LOGIC

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is "Busy". The Busy pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a busy indication, the write signal is gated internally to prevent the write from proceeding.

The use of busy logic is not required or desirable for all applications. In some cases it may be useful to logically OR the busy outputs together and use any busy indication as an interrupt source to flag the event of an illegal or illogical operation. In slave mode the $\overline{\text{BUSY}}$ pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the $\overline{\text{BUSY}}$ pins High. If desired, unintended write operations can be prevented to a port by tying the Busy pin for that port Low.

The Busy outputs on the IDT7130 RAM (Master) are open drain type outputs and require open drain resistors to operate. If these RAMs are being expanded in depth, then the Busy indication for the resulting array does not require the use of an external AND gate.

WIDTH EXPANSION WITH BUSY LOGIC MASTER/SLAVE ARRAYS

When expanding an RAM array in width while using busy logic, one master part is used to decide which side of the RAM array will receive a busy indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master, use the busy signal as a write inhibit signal. Thus on the IDT7130/IDT7140 RAMs the Busy pin is an output if the part is Master (IDT7130), and the Busy pin is an input if the part is a Slave (IDT7140) as shown in Figure 4.

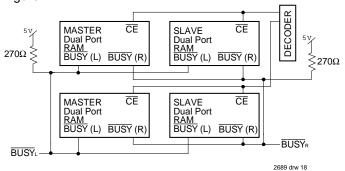
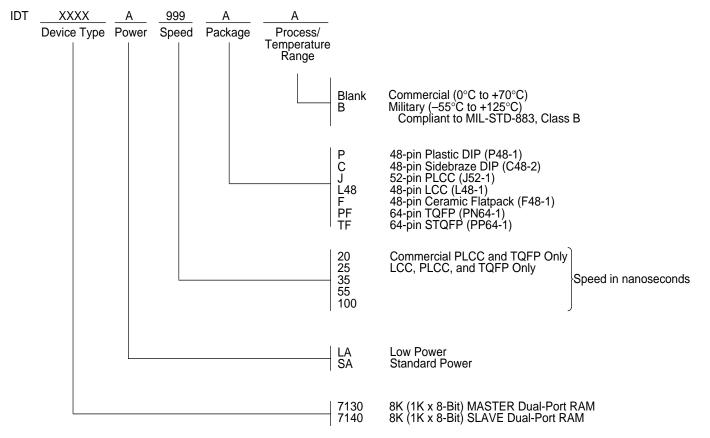


Figure 4. Busy and chip enable routing for both width and depth expansion with IDT7130 (Master) and IDT7140 (Slave) RAMs.

If two or more master parts were used when expanding in width, a split decision could result with one master indicating busy on one side of the array and another master indicating busy on one other side of the array. This would inhibit the write operations from one port for part of a word and inhibit the write operations from the other port for the other part of the word.

The Busy arbitration, on a Master, is based on the chip enable and address signals only. It ignores whether an access is a read or write. In a master/slave array, both address and chip enable must be valid long enough for a busy flag to be output from the master before the actual write pulse can be initiated with either the R/\overline{W} signal or the byte enables. Failure to observe this timing can result in a glitched internal write inhibit signal and corrupted data in the slave.

ORDERING INFORMATION



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