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74ALVC16245
Low Voltage 16-Bit Bidirectional Transceiver with 3.6V Tolerant Inputs and Outputs

General Description

The ALVC16245 contains sixteen non-inverting bidirectional buffers with 3-STATE outputs and is intended for bus oriented applications. The device is byte controlled. Each byte has separate 3-STATE control inputs which can be shorted together for full 16-bit operation. The $T/\overline{R}$ inputs determine the direction of data flow through the device. The $\overline{OE}$ inputs disable both the A and B ports by placing them in a high impedance state.

The 74ALVC16245 is designed for low voltage (1.65V to 3.6V) V_{CC} applications with I/O compatibility up to 3.6V.

The 74ALVC16245 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

Features

- 1.65V–3.6V V_{CC} supply operation
- 3.6V tolerant inputs and outputs
- t_{PD}
    3.0 ns max for 3.0V to 3.6V V_{CC}
    3.5 ns max for 2.3V to 2.7V V_{CC}
    6.0 ns max for 1.65V to 1.95V V_{CC}
- Power-down high impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- Uses patented noise/EMI reduction circuitry
- Latchup conforms to JEDEC JED78
- ESD performance:
    Human body model > 2000V
    Machine model >200V
- Also packaged in plastic Fine-Pitch Ball Grid Array (FBGA)

Note 1: To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.
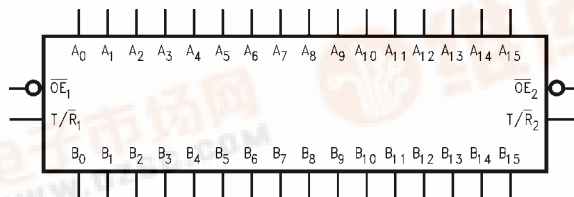
Ordering Code:

Order Number	Package Number	Package Description
74ALVC16245G (Note 2)(Note 3)	BGA54A	54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
74ALVC16245MTD (Note 3)	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Note 2: Ordering code "G" indicates Trays.

Note 3: Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.
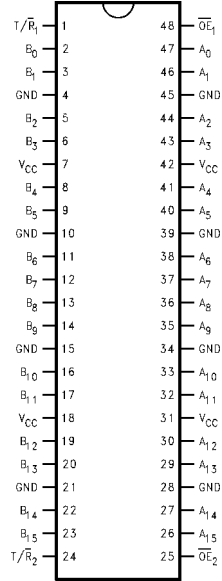
Logic Symbol

Connection Diagrams

Pin Assignment of TSSOP

$T/\overline{R}_1$	1	48	$\overline{OE}_1$
B_0	2	47	A_0
B_1	3	46	A_1
GND	4	45	GND
B_2	5	44	A_2
B_3	6	43	A_3
V_{CC}	7	42	V_{CC}
B_4	8	41	A_4
B_5	9	40	A_5
GND	10	39	GND
B_6	11	38	A_6
B_7	12	37	A_7
B_8	13	36	A_8
B_9	14	35	A_9
GND	15	34	GND
B_{10}	16	33	A_{10}
B_{11}	17	32	A_{11}
V_{CC}	18	31	V_{CC}
B_{12}	19	30	A_{12}
B_{13}	20	29	A_{13}
GND	21	28	GND
B_{14}	22	27	A_{14}
B_{15}	23	26	A_{15}
$T/\overline{R}_2$	24	25	$\overline{OE}_2$

Pin Assignment for FBGA
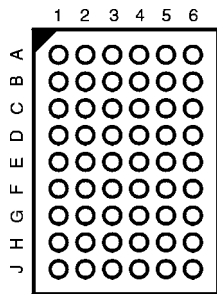
(Top Thru View)

Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
$T/\overline{R}_n$	Transmit/Receive Input
A_0–A_{15}	Side A Inputs or 3-STATE Outputs
B_0–B_{15}	Side B Inputs or 3-STATE Outputs
NC	No Connect

FBGA Pin Assignments

	1	2	3	4	5	6
A	B_0	NC	$T/\overline{R}_1$	$\overline{OE}_1$	NC	A_0
B	B_2	B_1	NC	NC	A_1	A_2
C	B_4	B_3	V_{CC}	V_{CC}	A_3	A_4
D	B_6	B_5	GND	GND	A_5	A_6
E	B_8	B_7	GND	GND	A_7	A_8
F	B_{10}	B_9	GND	GND	A_9	A_{10}
G	B_{12}	B_{11}	V_{CC}	V_{CC}	A_{11}	A_{12}
H	B_{14}	B_{13}	NC	NC	A_{13}	A_{14}
J	B_{15}	NC	$T/\overline{R}_2$	$\overline{OE}_2$	NC	A_{15}

Truth Tables

Inputs		Outputs
$\overline{OE}_1$	$T/\overline{R}_1$	
L	L	Bus B_0–B_7 Data to Bus A_0–A_7
L	H	Bus A_0–A_7 Data to Bus B_0–B_7
H	X	HIGH Z State on A_0–A_7, B_0–B_7

Inputs		Outputs
$\overline{OE}_2$	$T/\overline{R}_2$	
L	L	Bus B_8–B_{15} Data to Bus A_8–A_{15}
L	H	Bus A_8–A_{15} Data to Bus B_8–B_{15}
H	X	HIGH Z State on A_8–A_{15}, B_8–B_{15}

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial (HIGH or LOW, inputs and I/O's may not float)
Z = High Impedance

Logic Diagram

1 of 16
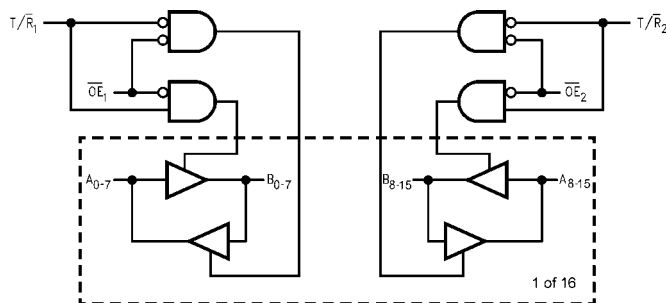
Absolute Maximum Ratings(Note 4)

Supply Voltage (V_{CC})	−0.5V to +4.6V
DC Input Voltage (V_I)	−0.5V to 4.6V
Output Voltage (V_O) (Note 5)	−0.5V to V_{CC} +0.5V
DC Input Diode Current (I_{IK})	
V_I < 0V	−50 mA
DC Output Diode Current (I_{OK})	
V_O < 0V	−50 mA
DC Output Source/Sink Current	
(I_{OH}/I_{OL})	±50 mA
DC V_{CC} or GND Current per	
Supply Pin (I_{CC} or GND)	±100 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C

Recommended Operating Conditions (Note 6)

Power Supply	
Operating	1.65V to 3.6V
Input Voltage	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Free Air Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate ($\Delta t/\Delta V$)	
V_{IN} = 0.8V to 2.0V, V_{CC} = 3.0V	10 ns/V

Note 4: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 5: I_O Absolute Maximum Rating must be observed.

Note 6: Floating or unused control inputs must be held HIGH or LOW.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
V_{IH}	HIGH Level Input Voltage		1.65 - 1.95	0.65 x V_{CC}		
			2.3 - 2.7	1.7		V
			2.7 - 3.6	2.0		
V_{IL}	LOW Level Input Voltage		1.65 - 1.95		0.35 x V_{CC}	
			2.3 - 2.7		0.7	V
			2.7 - 3.6		0.8	
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 µA	1.65 - 3.6	V_{CC} - 0.2		
		I_{OH} = −4 mA	1.65	1.2		
		I_{OH} = −6 mA	2.3	2.0		
		I_{OH} = −12 mA	2.3	1.7		V
			2.7	2.2		
			3.0	2.4		
		I_{OH} = −24 mA	3.0	2		
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 µA	1.65 - 3.6		0.2	
		I_{OL} = 4 mA	1.65		0.45	
		I_{OL} = 6 mA	2.3		0.4	V
		I_{OL} = 12 mA	2.3		0.7	
			2.7		0.4	
		I_{OL} = 24 mA	3.0		0.55	
I_I	Input Leakage Current	$0 \leq V_I \leq 3.6V$	3.6		±5.0	µA
I_{OZ}	3-STATE Output Leakage	$0 \leq V_O \leq 3.6V$	3.6		±10	µA
I_{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND, I_O = 0	3.6		40	µA
ΔI_{CC}	Increase in I_{CC} per Input	$V_{IH} = V_{CC}$ − 0.6V	3 - 3.6		750	µA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $R_L = 500\Omega$								Units
		C_L = 50 pF				C_L = 30 pF				
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		$V_{CC} = 2.5V \pm 0.2V$		$V_{CC} = 1.8V \pm 0.15V$		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PHL}, t_{PLH}	Propagation Delay	1.3	3	1.5	3.5	1.0	3.0	1.5	6.0	ns
t_{PZL}, t_{PZH}	Output Enable Time	1.3	4.3	1.5	5.4	1.0	4.9	1.5	9.3	ns
t_{PLZ}, t_{PHZ}	Output Disable Time	1.3	4.2	1.5	4.7	1.0	4.2	1.5	7.6	ns

Capacitance

Symbol	Parameter		Conditions	$T_A = +25°C$		Units
				V_{CC}	Typical	
C_{IN}	Input Capacitance		V_I = 0V or V_{CC}	3.3	6	pF
C_{IO}	Input, Output Capacitance		V_O = 0V or V_{CC}	3.3	7	pF
C_{PD}	Power Dissipation Capacitance	Outputs Enabled	f = 10 MHz, C_L = 50 pF	3.3	20	pF
				2.5	20	

AC Loading and Waveforms
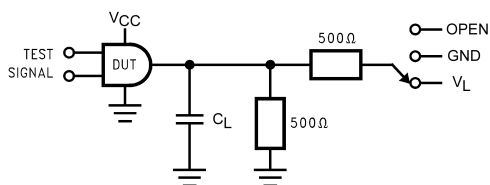
FIGURE 1. AC Test Circuit

TABLE 1. Values for Figure 1

TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	V_L
t_{PZH}, t_{PHZ}	GND

TABLE 2. Variable Matrix
(Input Characteristics: f = 1MHz; t_r = t_f = 2ns; Z_O = 50Ω)

Symbol	V_{CC}			
	3.3V ± 0.3V	2.7V	2.5 ± 0.2V	1.8V ± 0.15V
V_{mi}	1.5V	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_{mo}	1.5V	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_X	$V_{OL} + 0.3V$	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$	$V_{OL} + 0.15V$
V_Y	$V_{OH} - 0.3V$	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$	$V_{OH} - 0.15V$
V_L	6V	6V	$V_{CC}*2$	$V_{CC}*2$
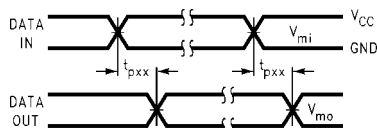
FIGURE 2. Waveform for Inverting and Non-inverting Functions
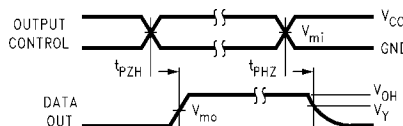
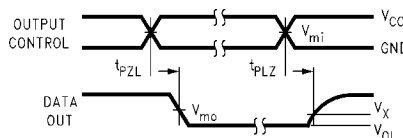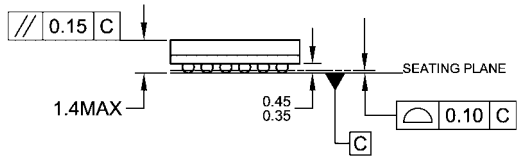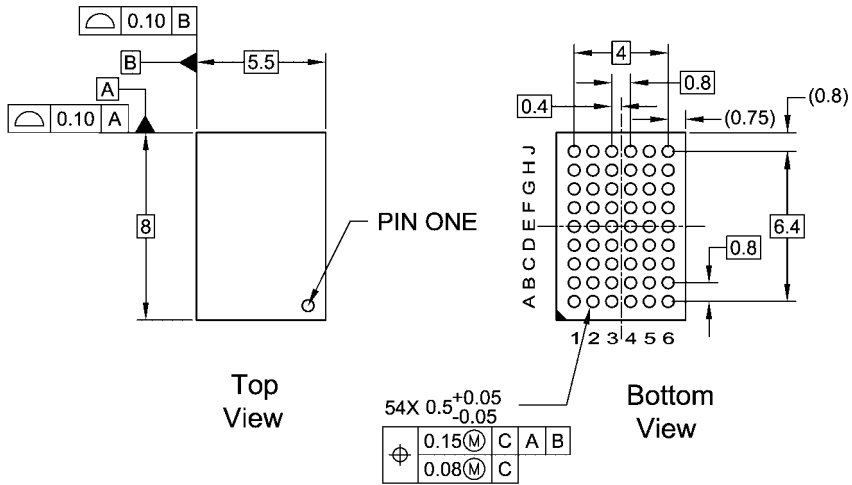**FIGURE 3. 3-STATE Output High Enable and Disable Times for Low Voltage Logic**

FIGURE 4. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

Physical Dimensions inches (millimeters) unless otherwise noted

⌒ 0.10 B

B ◄ 5.5

A

⌒ 0.10 A

8

PIN ONE

**Top
View**

**Bottom
View**

4

0.8

0.4

(0.8)

(0.75)

A B C D E F G H J

6.4

0.8

1 2 3 4 5 6

54X 0.5 +0.05 -0.05

⊕ | 0.15 Ⓜ | C | A | B
 | 0.08 Ⓜ | C

∥ 0.15 C

SEATING PLANE

1.4MAX

0.45
0.35

C

⌒ 0.10 C

NOTES:
A. THIS PACKAGE CONFORMS TO JEDEC M0-205
B. ALL DIMENSIONS IN MILLIMETERS
C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)
   .35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA54ArevD

**54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
Package Number BGA54A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

DIMENSIONS ARE IN MILLIMETERS
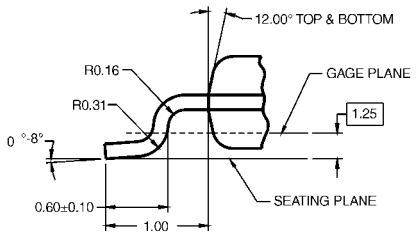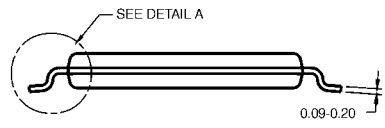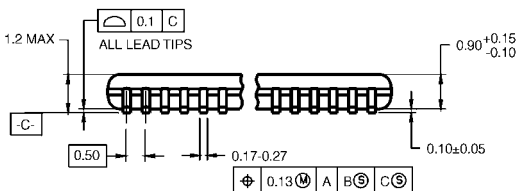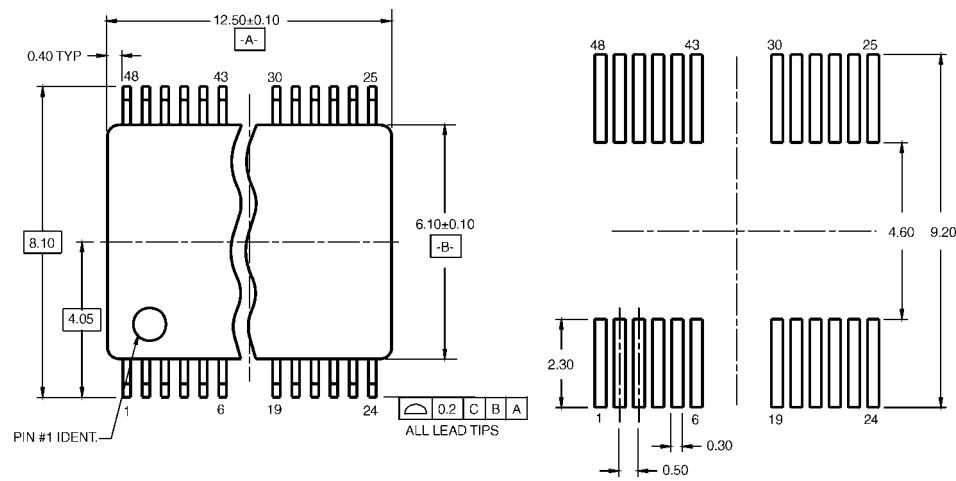
NOTES:
A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATE 7/93.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTD48RevB1

48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD48

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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