查询TPS3306-18DGK供应商 捷多邦，专业PCB打样工厂，24小时加急出货

TPS3306-15
TPS3306-18, TPS3306-20
TPS3306-25, TPS3306-33

SLVS290A–APRIL 2000–REVISED MAY 2004

DUAL PROCESSOR SUPERVISORY CIRCUITS WITH POWER-FAIL

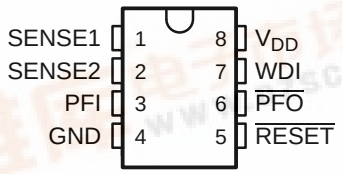
FEATURES

- Dual Supervisory Circuits With Power-Fail for DSP and Processor-Based Systems
- Voltage Monitor for Power-Fail or Low-Battery Warning
- Watchdog Timer With 0.8 Second Time-Out
- Power-On Reset Generator With Integrated 100 ms Delay Time
- Open-Drain Reset and Power-Fail Output
- Supply Current of 15 µA (Typ.)
- Supply Voltage Range . . . 2.7 V to 6 V
- Defined $\overline{\text{RESET}}$ Output From $V_{DD} \geq 1.1$ V
- MSOP-8 and SO-8 Packages
- Temperature Range . . . - 40°C to 85°C

APPLICATIONS

- Multivoltage DSPs and Processors
- Portable Battery-Powered Equipment
- Embedded Control Systems
- Intelligent Instruments
- Automotive Systems

D OR DGK PACKAGE
(TOP VIEW)

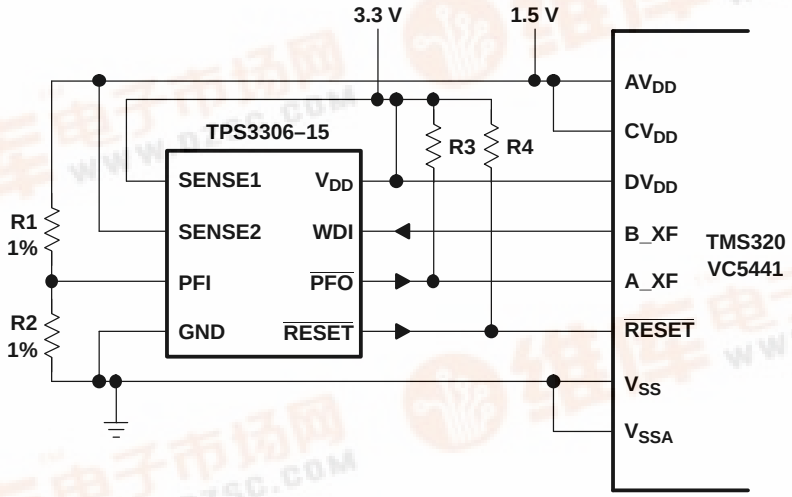


DESCRIPTION

The TPS3306 family is a series of supervisory circuits designed for circuit initialization which require two supply voltages, primarily in DSP and processor-based systems.

The product spectrum of the TPS3306-xx is designed for monitoring two independent supply voltages of 3.3 V/1.5 V, 3.3 V/1.8 V, 3.3 V/2 V, 3.3 V/2.5 V, or 3.3 V/5 V.

TYPICAL OPERATING CIRCUIT



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The various supervisory circuits are designed to monitor the nominal supply voltage, as shown in the following supply voltage monitoring table.

SUPPLY VOLTAGE MONITORING

DEVICE	NOMINAL SUPERVISED VOLTAGE		THRESHOLD VOLTAGE (typ)	
	SENSE1	SENSE2	SENSE1	SENSE2
TPS3306-15	3.3 V	1.5 V	2.93 V	1.4 V
TPS3306-18	3.3 V	1.8 V	2.93 V	1.68 V
TPS3306-20	3.3 V	2 V	2.93 V	1.85 V
TPS3306-25	3.3 V	2.5 V	2.93 V	2.25 V
TPS3306-33	5 V	3.3 V	4.55 V	2.93 V

During power-on, $\overline{RESET}$ is asserted when the supply voltage V_{DD} becomes higher than 1.1 V. Thereafter, the supervisory circuits monitor the SENSEn inputs and keep $\overline{RESET}$ active as long as SENSEn remains below the threshold voltage V_{IT}.

An internal timer delays the return of the $\overline{RESET}$ output to the inactive state (high) to ensure proper system reset. The delay time, $t_{d(typ)}$ = 100 ms, starts after SENSE1 and SENSE2 inputs have risen above the threshold voltage V_{IT}. When the voltage at SENSE1 or SENSE2 input drops below the threshold voltage V_{IT}, the output becomes active (low) again.

The integrated power-fail (PFI) comparator with separate open-drain ($\overline{PFO}$) output can be used for low-battery detection, power-fail warning, or for monitoring a power supply other than the main supply.

The TPS3306-xx devices integrate a watchdog timer that is periodically triggered by a positive or negative transition of WDI. When the supervising system fails to retrigger the watchdog circuit within the time-out interval, $t_{t(out)}$ = 0.50 s, $\overline{RESET}$ becomes active for the time period t_d. This event also reinitializes the watchdog timer. Leaving WDI unconnected disables the watchdog.

The TPS3306-xx devices are available in either 8-pin MSOP or standard 8-pin SO packages, and are characterized for operation over a temperature range of -40°C to 85°C.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES		MARKING DGK PACKAGE
	SMALL OUTLINE (D)	µ-SMALL OUTLINE (DGK)	
-40°C to 85°C	TPS3306-15D	TPS3306-15DGK	TIAIC
	TPS3306-18D	TPS3306-18DGK	TIAID
	TPS3306-20D	TPS3306-20DGK	TIAIE
	TPS3306-25D	TPS3306-25DGK	TIAIF
	TPS3306-33D	TPS3306-33DGK	TIAIG

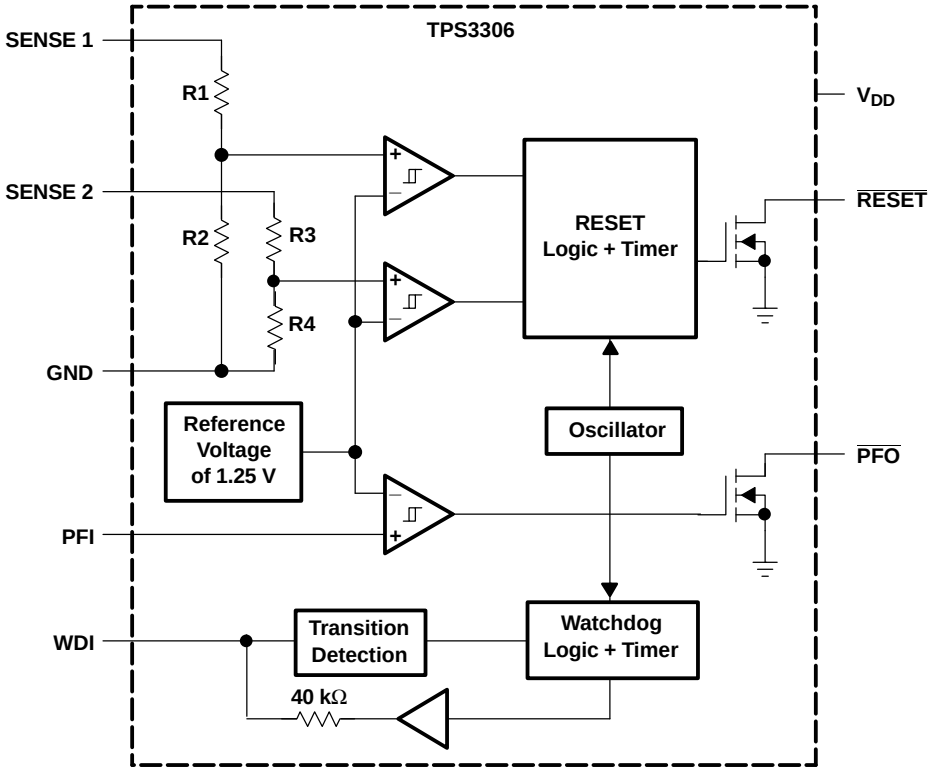
FUNCTION/TRUTH TABLES

SENSE1 > V_{IT1}	SENSE2 > V_{IT2}	$\overline{RESET}$
0	0	L
0	1	L
1	0	L
1	1	H

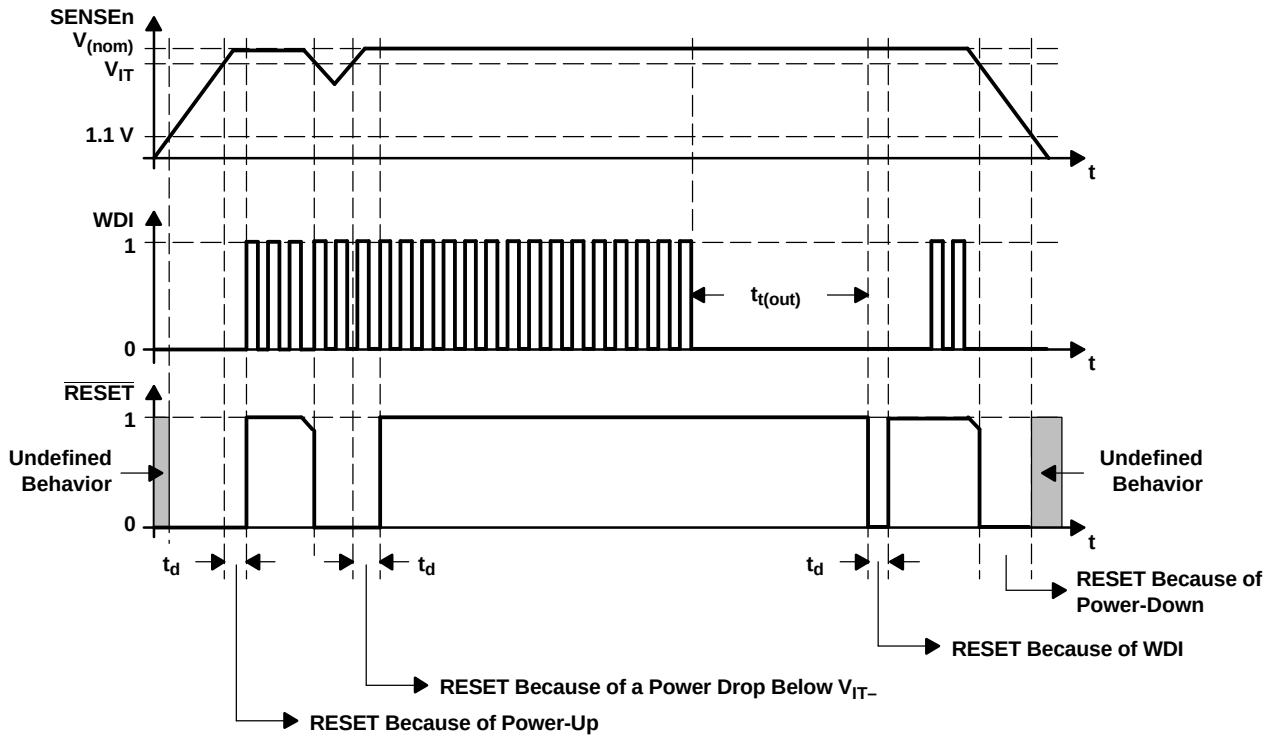
FUNCTION/TRUTH TABLES

PFI > V_{IT}	$\overline{PFO}$	TYPICAL DELAY
0"1	L"H	0.5 µs
1"0	H"L	0.5 µs

FUNCTIONAL BLOCK DIAGRAM



TIMING DIAGRAM



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
GND	4	I	Ground
PFI	3	I	Power-fail comparator input
$\overline{PFO}$	6	O	Power-fail comparator output, open-drain
$\overline{RESET}$	5	O	Active-low reset output, open-drain
SENSE1	1	I	Sense voltage input 1
SENSE2	2	I	Sense voltage input 2
WDI	7	I	Watchdog timer input
V_{DD}	8	I	Supply voltage

DETAILED DESCRIPTION

Watchdog

In a microprocessor- or DSP-based system, it is not only important to supervise the supply voltage, it is also important to ensure correct program execution. The task of a watchdog is to ensure that the program is not stalled in an indefinite loop. The microprocessor, microcontroller, or DSP has to typically toggle the watchdog input within 0.8 s to avoid a time out occurring. Either a low-to-high or a high-to-low transition resets the internal watchdog timer. If the input is unconnected or tied with a high impedance driver, the watchdog is disabled and will be retriggered internally.

DETAILED DESCRIPTION (continued)

Saving Current While Using the Watchdog

The watchdog input is internally driven low during the first 7/8 of the watchdog time-out period, then momentarily pulses high, resetting the watchdog counter. For minimum watchdog input current (minimum overall power consumption), leave WDI low for the majority of the watchdog time-out period, pulsing it low-high-low once within 7/8 of the watchdog time-out period to reset the watchdog timer. If instead WDI is externally driven high for the majority of the time-out period, a current of 5 V/40 kΩ 9 125 µA can flow into WDI.

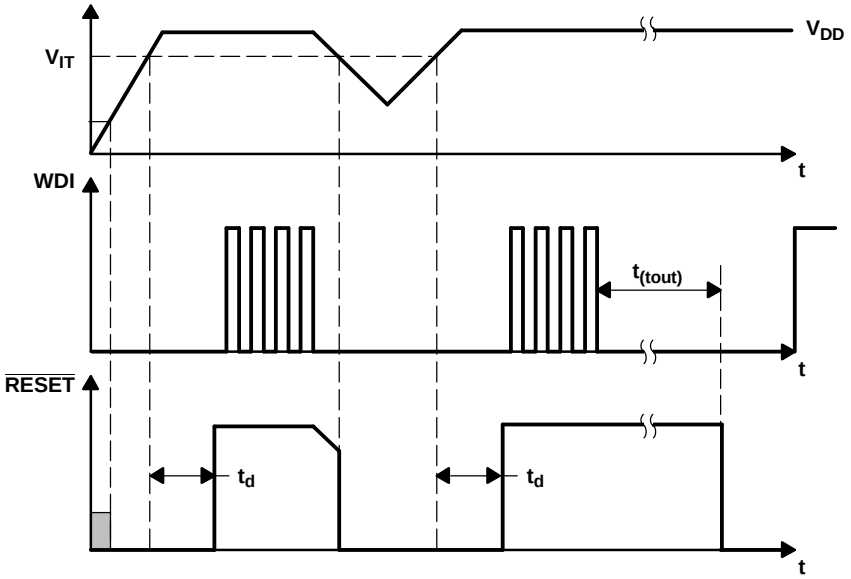
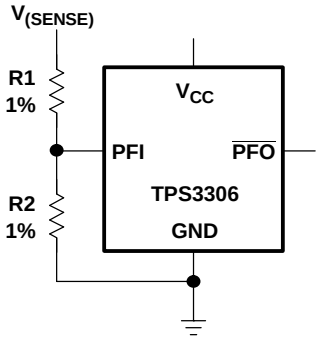


Figure 1. Watchdog Timing

Power-Fail Comparator (PFI and $\overline{PFO}$)

An additional comparator is provided to monitor voltages other than the nominal supply voltage. The power-fail-input (PFI) will be compared with an internal voltage reference of 1.25 V. If the input voltage falls below the power-fail threshold (V_{PFI}) of typ. 1.25 V, the power-fail output ($\overline{PFO}$) goes low. If it goes above 1.25 V plus about 10 mV hysteresis, the output returns to high. By connecting two external resistors, it is possible to supervise any voltages above 1.25 V. The sum of both resistors should be about 1 MΩ, to minimize power consumption and also to assure that the current in the PFI pin can be neglected compared with the current through the resistor network. The tolerance of the external resistors should be not more than 1% to ensure minimal variation of sensed voltage. If the power-fail comparator is unused, connect PFI to ground and leave $\overline{PFO}$ unconnected.



$$V_{PFI,trip} = 1.25\ V \times \frac{R_1 + R_2}{R_2}$$

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)[1]

	UNIT
Supply voltage, V_{DD} (see [2])	7 V
All other pins (see [2])	-0.3 V to 7 V
Maximum low output current, I_{OL}	5 mA
Maximum high output current, I_{OH}	- 5 mA
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{DD}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$)	±20 mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	-40°C to 85°C
Storage temperature range, T_{stg}	-65°C to 150°C
Soldering temperature	260°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND. For reliable operation, the device must not be operated at 7 V for more than t = 1000 h continuously.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DGK	424 mW	3.4 mW/°C	271 mW	220 mW
D	725 mW	5.8 mW/°C	464 mW	377 mW

RECOMMENDED OPERATING CONDITIONS

at specified temperature range

	MIN	MAX	UNIT
Supply voltage, V_{DD}	2.7	6	V
Input voltage at WDI and PFI, V_I	0	V_{DD} + 0.3	V
Input voltage at SENSE1 and SENSE2, V_I	0	$(V_{DD} + 0.3)V_{IT}/1.25$ V	V
High-level input voltage at WDI, V_{IH}	0.7 x V_{DD}		V
Low-level input voltage at WDI, V_{IL}		$0.3 \times V_{DD}$	V
Operating free-air temperature range, T_A	-40	85	°C

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Low-level output voltage	$\overline{RESET}$, $\overline{PFO}$	V_{DD} = 2.7 V to 6 V, I_{OL} = 20 µA			0.2	V
			V_{DD} = 3.3 V, I_{OL}= 2 mA			0.4	
			V_{DD} = 6 V, I_{OL} = 3 mA			0.4	
	Power-up reset voltage (see (1))		$V_{DD} \geq$ 1.1 V, I_{OL} = 20 µA			0.4	V
V_{IT}	Negative-going input threshold voltage (see (2))	V_{SENSE1}, V_{SENSE2}	V_{DD} = 2.7 V to 6 V T_A = 0°C to 85°C	1.37	1.40	1.43	V
				1.64	1.68	1.72	
				1.81	1.85	1.89	
				2.20	2.25	2.30	
				2.86	2.93	3	
				4.46	4.55	4.64	
		PFI		1.22	1.25	1.28	
		V_{SENSE1}, V_{SENSE2}	V_{DD} = 2.7 V to 6 V T_A = -40°C to 85°C	1.37	1.40	1.44	V
				1.64	1.68	1.73	
				1.81	1.85	1.90	
				2.20	2.25	2.32	
				2.86	2.93	3.02	
				4.46	4.55	4.67	
		PFI		1.22	1.25	1.29	
V_{hys}	Hysteresis	PFI	V_{IT} = 1.25 V		10		mV
		V_{SENSEn}	V_{IT} = 1.40 V		15		
			V_{IT} = 1.68 V		15		
			V_{IT} = 1.86 V		20		
			V_{IT} = 2.25 V		20		
			V_{IT} = 2.93 V		30		
			V_{IT} = 4.55 V		40		
$I_{H(AV)}$	Average high-level input current	WDI	WDI = V_{DD} = 6 V, Time average (dc = 88%)		100	150	µA
$I_{L(AV)}$	Average low-level input current		WDI = 0 V, V_{DD} = 6 V, Time average (dc = 12%)		-15	-20	
I_H	High-level input current	WDI	WDI = V_{DD} = 6 V		120	170	µA
		SENSE1	V_{SENSE1} = V_{DD} = 6 V		5	8	
		SENSE2	V_{SENSE2} = V_{DD} = 6 V		6	9	
I_L	Low-level input current	WDI	WDI = 0 V, $V_{DD,}$ = 6 V		-120	-170	µA
I_I	Input current	PFI	V_{DD} = 6 V, 0 V ≤ V_I ≤ V_{DD}	-25		25	nA
I_{DD}	Supply current				15	40	µA
C_i	Input capacitance		V_I = 0 V to V_{DD}		10		pF

(1) The lowest supply voltage at which $\overline{RESET}$ becomes active. t_r, $V_{DD} \geq$ 15 µs/V.
(2) To ensure best stability of the threshold voltage, a bypass capacitor (ceramic 0.1 µF) should be placed close to the supply terminals.

TIMING REQUIREMENTS

at V_{DD} = 2.7 V to 6 V, R_L= 1 MΩ, C_L= 50 pF, T_A= 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_w	Pulse width	SENSEn	$V_{SENSEnL} = V_{IT}$ - 0.2 V, $V_{SENSEnH} = V_{IT}$ + 0.2 V	6			µs
		WDI	$V_{IH} = 0.7 \times V_{DD}$, $V_{IL} = 0.3 \times V_{DD}$	100			ns

SWITCHING CHARACTERISTICS

at V_{DD} = 2.7 V to 6 V, R_L= 1 MΩ, C_L = 50 pF, T_A= 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{t(out)}$	Watchdog time out		$V_{I(SENSEn)} \geq V_{IT}$ + 0.2 V, See timing diagram	0.5	0.8	1.2	s
t_d	Delay time		$V_{I(SENSEn)} \geq V_{IT}$ + 0.2 V, See timing diagram	70	100	140	ms
t_{PHL}	Propagation (delay) time, high-to-low level output	SENSEn to $\overline{RESET}$	$V_{IH} = V_{IT}$ + 0.2 V, $V_{IL} = V_{IT}$ - 0.2 V		1	5	µs
t_{PHL}	Propagation (delay) time, high-to-low level output	PFI to $\overline{PFO}$			0.5	1	µs
t_{PLH}	Propagation (delay) time, low-to-high level output						

TYPICAL CHARACTERISTICS

NORMALIZED SENSE THRESHOLD VOLTAGE vs FREE-AIR TEMPERATURE AT V_{DD}

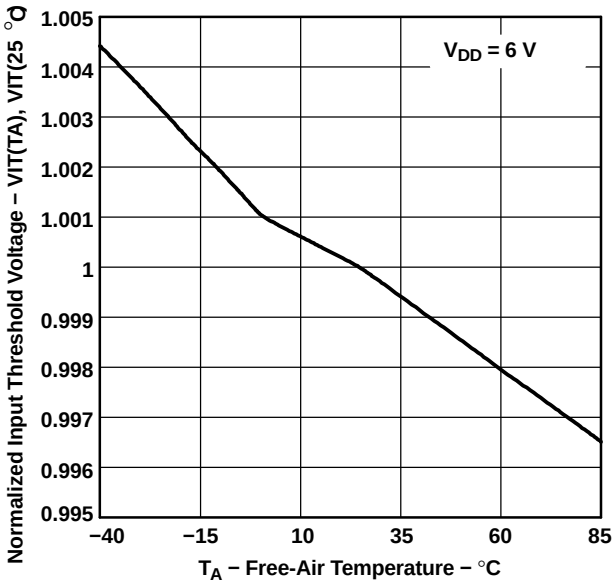


Figure 2.

SUPPLY CURRENT vs SUPPLY VOLTAGE

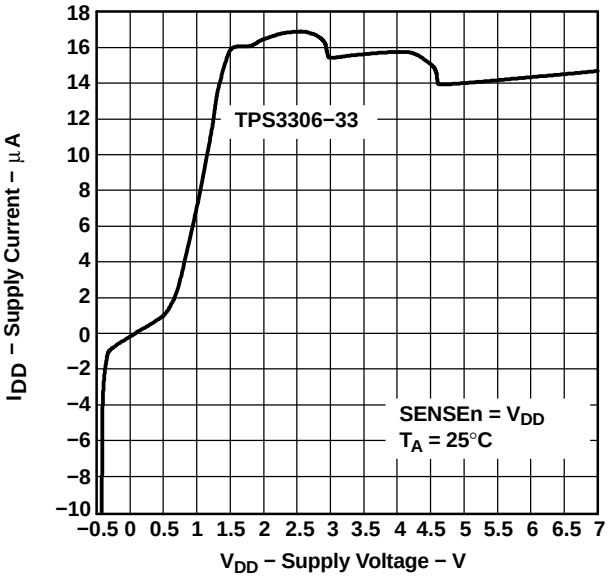


Figure 3.

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

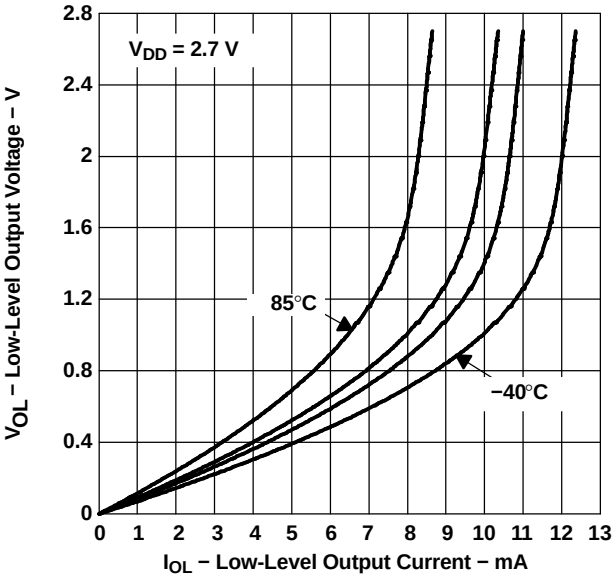


Figure 4.

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

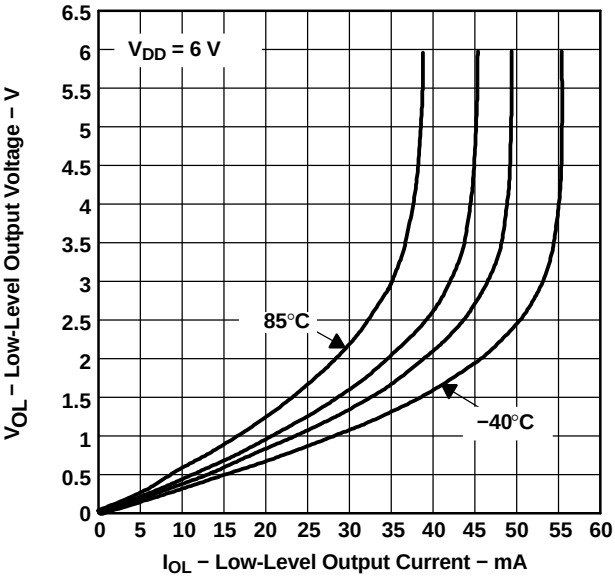


Figure 5.

TYPICAL CHARACTERISTICS (continued)

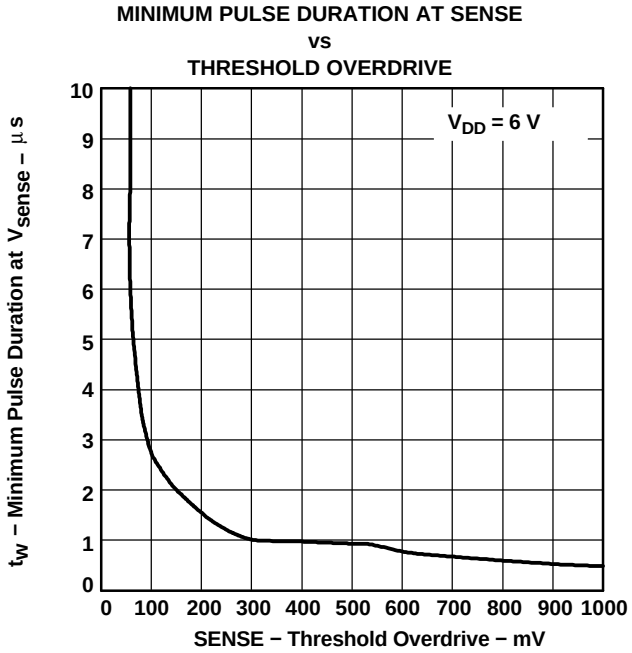
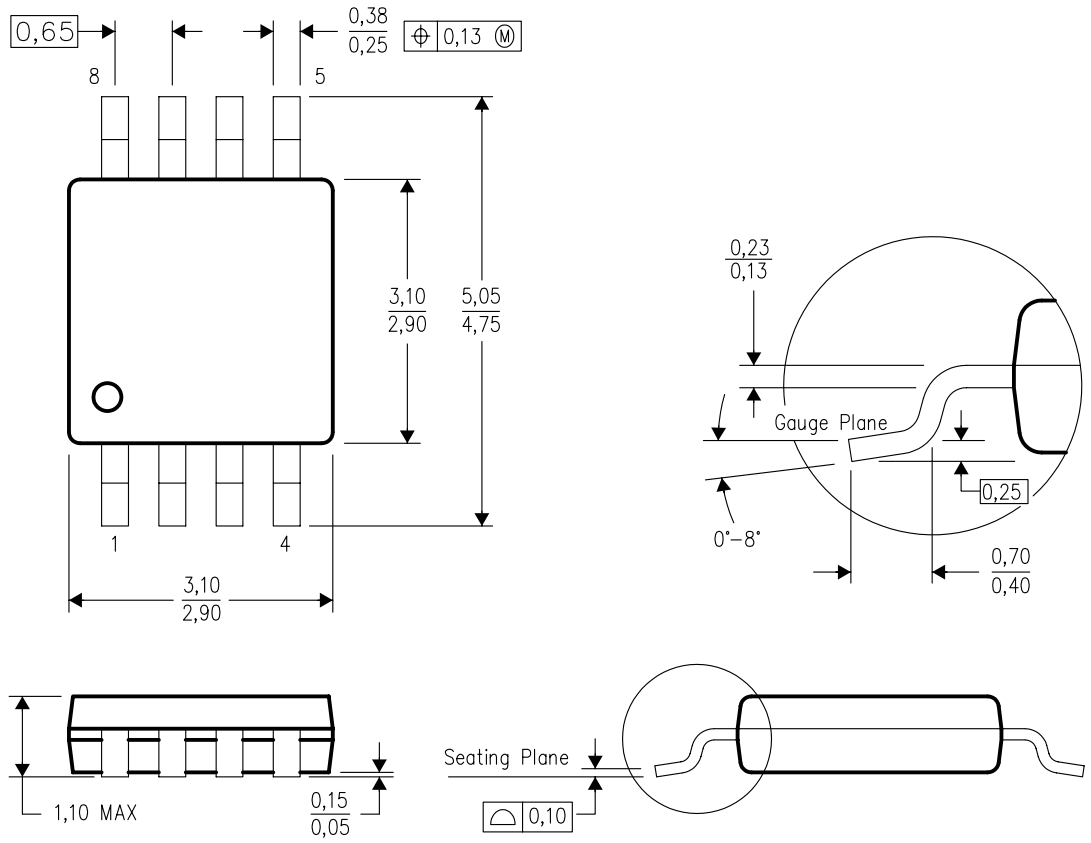


Figure 6.

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



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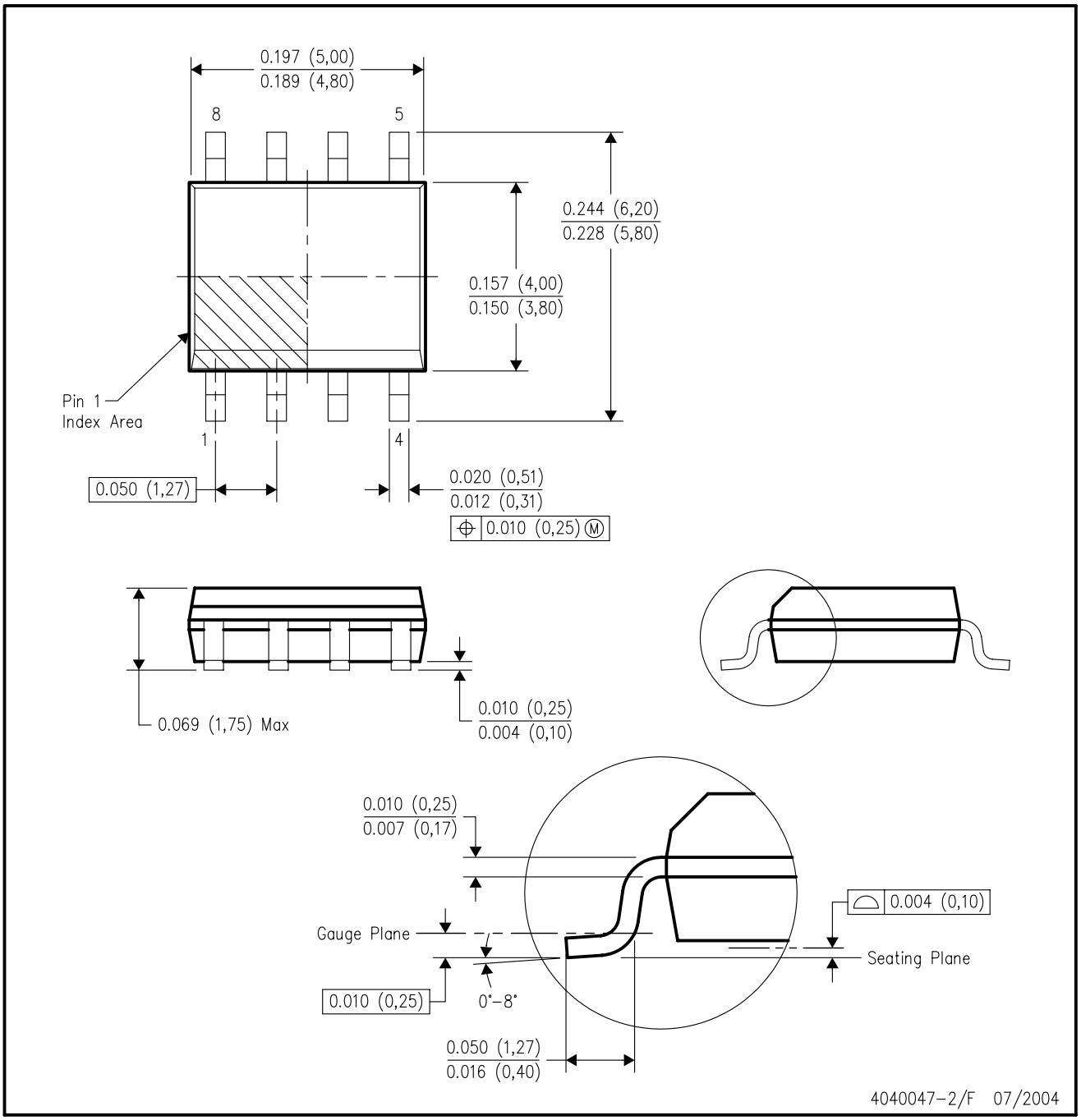
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation AA.

D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–012 variation AA.

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

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