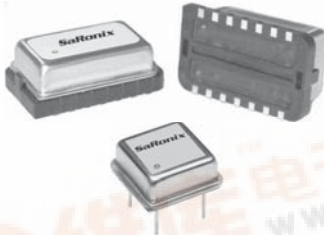


# SaRonix

## Crystal Clock Oscillator 3.3V, LVCMOS / HCMOS, Tri-State

### Technical Data

NTH / NCH Series



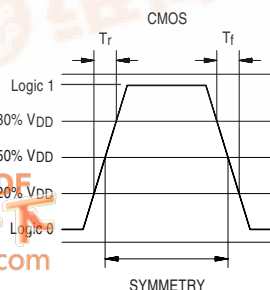
#### Description

A crystal controlled, low current, low jitter and high frequency oscillator with precise rise and fall times demanded in networking applications. The tri-state function on the NTH enables the output to go high impedance. Device is packaged in a 14 or an 8-pin DIP compatible resistance welded, all metal grounded case to reduce EMI. True SMD DIL14 versions for IR reflow are available, select option "S" in part number builder. See separate data sheet for SMD package dimensions.

#### Applications & Features

- ADSL, DSL
- DS3, ES3, E1, STS-1, T1
- Ethernet Switch, Gigabit Ethernet
- Fibre Channel Controller
- MPEG
- Network Processors
- Voice Over Packet
- 32 Bit Microprocessors
- Tri-State output on NTH
- LVCMOS / HCMOS compatible
- Available up to 106.25 MHz

#### Output Waveform



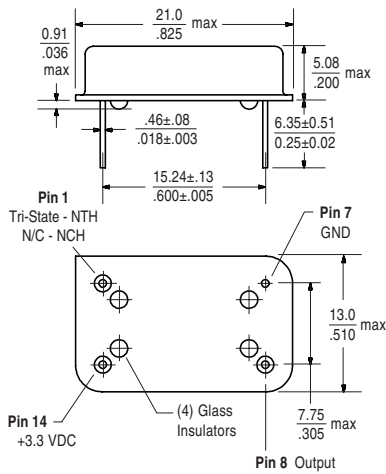
<b>Frequency Range:</b>	0.5 MHz to 106.25 MHz																		
<b>Frequency Stability:</b>	±20, ±25, ±50 or ±100 ppm over all conditions: calibration tolerance, operating temperature, input voltage change, load change, 30 day aging, shock and vibration.																		
<b>Temperature Range:</b>	Operating: 0 to +70°C or -40 to +85°C, See Part Numbering Guide Storage: -55 to +125°C																		
<b>Supply Voltage:</b>	Recommended Operating: 3.3V ±10%																		
<b>Supply Current:</b>	20mA max, 0.5 to 30 MHz 25mA max, 30+ to 50 MHz 30mA max, 50+ to 80 MHz 35mA max, 80+ to 106.25 MHz																		
<b>Output Drive:</b>	<table border="0"> <tr> <td><b>HCMOS</b></td> <td>Symmetry:</td> <td>45/55% max 0.5 to 70 MHz max 40/60% max @ 50% VDD</td> </tr> <tr> <td></td> <td>Rise and Fall Times:</td> <td>4ns max 0.5 to 50 MHz, 20% to 80% VDD 3ns max 50+ to 80 MHz 1.5ns max 80+ to 106.25 MHz</td> </tr> <tr> <td></td> <td>Logic 0:</td> <td>10% VDD max</td> </tr> <tr> <td></td> <td>Logic 1:</td> <td>90% VDD min</td> </tr> <tr> <td></td> <td>Load:</td> <td>50 pF, 0.5 to 50 MHz 30 pF, 50+ to 70 MHz 15 pF, 70+ to 106.25 MHz</td> </tr> <tr> <td></td> <td>Period Jitter RMS:</td> <td>8ps max</td> </tr> </table>	<b>HCMOS</b>	Symmetry:	45/55% max 0.5 to 70 MHz max 40/60% max @ 50% VDD		Rise and Fall Times:	4ns max 0.5 to 50 MHz, 20% to 80% VDD 3ns max 50+ to 80 MHz 1.5ns max 80+ to 106.25 MHz		Logic 0:	10% VDD max		Logic 1:	90% VDD min		Load:	50 pF, 0.5 to 50 MHz 30 pF, 50+ to 70 MHz 15 pF, 70+ to 106.25 MHz		Period Jitter RMS:	8ps max
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### Technical Data

### NTH / NCH Series

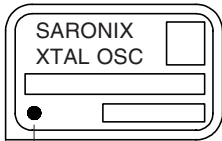
#### Package Details

##### FULL SIZE PACKAGE



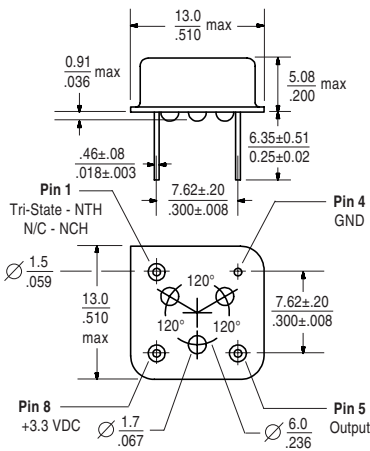
##### Standard Marking Format\*\*

Includes Date Code, Frequency & Part Number



Denotes Pin 1

##### HALF SIZE PACKAGE



##### Standard Marking Format\*\*

Includes Date Code, Frequency & Part Number



Denotes Pin 1

\*\*Exact location of items may vary

#### Part Numbering Guide

NTH 0 8 0 C 3 - 40.0000 (T)

NTH = Pin 1: Tri state, LVCMOS  
NCH = Pin 1: N/C, LVCMOS

##### Symmetry

- 0 = 40/60% max, 0 to 70°C
- 2 = 40/60% max, -40 to 85°C
- A = 45/55% max, 0 to 70°C, 70 MHz max
- C = 45/55% max, -40 to 85°C, 70 MHz max

##### Frequency Range

- 3 = 0.5 to 6 MHz
- 6 = 6+ to 24 MHz
- 8 = 24+ to 106.25 MHz

##### Package

- 0 = Full Size, Thru-Hole
- 9 = Half Size, Thru-Hole
- K = Full Size, Gull Wing
- J = Half Size, Gull Wing
- N = Half Size, Gull Wing, Spanked Leads
- S = Full Size, True SMD Adaptor (see separate data sheet for dimensions)

##### Packing Method

- (T) = Tape & Reel for SMD versions, full reel increments only, 200pcs (full size) or 250pcs (half size)
- Blank = Bulk

##### Frequency (MHz)

3.3V Supply

##### Stability Tolerance

- C = ±100ppm
- B = ±50ppm
- A = ±25ppm, 0 to +70°C only
- AA = ±20ppm, 0 to +70°C only

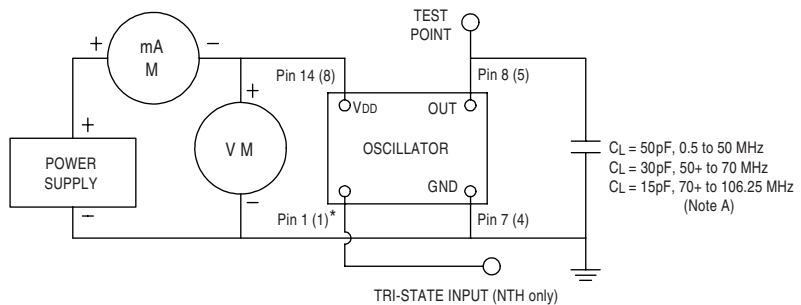
#### Tri-State Logic Table (NTH only)

Pin 1 Input	Pin 8 (5) Output
Logic 1 or NC	Oscillation
Logic 0 or GND	High Impedance

Required Input Levels on Pin 1:  
Logic 1 = 2.2V min  
Logic 0 = 0.8V max

Output: Oscillation @  $V_{IN}$ , 2.2V min  
Output: High Impedance @  $V_{IN}$ , 0.8V max  
Internal Pullup Resistance: 50KΩ min  
Control Input: Disable Output Delay: 100ns max

#### Test Circuit



$C_L$  = 50pF, 0.5 to 50 MHz  
 $C_L$  = 30pF, 50+ to 70 MHz  
 $C_L$  = 15pF, 70+ to 106.25 MHz  
(Note A)

NOTE A:  $C_L$  includes probe and fixture capacitance  
( ) Indicates pin numbers for half-size package

All specifications are subject to change without notice.

# SaRonix

## True SMD Adaptor - 7.57mm High

### Technical Data

