



### 3.3V CMOS 12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCH WITH 3-STATE OUTPUTS AND BUS-HOLD

IDT74ALVCH16260

#### FEATURES:

- 0.5 MICRON CMOS Technology
- Typical  $t_{sk(o)}$  (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- $V_{CC} = 3.3V \pm 0.3V$ , Normal Range
- $V_{CC} = 2.7V$  to  $3.6V$ , Extended Range
- $V_{CC} = 2.5V \pm 0.2V$
- CMOS power levels (0.4 $\mu$ W typ. static)
- Rail-to-Rail output swing for increased noise margin
- Available in SSOP and TSSOP packages

#### DRIVE FEATURES:

- High Output Drivers:  $\pm 24mA$
- Suitable for heavy loads

#### APPLICATIONS:

- 3.3V high speed systems
- 3.3V and lower voltage computing systems

#### DESCRIPTION:

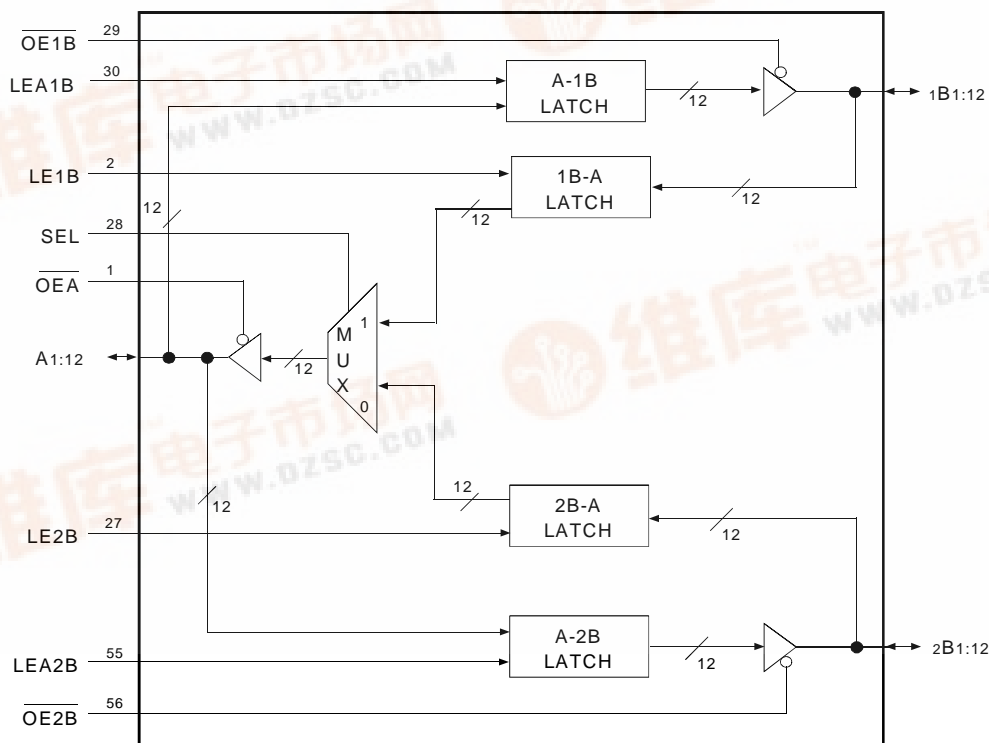
This 12-bit to 24-bit multiplexed D-type latch is built using advanced dual metal CMOS technology. The ALVCH16260 is used in applications in which two separate data paths must be multiplexed onto, or demultiplexed from, a single data path. Typical applications include multiplexing and/or demultiplexing address and data information in microprocessor or bus-interface applications. This device also is useful in memory interleaving applications.

Three 12-bit I/O ports (A1-A12, 1B1-1B12, and 2B1-2B12) are available for address and/or data transfer. The output-enable ( $\overline{OE1B}$ ,  $\overline{OE2B}$ , and  $\overline{OEA}$ ) inputs control the bus transceiver functions. The  $\overline{OE1B}$  and  $\overline{OE2B}$  control signals also allow bank control in the A-to-B direction. Address and/or data information can be stored using the internal storage latches. The latch-enable ( $LE1B$ ,  $LE2B$ ,  $LEA1B$ , and  $LEA2B$ ) inputs are used to control data storage. When the latch-enable input is high, the latch is transparent. When the latch-enable input goes low, the data present at the inputs is latched and remains latched until the latch-enable input is returned high.

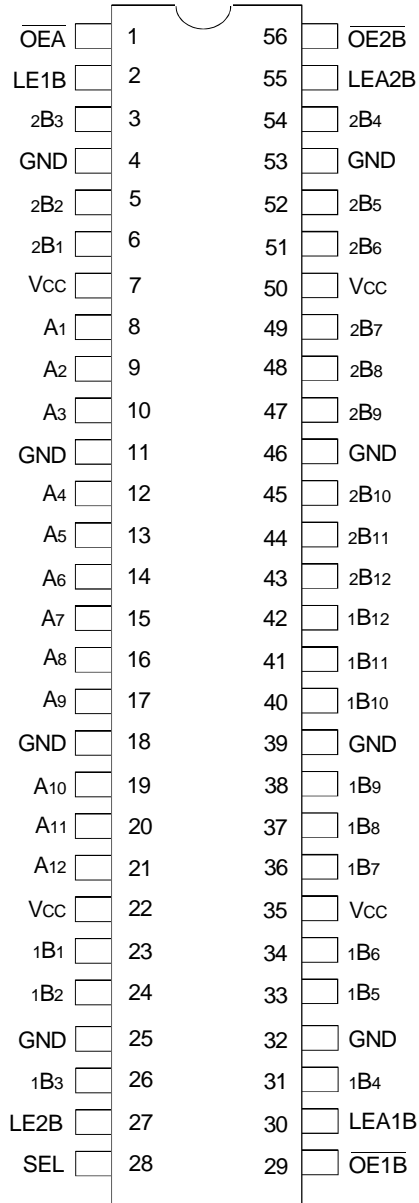
The ALVCH16260 has been designed with a  $\pm 24mA$  output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

The ALVCH16260 has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

#### FUNCTIONAL BLOCK DIAGRAM



## PIN CONFIGURATION



SSOP/ TSSOP  
TOP VIEW

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Description	Max	Unit
VTERM <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
VTERM <sup>(3)</sup>	Terminal Voltage with Respect to GND	-0.5 to V <sub>CC</sub> +0.5	V
TSTG	Storage Temperature	-65 to +150	°C
I <sub>OUT</sub>	DC Output Current	-50 to +50	mA
I <sub>IK</sub>	Continuous Clamp Current, V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>CC</sub>	±50	mA
I <sub>OK</sub>	Continuous Clamp Current, V <sub>O</sub> < 0	-50	mA
I <sub>CC</sub> I <sub>SS</sub>	Continuous Current through each V <sub>CC</sub> or GND	±100	mA

### NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V<sub>CC</sub> terminals.
- All terminals except V<sub>CC</sub>.

## CAPACITANCE (T<sub>A</sub> = +25°C, F = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	5	7	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	7	9	pF
C <sub>I/O</sub>	I/O Port Capacitance	V <sub>IN</sub> = 0V	7	9	pF

### NOTE:

- As applicable to the device type.

## FUNCTION TABLES<sup>(1)</sup>

### B-TO-A (OEĀ = H)

Inputs						Output
1B <sub>x</sub>	2B <sub>x</sub>	SEL	LE1B	LE2B	OEĀ	A <sub>x</sub>
H	X	H	H	X	L	H
L	X	H	H	X	L	L
X	X	H	L	X	L	A <sub>0</sub> <sup>(2)</sup>
X	H	L	X	H	L	H
X	L	L	X	H	L	L
X	X	L	X	L	L	A <sub>0</sub> <sup>(2)</sup>
X	X	X	X	X	H	Z

FUNCTION TABLES (CONTINUED)<sup>(1)</sup>A-TO-B ( $\overline{OE\bar{A}} = H$ )

Inputs					Outputs	
Ax	LEA1B	LEA2B	$\overline{OE1B}$	$\overline{OE2B}$	1Bx	2Bx
H	H	H	L	L	H	H
L	H	H	L	L	L	L
H	H	L	L	L	H	2B <sub>0</sub> <sup>(2)</sup>
L	H	L	L	L	L	2B <sub>0</sub> <sup>(2)</sup>
H	L	H	L	L	1B <sub>0</sub> <sup>(2)</sup>	H
L	L	H	L	L	1B <sub>0</sub> <sup>(2)</sup>	L
X	L	L	L	L	1B <sub>0</sub> <sup>(2)</sup>	2B <sub>0</sub> <sup>(2)</sup>
X	X	X	H	H	Z	Z
X	X	X	L	H	Active	Z
X	X	X	H	L	Z	Active
X	X	X	L	L	Active	Active

## NOTES:

- H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care  
Z = High Impedance
- Output level before the indicated steady-state input conditions were established.

## PIN DESCRIPTION

Pin Names	I/O	Description
Ax(1:12)	I/O	Bidirectional Data Port A. Usually connected to the CPU's address/data bus. <sup>(1)</sup>
1Bx(1:12)	I/O	Bidirectional Data Port 1B. Usually connected to the even path or even bank of memory. <sup>(1)</sup>
2Bx(1:12)	I/O	Bidirectional Data Port 2B. Usually connected to the odd path or odd bank of memory. <sup>(1)</sup>
LEA1B	I	Latch Enable Input for A-1B Latch. The latch is open when LEA1B is HIGH. Data from the A-port is latched on the HIGH to LOW transition of LEA1B.
LEA2B	I	Latch Enable Input for A-2B Latch. The latch is open when LEA2B is HIGH. Data from the A-port is latched on the HIGH to LOW transition of LEA2B.
LE1B	I	Latch Enable Input for 1B-A Latch. The latch is open when LE1B is HIGH. Data from the A-port is latched on the HIGH to LOW transition of LE1B.
LE2B	I	Latch Enable Input for 2B-A Latch. The latch is open when LE2B is HIGH. Data from the A-port is latched on the HIGH to LOW transition of LE2B.
SEL	I	1B or 2B Port Selection. When HIGH, SEL enables data transfer from 1B Port to A Port. When LOW, SEL enables data transfer from 2B Port to A Port.
$\overline{OE\bar{A}}$	I	Output Enable for A Port (Active LOW)
$\overline{OE1B}$	I	Output Enable for 1B Port (Active LOW)
$\overline{OE2B}$	I	Output Enable for 2B Port (Active LOW)

## NOTE:

- These pins have "Bus-Hold". All other pins are standard inputs, outputs, or I/Os.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition:  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$

Symbol	Parameter	Test Conditions		Min.	Typ. <sup>(1)</sup>	Max.	Unit
V <sub>IH</sub>	Input HIGH Voltage Level	V <sub>CC</sub> = 2.3V to 2.7V		1.7	—	—	V
		V <sub>CC</sub> = 2.7V to 3.6V		2	—	—	
V <sub>IL</sub>	Input LOW Voltage Level	V <sub>CC</sub> = 2.3V to 2.7V		—	—	0.7	V
		V <sub>CC</sub> = 2.7V to 3.6V		—	—	0.8	
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> = 3.6V	V <sub>I</sub> = V <sub>CC</sub>	—	—	±5	μA
I <sub>IL</sub>	Input LOW Current	V <sub>CC</sub> = 3.6V	V <sub>I</sub> = GND	—	—	±5	μA
I <sub>OZH</sub> I <sub>OZL</sub>	High Impedance Output Current (3-State Output pins)	V <sub>CC</sub> = 3.6V	V <sub>O</sub> = V <sub>CC</sub>	—	—	±10	μA
			V <sub>O</sub> = GND	—	—	±10	
V <sub>IK</sub>	Clamp Diode Voltage	V <sub>CC</sub> = 2.3V, I <sub>IN</sub> = -18mA		—	-0.7	-1.2	V
V <sub>H</sub>	Input Hysteresis	V <sub>CC</sub> = 3.3V		—	100	—	mV
I <sub>CC1</sub> I <sub>CC2</sub> I <sub>CC3</sub>	Quiescent Power Supply Current	V <sub>CC</sub> = 3.6V V <sub>IN</sub> = GND or V <sub>CC</sub>		—	0.1	40	μA
ΔI <sub>CC</sub>	Quiescent Power Supply Current Variation	One input at V <sub>CC</sub> - 0.6V, other inputs at V <sub>CC</sub> or GND		—	—	750	μA

**NOTE:**

1. Typical values are at V<sub>CC</sub> = 3.3V, +25°C ambient.

## BUS-HOLD CHARACTERISTICS

Symbol	Parameter <sup>(1)</sup>	Test Conditions		Min.	Typ. <sup>(2)</sup>	Max.	Unit
I <sub>BH1</sub> I <sub>BH2</sub>	Bus-Hold Input Sustain Current	V <sub>CC</sub> = 3V	V <sub>I</sub> = 2V	-75	—	—	μA
			V <sub>I</sub> = 0.8V	75	—	—	
I <sub>BH3</sub> I <sub>BH4</sub>	Bus-Hold Input Sustain Current	V <sub>CC</sub> = 2.3V	V <sub>I</sub> = 1.7V	-45	—	—	μA
			V <sub>I</sub> = 0.7V	45	—	—	
I <sub>BHO1</sub> I <sub>BHO2</sub>	Bus-Hold Input Overdrive Current	V <sub>CC</sub> = 3.6V	V <sub>I</sub> = 0 to 3.6V	—	—	±500	μA

**NOTES:**

1. Pins with Bus-Hold are identified in the pin description.
2. Typical values are at V<sub>CC</sub> = 3.3V, +25°C ambient.

## OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Max.	Unit
VOH	Output HIGH Voltage	VCC = 2.3V to 3.6V	IOH = - 0.1mA	VCC - 0.2	—	V
		VCC = 2.3V	IOH = - 6mA	2	—	
		VCC = 2.3V	IOH = - 12mA	1.7	—	
		VCC = 2.7V		2.2	—	
		VCC = 3V		2.4	—	
		VCC = 3V	IOH = - 24mA	2	—	
VOL	Output LOW Voltage	VCC = 2.3V to 3.6V	IOL = 0.1mA	—	0.2	V
		VCC = 2.3V	IOL = 6mA	—	0.4	
			IOL = 12mA	—	0.7	
		VCC = 2.7V	IOL = 12mA	—	0.4	
		VCC = 3V	IOL = 24mA	—	0.55	

**NOTE:**  
1. VIH and VIL must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate VCC range. TA = - 40°C to + 85°C.

## OPERATING CHARACTERISTICS, TA = 25°C

Symbol	Parameter	Test Conditions	VCC = 2.5V ± 0.2V	VCC = 3.3V ± 0.3V	Unit
			Typical	Typical	
CPD	Power Dissipation Capacitance Outputs enabled	CL = 0pF, f = 10MHz	37	41	pF
CPD	Power Dissipation Capacitance Outputs disabled		4	7	

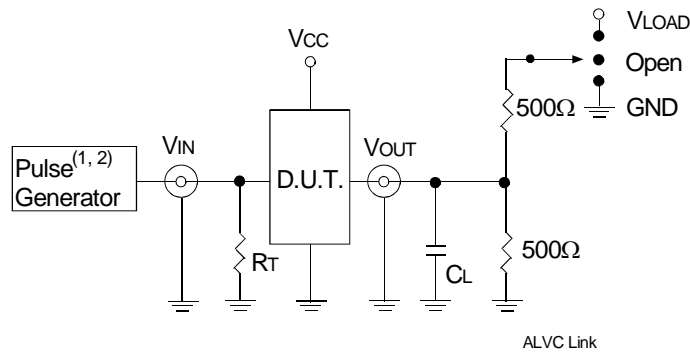
## SWITCHING CHARACTERISTICS<sup>(1)</sup>

Symbol	Parameter	VCC = 2.5V ± 0.2V		VCC = 2.7V		VCC = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
tPLH	Propagation Delay	1	5.4	—	5.1	1.2	4.3	ns
tPHL	Ax to 1Bx or Ax to 2Bx							
tPLH	Propagation Delay	1	5.4	—	5.1	1.2	4.3	ns
tPHL	1Bx to Ax or 2Bx to Ax							
tPLH	Propagation Delay	1	5.6	—	5.2	1	4.4	ns
tPHL	LEXB to Ax							
tPLH	Propagation Delay	1	5.6	—	5.2	1	4.4	ns
tPHL	LE1B to 1Bx or LEA2B to 2Bx							
tPLH	Propagation Delay	1	6.9	—	6.6	1.1	5.6	ns
tPHL	SEL to Ax							
tPZH	Output Enable Time	1	6.7	—	6.4	1	5.4	ns
tPZL	$\overline{OE}A$ to Ax, $\overline{OE}1B$ to 1Bx, or $\overline{OE}2B$ to 2Bx							
tPHZ	Output Disable Time	1	5.7	—	5	1.3	4.6	ns
tPLZ	$\overline{OE}A$ to Ax, $\overline{OE}1B$ to 1Bx, or $\overline{OE}2B$ to 2Bx							
tSU	Set-up Time, data before LE1B, LE2B, LEA1B, LEA2B	1.4	—	1.1	—	1.1	—	ns
tH	Hold Time, data after LE1B, LE2B, LEA1B, LEA2B	1.6	—	1.9	—	1.5	—	ns
tW	Pulse Width, LE1B, LE2B, LEA1B, or LEA2B HIGH	3.3	—	3.3	—	3.3	—	ns
tSK(O)	Output Skew <sup>(2)</sup>	—	—	—	—	—	500	ps

**NOTES:**  
1. See TEST CIRCUITS AND WAVEFORMS. TA = - 40°C to + 85°C.  
2. Skew between any two outputs of the same package and switching in the same direction.

TEST CIRCUITS AND WAVEFORMS  
TEST CONDITIONS

Symbol	V <sub>CC</sub> <sup>(1)</sup> =3.3V±0.3V	V <sub>CC</sub> <sup>(1)</sup> =2.7V	V <sub>CC</sub> <sup>(2)</sup> =2.5V±0.2V	Unit
V <sub>LOAD</sub>	6	6	2 x V <sub>CC</sub>	V
V <sub>IH</sub>	2.7	2.7	V <sub>CC</sub>	V
V <sub>T</sub>	1.5	1.5	V <sub>CC</sub> / 2	V
V <sub>LZ</sub>	300	300	150	mV
V <sub>HZ</sub>	300	300	150	mV
CL	50	50	30	pF



Test Circuit for All Outputs

DEFINITIONS:

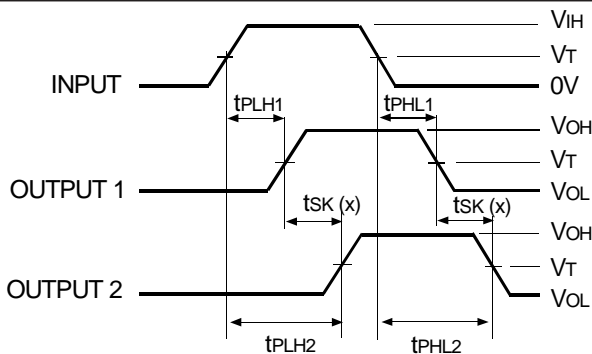
CL = Load capacitance: includes jig and probe capacitance.  
RT = Termination resistance: should be equal to Z<sub>out</sub> of the Pulse Generator.

NOTES:

1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t<sub>r</sub> ≤ 2.5ns; t<sub>r</sub> ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t<sub>r</sub> ≤ 2ns; t<sub>r</sub> ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V <sub>LOAD</sub>
Disable High Enable High	GND
All Other Tests	Open

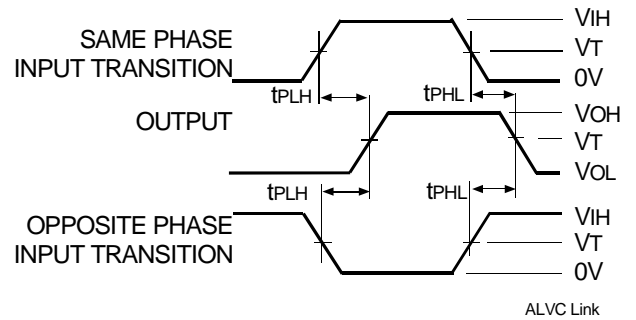


$$tsk(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

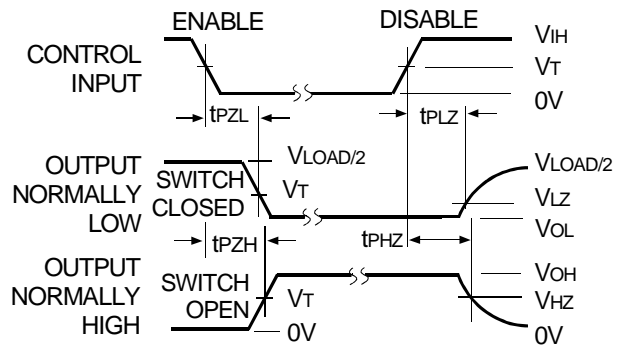
Output Skew - tsk(x)

NOTES:

1. For tsk(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For tsk(b) OUTPUT1 and OUTPUT2 are in the same bank.



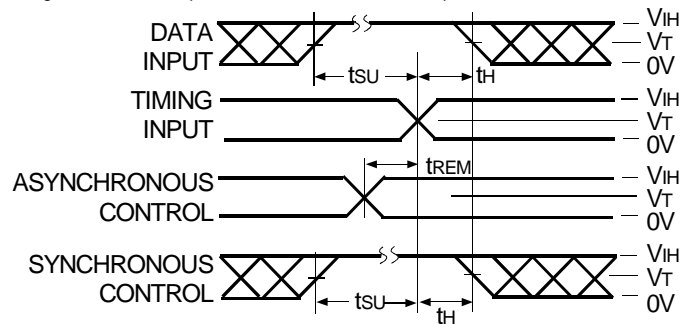
Propagation Delay



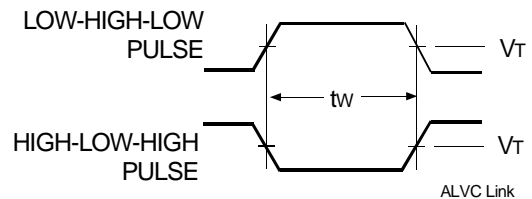
Enable and Disable Times

NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

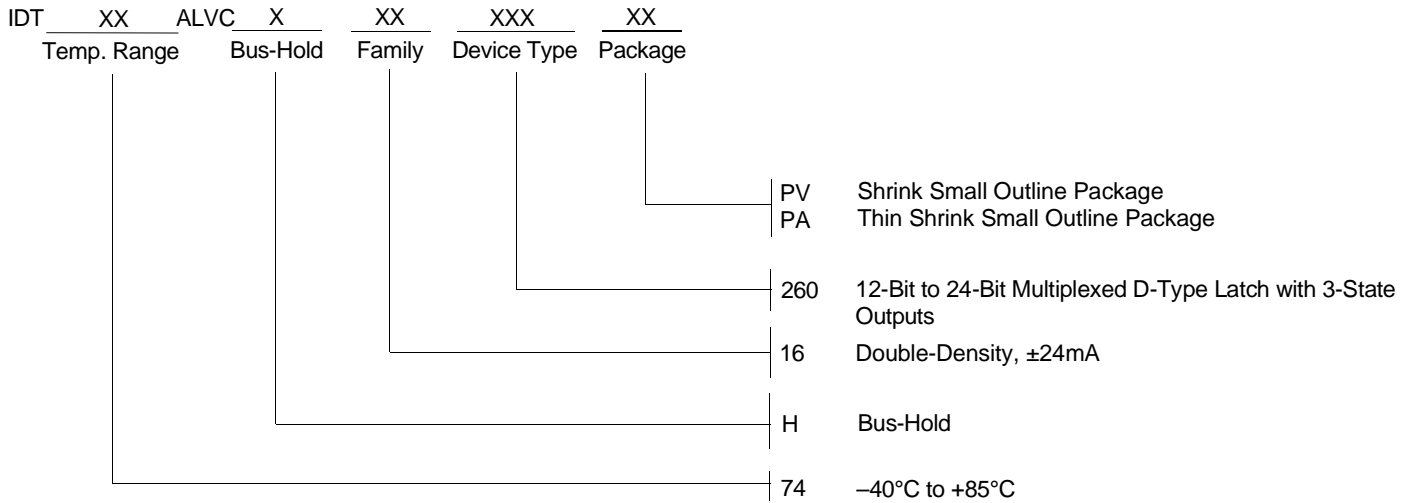


Set-up, Hold, and Release Times



Pulse Width

## ORDERING INFORMATION



**CORPORATE HEADQUARTERS**  
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