Addendum

MPC860UMAD
Rev. 2.4, 4/2004

Errata to the MPC860 PowerQUICC™ Family User's Manual, Rev. 2

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This errata describes corrections to Revision 2 of the *MPC860 PowerQUICC™ Family User's Manual* (Order No. MPC860UM, Rev. 2).

The MPC860 is a PowerPC™ architecture-based quad integrated communications controller (PowerQUICC™). The CPU on the MPC860 is the MPC8xx core, a 32-bit microprocessor that implements the PowerPC architecture, incorporating memory management units (MMUs) and instruction and data caches.

1 Document Revision History

Table 1 provides a revision history for this document.

Table 1. Document Revision History

Rev. No.	Substantive Change(s)
2.2	Added new errata items from Section 12.5 (page 12-27), Section 27.8 (page 27-13, 27-14), Section 27.22 (page 27-29), Section 31.4.1.2 (page 30-9, 30-10), and Section 34.2.1 (page 34-4).
2.3	Added new errata item from Section 32.4.3 (page 32-8).
2.4	Added new errata items for Section 22 (page 22-1), Section 22.16 (page 22-15), Section 31.4.1.2 (page 30-9), and Section B.3.1 (page B-4)

2 Document Errata

The section and page numbers of new errata items added since the last errata addendum are boldfaced.

Section/Page	Changes
12.5, 12-27	In the second row of Table 12-5, add a footnote at the end of the sentence that states: At power-on reset, port pin states are not defined in any particular state until CLKOUT is present for two clocks.
22, 22-1	The last sentence in the last paragraph should be removed.
22.16, 22-15	In the RZS field (bit 7) of Table 22-9, for selection 1, the second sentence in the paragraph (making reference to V.14 applications) should be removed.

Section, Page No.	Changes
27.8, 27-13	Add superscript number 2 after PADDR1_H, PADDR1_M, and PADDR1_L.
27.8, 27-14	Add superscript number 2 after TADDR_H, TADDR_M, and TADDR_L. At the end of Table 27-1, add a note with the following statement: The address should be written in little endian, not Motorola's big-endian format (that is, physical address 112233445566 should be written PADDR_L = 6655, PADDR_M = 4433, and PADDR_H = 2211. The TADDR should be written in the same way as the PADDR).
27.22, 27-29	Change the last sentence in step 26 to read, "Then write 0x000E to TxBD[Data..."
30.4.1.2, 30-9	In the last sentence of example 1, change the order of the string for REV = 1 to the following: first j_klmn__r_stuv last Also, on all three examples, tab last and lsb to the right so that they do not appear to be part of the string.
30.4.1.2, 30-10	In the last sentence of example 3, change the order of the string for REV = 1 to the following: first r_stuv_ghij_klmn last
32.4.3, 32-8	In Table 31-3, replace the text in the description with the following: Division ratio 0–7. Specifies the divide ratio of the BRG divider in the I^2C clock generator. The output of the prescalar is divided by $2 \times (DIV + 3 + (2 \times FLT))$, and the clock has a 50% duty cycle. The FLT bit is in the I2MOD register. The minimum value for DIV is 3 if the digital filter is disabled (FLT = 0) and 6 if the digital filter is enabled (FLT = 1).
33.1, 33-2	Add a footnote reference number at the end of the statement of the sixth bullet with the following footnote: At power-on reset, port pin states are not defined in any particular state until CLKOUT is present for two clocks.
34.2.1, 34-4	The first bullet should reference SPS = 0, and the second bullet should reference SPS = 1.
43.2.12, 43-10	Change the term '60x' in the first and fourth sentences to 'external.'
B.3.1, B-4	In Table B-1, the row making reference to SCC in Profibus (seventeenth row) should be removed.

Section, Page No.	Changes

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