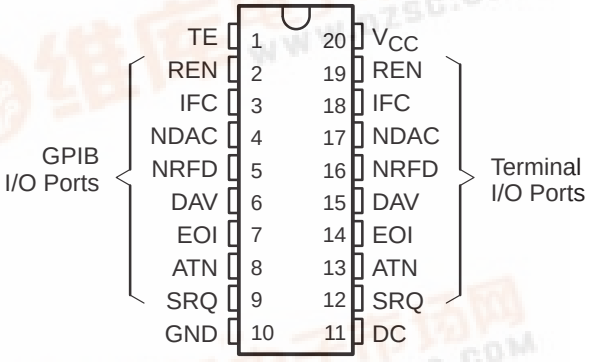
OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVERS

SLLS019E – JUNE 1986 – REVISED NOVEMBER 1999

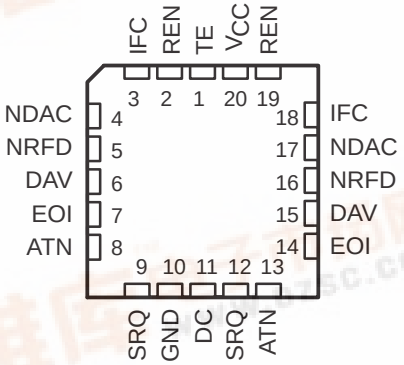
SUITABLE FOR IEEE STANDARD 488-1978 (GPIB)†

- 8-Channel Bidirectional Transceivers
- Designed to Implement Control Bus Interface
- Designed for Single Controller
- High-Speed Advanced Low-Power Schottky Circuitry
- Low Power Dissipation:
  - SN55ALS161 . . . 59 mW Max Per Channel
  - SN75ALS161 . . . 46 mW Max Per Channel
- Fast Propagation Times:
  - SN55ALS161 . . . 25 ns Max
  - SN75ALS161 . . . 20 ns Max
- High-Impedance pnp Inputs
- Receiver Hysteresis:
  - SN55ALS161 . . . 550 mV Typ
  - SN75ALS161 . . . 650 mV Typ
- Bus-Terminating Resistors Provided on Driver Outputs
- No Loading of Bus When Device Is Powered Down (V_{CC} = 0)
- Power-Up/Power-Down Protection (Glitch Free)

SN55ALS161 . . . J OR W PACKAGE
SN75ALS161 . . . DW OR N PACKAGE
(TOP VIEW)



SN55ALS161 . . . FK PACKAGE
(TOP VIEW)



description

The SN55ALS161 and SN75ALS161 eight-channel general-purpose interface bus transceivers are high-speed, advanced low-power Schottky-process devices designed to provide the bus-management and data-transfer signals between operating units of a single-controller instrumentation system. When combined with the SN55ALS160 and SN75ALS160 octal bus transceivers, these devices provide a complete 16-wire interface for the IEEE 488 bus.

The SN55ALS161 and SN75ALS161 devices feature eight driver-receiver pairs connected in a front-to-back configuration to form input/output (I/O) ports at both the bus and terminal sides. The direction of data through these driver-receiver pairs is determined by the direction-control (DC) and talk-enable (TE) signals.

CHANNEL-IDENTIFICATION TABLE

NAME	IDENTITY	CLASS
DC	Direction Control	Control
TE	Talk Enable	
ATN	Attention	Bus Management
SRQ	Service Request	
REN	Remote Enable	
IFC	Interface Clear	
EOI	End or Identify	
DAV	Data Valid	Data Transfer
NDAC	Not Data Accepted	
NRFD	Not Ready for Data	

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

† The transceivers are suitable for IEEE Standard 488 applications to the extent of the operating conditions and characteristics specified in this data sheet. Certain limits contained in the IEEE specification are not met or cannot be tested over the entire military temperature range.

description (continued)

The driver outputs general-purpose interface bus (GPIB I/O ports) feature active bus-terminating resistor circuits designed to provide a high impedance to the bus when V_{CC} = 0. The drivers are designed to handle sink-current loads up to 48 mA. Each receiver features pnp transistor inputs for high input impedance and hysteresis of 400 mV on the commercial part, 250 mV on the military part, minimum, for increased noise immunity. All receivers have 3-state outputs to present a high impedance to the terminal when disabled.

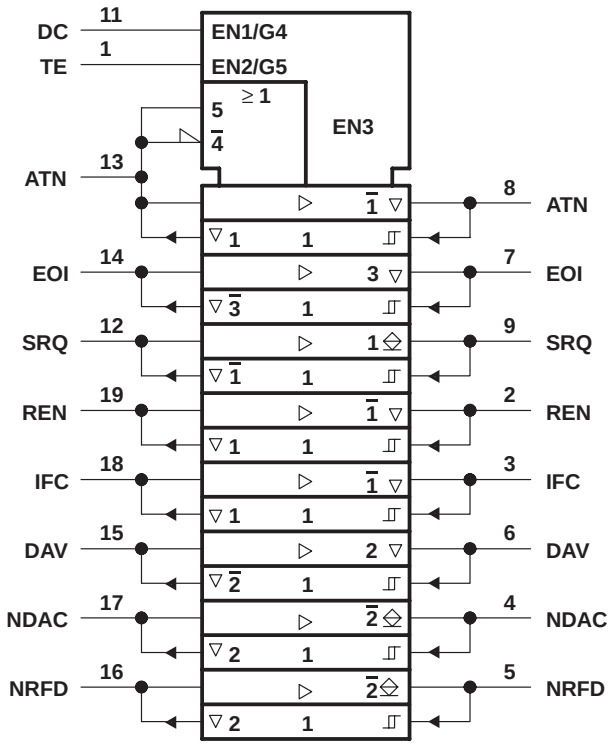
The SN55ALS161 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN75ALS161 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
RECEIVE/TRANSMIT

CONTROLS			BUS-MANAGEMENT CHANNELS					DATA-TRANSFER CHANNELS		
DC	TE	ATN†	ATN† (CONTROLLED BY DC)	SRQ (CONTROLLED BY DC)	REN (CONTROLLED BY DC)	IFC (CONTROLLED BY DC)	EOI	DAV (CONTROLLED BY TE)	NDAC (CONTROLLED BY TE)	NRFD (CONTROLLED BY TE)
H	H	H	R	T	R	R	T	T	R	R
H	H	L					R			
L	L	H	T	R	T	T	R	R	T	T
L	L	L					T			
H	L	X	R	T	R	R	R	R	T	T
L	H	X	T	R	T	T	T	T	R	R

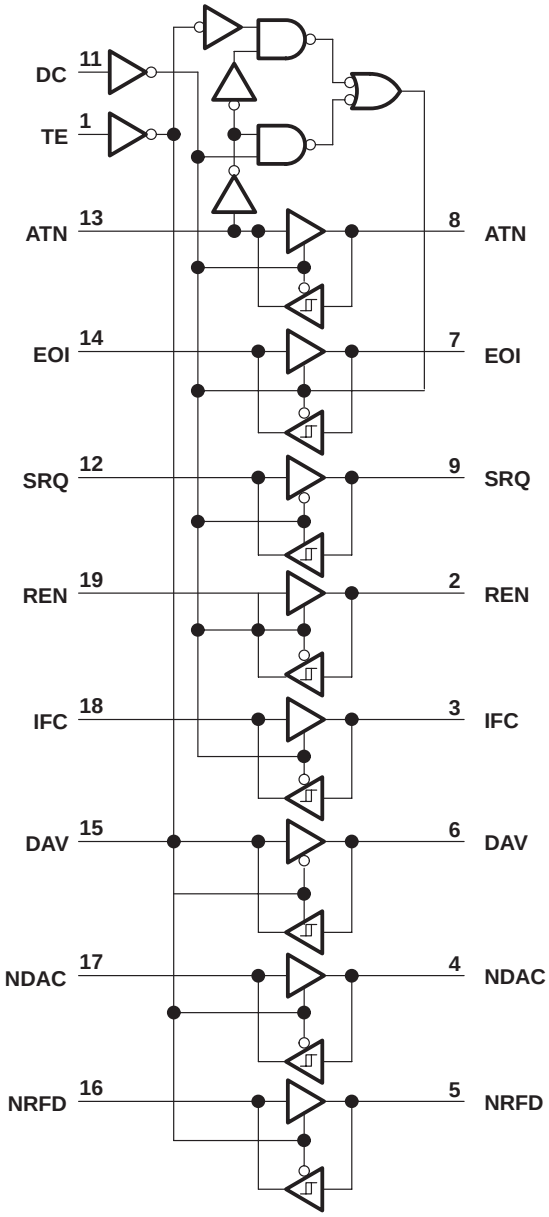
H = high level, L = low level, R = receive, T = transmit, X = irrelevant
Direction of data transmission is from the terminal side to the bus side, and the direction of data receiving is from the bus side to the terminal side.
Data transfer is noninverting in both directions.
† ATN is a normal transceiver channel that functions additionally as an internal direction control or talk enable for EOI whenever the DC and TE inputs are in the same state. When DC and TE are in opposite states, the ATN channel functions as an independent transceiver only.

logic symbol†



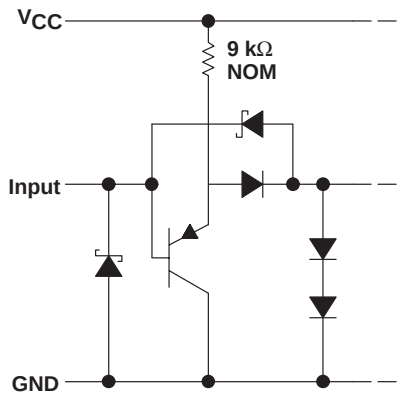
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

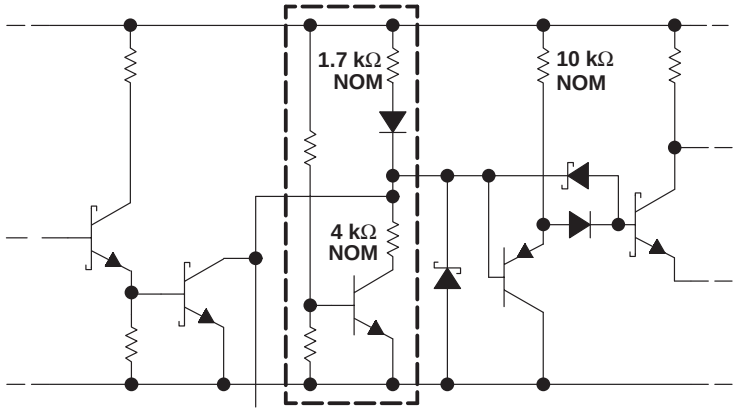


schematics of inputs and outputs

EQUIVALENT OF ALL CONTROL INPUTS

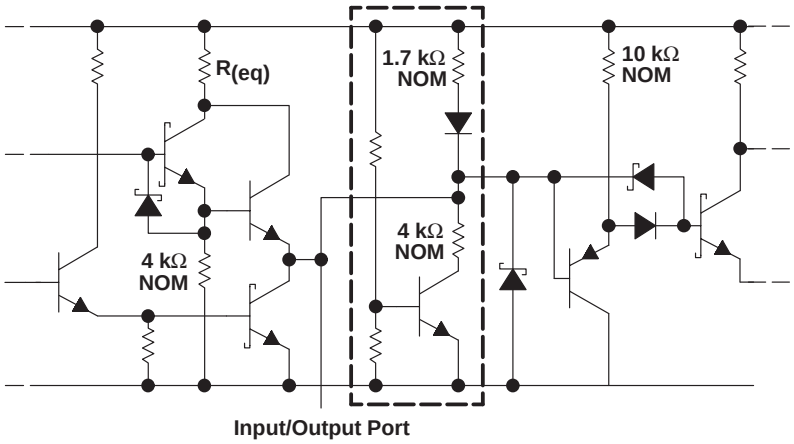


TYPICAL OF SRQ, NDAC, AND NRFD GPIB I/O PORT



Circuit inside dashed lines is on the driver outputs only.

TYPICAL OF ALL I/O PORTS EXCEPT SRQ, NDAC, NRFD GPIB I/O PORTS



Driver output $R_{(eq)}$ = 30 Ω NOM
Receiver output $R_{(eq)}$ = 110 Ω NOM
$R_{(eq)}$ = equivalent resistor
Circuit inside dashed lines is on the driver outputs only.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, V_I . . . . . 5.5 V
Low-level driver output current, I_{OL} . . . . . 100 mA
Continuous total dissipation . . . . . See Dissipation Rating Table
Package thermal impedance, θ_{JA} (see Note 2): DW package . . . . . 58°C/W
N package . . . . . 69°C/W
Case temperature for 60 seconds: FK package, T_C . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from the case for 60 seconds: J or W package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds: DW or N package . . . . . 260°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to network ground terminal.
2. The package thermal impedance is calculated in accordance with JESD 51.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	OPERATING FACTOR	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	275 mW
W	1000 mW	8.0 mW/°C	640 mW	200 mW

SN55ALS161 recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}	TE and DC at T_A = –55°C to 125°C	2			V
	Bus and terminal at T_A = 25°C to 125°C	2			
	Bus and terminal at T_A = –55°C	2.1			
Low-level input voltage, V_{IL}	TE and DC at T_A = –55°C to 125°C			0.8	V
	Bus and terminal at T_A = 25°C to –55°C			0.8	
	Bus and terminal at T_A = 125°C			0.7	
High-level output current, I_{OH}	Bus ports with pullups active (V_{CC} = 5 V)			–5.2	mA
	Terminal ports			–800	µA
Low-level output current, I_{OL}	Bus ports			48	mA
	Terminal ports			16	
Operating free-air temperature, T_A		–55		125	°C

SN75ALS161 recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}	Bus ports with pullups active			–5.2	mA
	Terminal ports			–800	µA
Low-level output current, I_{OL}	Bus ports			48	mA
	Terminal ports			16	
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS†			SN55ALS161			SN75ALS161			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	Input clamp voltage		I_I = –18 mA				–0.8	–1.5		–0.8	–1.5	V
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)	Bus							0.4	0.65		V
		Bus	V_{CC} = 5 V,	T_A = –55°C and 25°C		0.4	0.55					
			V_{CC} = 5 V,	T_A = 125°C		0.25						
V_{OH}§	High-level output voltage	Terminal	I_{OH} = – 800 µA,	V_{CC} = MIN	T_A = 25°C and MAX	2.7	3.5		2.7	3.5		V
					T_A = MIN	2.5	3.5		2.7	3.5		
		Bus	I_{OH} = – 5.2 mA,	V_{CC} = MIN	T_A = 25°C and MAX	2.2			2.2			
					T_A = MIN	2.0			2.2			
V_{OL}	Low-level output voltage	Terminal	I_{OL} = 16 mA,	V_{CC} = MIN			0.3	0.5		0.3	0.5	V
		Bus	I_{OL} = 48 mA¶,	V_{CC} = MIN			0.35	0.5		0.35	0.5	
I_I	Input current at maximum input voltage	Terminal	V_I = 5.5 V,	V_{CC} = MAX			0.2	100		0.2	100	µA
I_{IH}	High-level input current	Terminal and control inputs	V_I = 2.7 V,	V_{CC} = MAX			0.1	20		0.1	20	µA
I_{IL}	Low-level input current		V_I = 0.5 V,	V_{CC} = MAX			–30	–100		–10	–100	µA
$V_{I/O}$	Voltage at GPIB I/O port		Driver disabled, V_{CC} = 5 V (SN55')	$I_{I(bus)}$ = 0		2.5	3	3.7	2.5	3	3.7	V
				$I_{I(bus)}$ = –12 mA				–1.5			–1.5	
$I_{I/O}$	Current into GPIB I/O port	Power on	Driver disabled, V_{CC} = 5 V (SN55')	$V_{I(bus)}$ = –1.5 V to 0.4 V		–1.3			–1.3			mA
				$V_{I(bus)}$ = 0.4 V to 2.5 V		0		–3.2	0		–3.2	
				$V_{I(bus)}$ = 2.5 V to 3.7 V				2.5 –3.2			2.5 –3.2	
				$V_{I(bus)}$ = 3.7 V to 5 V		0		2.5	0		2.5	
				$V_{I(bus)}$ = 5 V to 5.5 V		0.7		2.5	0.7		2.5	
		Power off	V_{CC} = 0	$V_{I(bus)}$ = 0 to 2.5 V				40			40	µA
I_{OS}§	Short-circuit output current	Terminal	V_{CC} = MAX			–15	–35	–75	–15	–35	–75	mA
		Bus				–25	–50	–125	–25	–50	–125	
I_{CC}	Supply current		No load,	TE and DC low, V_{CC} = MAX			55	90		55	75	mA
$C_{I/O}$	GPIB I/O port capacitance		V_{CC} = 0 to 5 V,	$V_{I/O}$ = 0 to 2 V, f = 1 MHz			30			30		pF

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ V_{OH} and I_{OS} apply to 3-state outputs only.
¶ For SN55', I_{OL} = 24 mA at –55°C.

SN55ALS161 switching characteristics, V_{CC} = 5 V and C_L = 50 pF (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A†	MIN	TYP‡	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	Terminal	Bus (Except SRQ, NDAC, and NRFD)	See Figure 1	25°C		10	17	ns
					Full range			20	
t_{PHL}	Propagation delay time, high- to low-level output				25°C		10	14	
					Full range			18	
t_{PLH}	Propagation delay time, low- to high-level output	Terminal	Bus (NRFD, SRQ, NDAC)	See Figure 2	25°C			25	ns
					Full range			37	
t_{PHL}	Propagation delay time, high- to low-level output				25°C		10	14	
					Full range			19	
t_{PLH}	Propagation delay time, low- to high-level output	Bus	Terminal	See Figure 2	25°C		10	15	ns
					Full range			22	
t_{PHL}	Propagation delay time, high- to low-level output				25°C		10	15	
					Full range			24	
t_{PZH}	Output enable time to high level	TE or DC	Bus (ATN, REN, IFC, and DAV)	See Figure 3	25°C		20	30	ns
					Full range			52	
t_{PHZ}	Output disable time from high level				25°C		8	14	
					Full range			18	
t_{PZL}	Output enable time to low level				25°C		16	28	
					Full range			44	
t_{PLZ}	Output disable time from low level				25°C		10	19	
					Full range			30	
t_{PZH}	Output enable time to high level	TE or DC	Bus (EOI)	See Figure 3	25°C		24	30	ns
					Full range			64	
t_{PHZ}	Output disable time from high level				25°C		13	19	
					Full range			30	
t_{PZL}	Output enable time to low level,				25°C		21	35	
					Full range			54	
t_{PLZ}	Output disable time from low level				25°C		13	20	
					Full range			40	
t_{PZH}	Output enable time to high level	TE or DC	Terminal	See Figure 4	25°C		24	36	ns
					Full range			70	
t_{PHZ}	Output disable time from high level				25°C		12	20	
					Full range			40	
t_{PZL}	Output enable time to low level				25°C		20	34	
					Full range			56	
t_{PLZ}	Output disable time from low level				25°C		13	24	
					Full range			43	

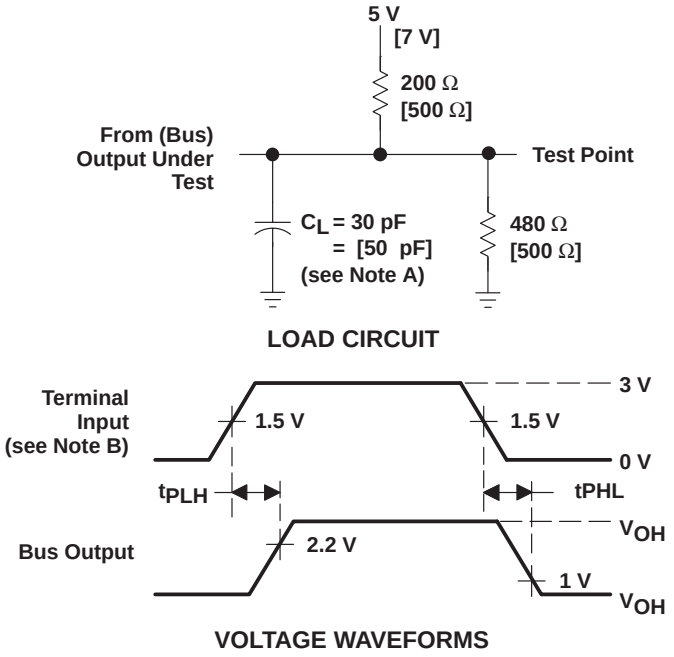
† Full range is –55°C to 125°C.
‡ All typical values are at V_{CC} = 5 V.

SN75ALS161 switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	Terminal	Bus	C_L = 30 pF, See Figure 1		10	20	ns
t_{PHL}	Propagation delay time, high- to low-level output					12	20	
t_{PLH}	Propagation delay time, low- to high-level output	Bus	Terminal	C_L = 30 pF, See Figure 2		5	10	ns
t_{PHL}	Propagation delay time, high- to low-level output					7	14	
t_{PZH}	Output enable time to high level	TE or DC	Bus (ATN, EOI, REN, IFC, and DAV)	C_L = 15 pF, See Figure 3			30	ns
t_{PHZ}	Output disable time from high level						20	
t_{PZL}	Output enable time to low level						45	
t_{PLZ}	Output disable time from low level						20	
t_{PZH}	Output enable time to high level	TE or DC	Terminal	C_L = 15 pF, See Figure 4			30	ns
t_{PHZ}	Output disable time from high level						25	
t_{PZL}	Output enable time to low level						30	
t_{PLZ}	Output disable time from low level						25	

† All typical values are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION



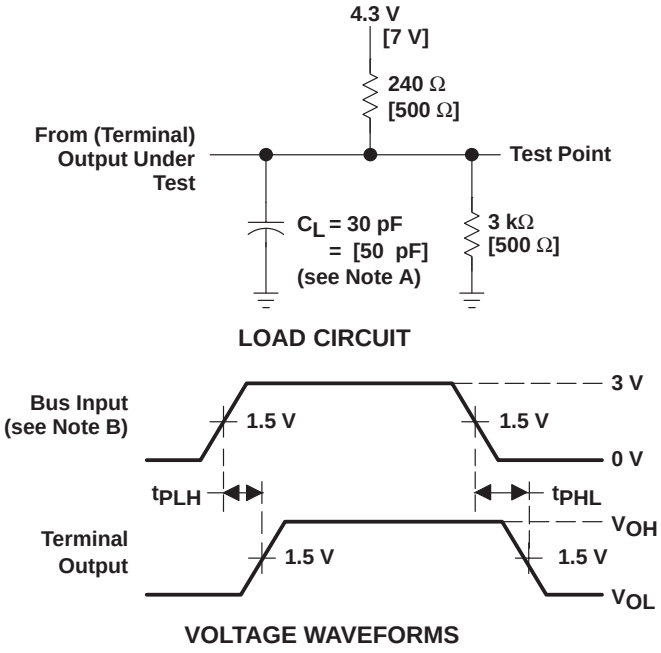
[ ] denotes the SN55ALS161 military test conditions.

NOTES: A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

Figure 1. Terminal-to-Bus Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



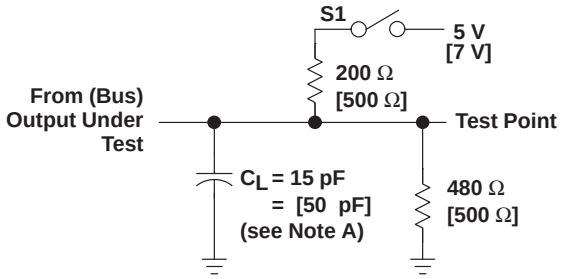
[ ] denotes the SN55ALS161 military test conditions.

NOTES: A. C_L includes probe and jig capacitance.

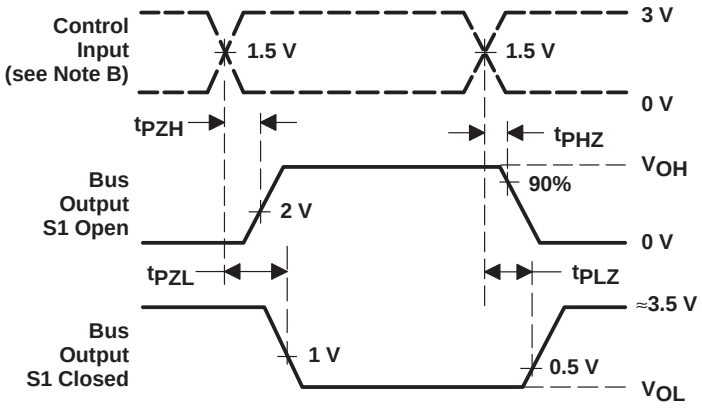
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

Figure 2. Bus-to-Terminal Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

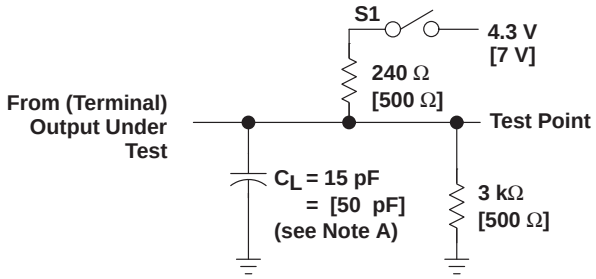
[ ] denotes the SN55ALS161 military test conditions.

NOTES: A. C_L includes probe and jig capacitance.

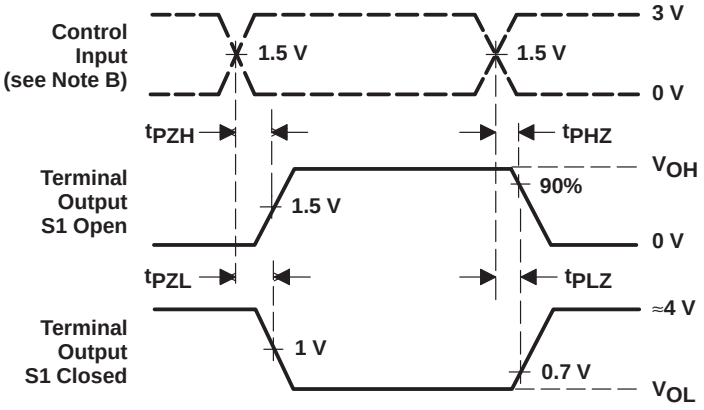
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

Figure 3. Bus Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

[ ] denotes the SN55ALS161 military test conditions.

NOTES: A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

Figure 4. Terminal Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS†

**TERMINAL I/O PORTS
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT**

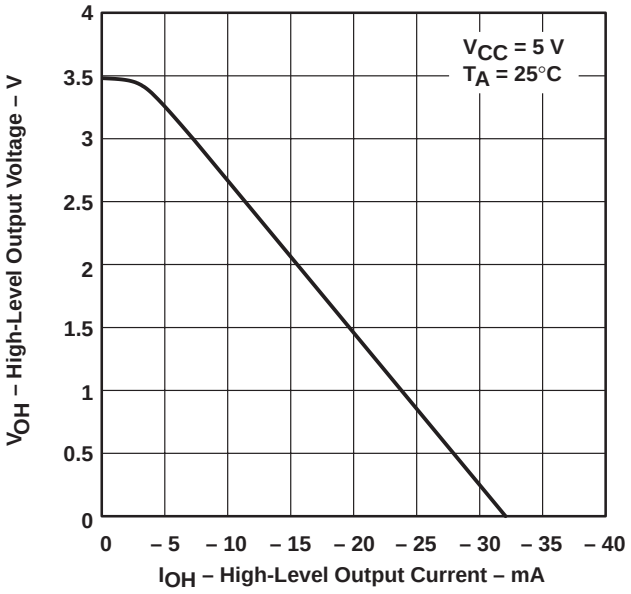


Figure 5

**TERMINAL I/O PORTS
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT**

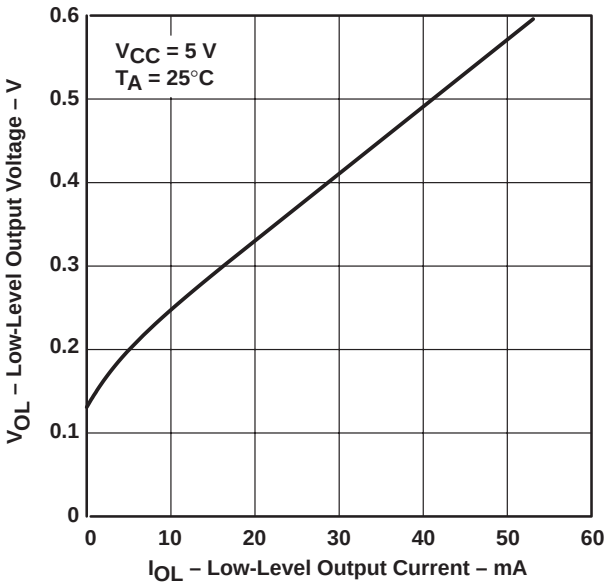


Figure 6

**TERMINAL OUTPUT VOLTAGE
vs
BUS INPUT VOLTAGE**

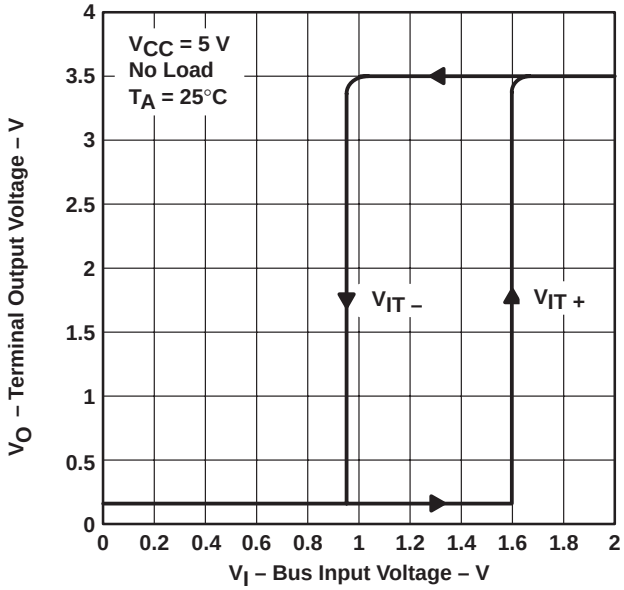


Figure 7

† Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

TYPICAL CHARACTERISTICS†

**GPIB I/O BUS
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT**

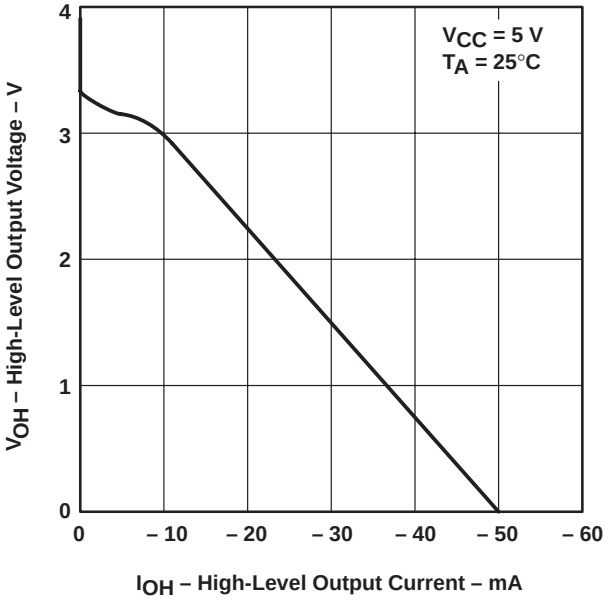


Figure 8

**GPIB I/O BUS
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT**

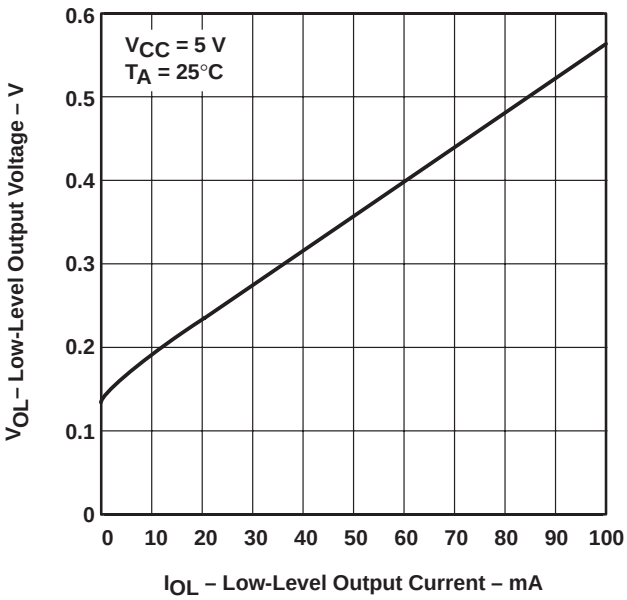


Figure 9

**BUS OUTPUT VOLTAGE
vs
TERMINAL INPUT VOLTAGE**

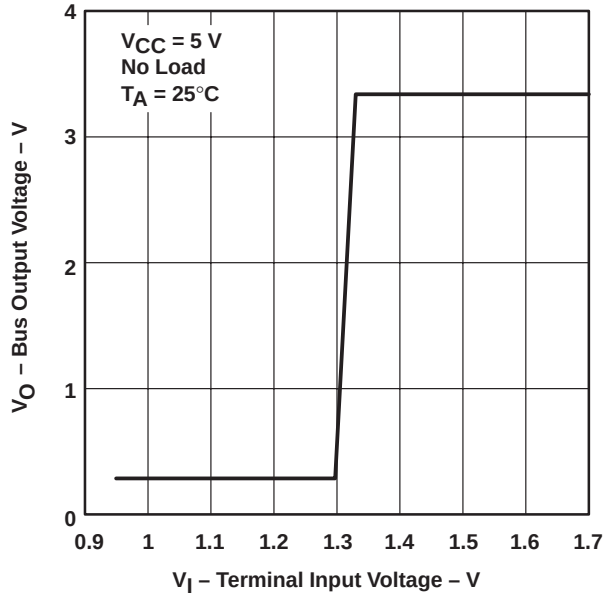


Figure 10

**GPIB I/O BUS
CURRENT
vs
VOLTAGE**

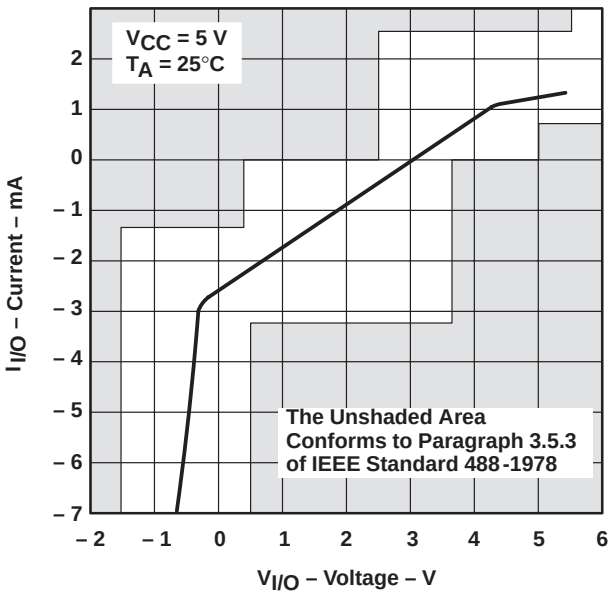


Figure 11

† Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

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