OKI semiconductor

MSM6240

DOT MATRIX LCD CONTROLLER

GENERAL DESCRIPTION

The OKI MSM6240GS is a CMOS Si-gate LSI to control large size dot matrix LCD in characters and graphics.

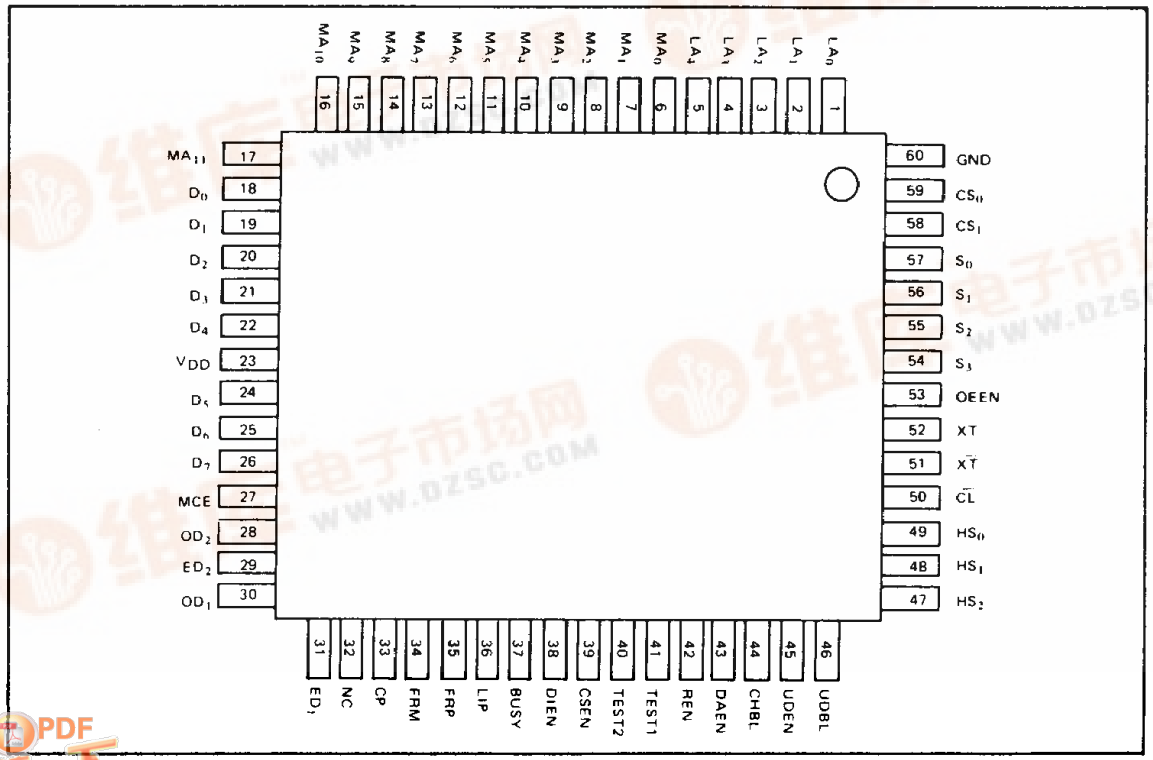
Three kinds of display modes are provided; Semi-graphic mode, Full-graphic mode and Character mode.

FEATURES

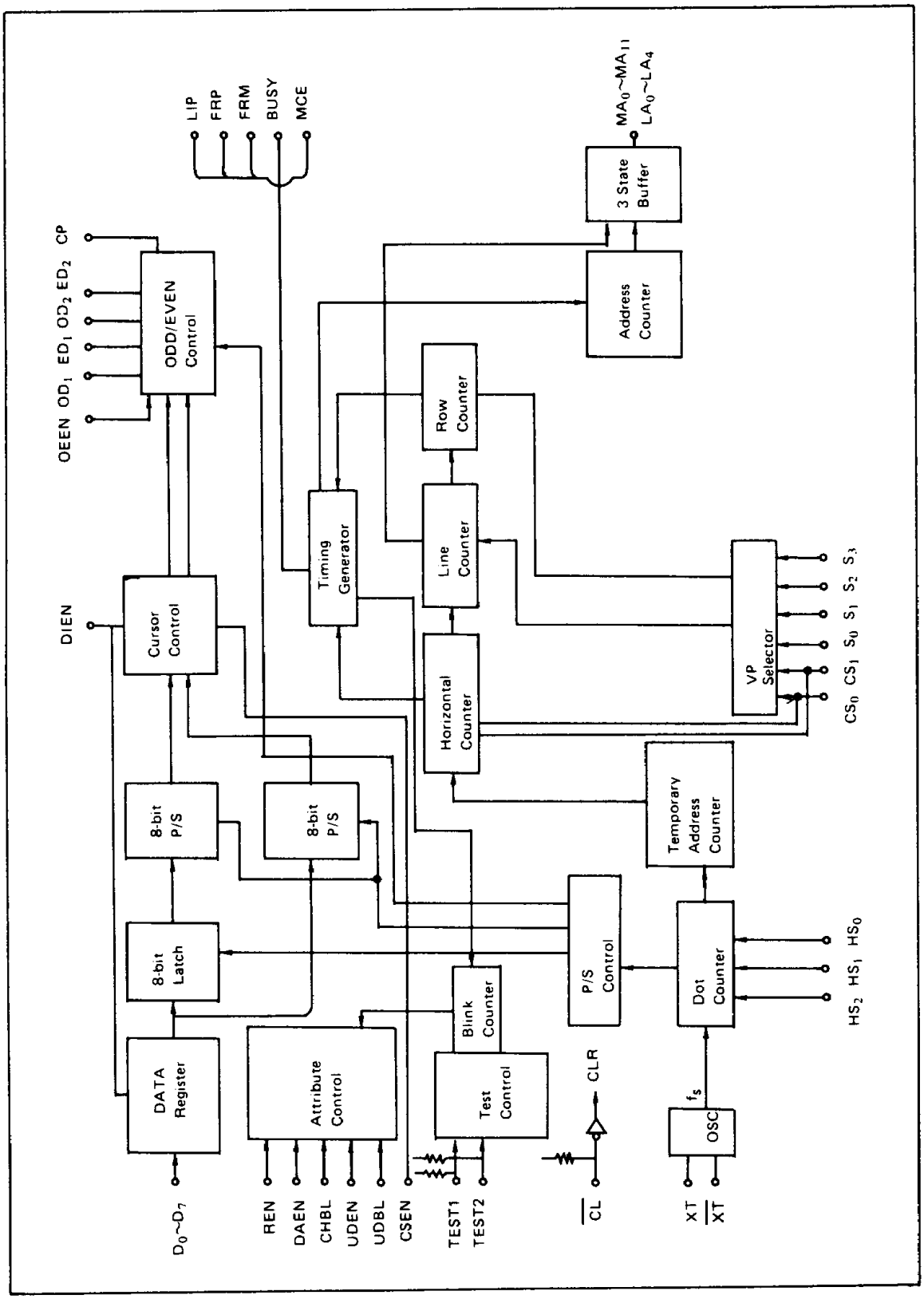
- Number of characters: 32, 40, 64 and 80/line
- Number of lines: 4 X 2, 6 X 2, 8 X 2 and 16 X 2
- Font composition (vertical): 8, 12, 18 and 20; hereinafter called VP (vertical pitch)
- Font composition (horizontal): 5, 6, 7, 8, 10, 12, 14 and 16; hereinafter called HP (horizontal pitch)
- Address: Straight binary
- Attribute
  1) Display inversion
  2) Display blank
  3) Cursor display
  4) Character blink
  5) Cursor blink
- Applicable LCD duty: 1/32, 1/48, 1/64, 1/72, 1/80, 1/96, 1/108, 1/128, 1/144
- Low power CMOS Silicon gate technology
- Single +5V power supply.
- 60 pin plastic QFP (QFP60-P-1519-K)

PIN CONFIGURATION

(Top view) 60 pin plastic QFP



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Condition	Limits	Unit
Power supply voltage	V_{DD}	T_a = 25°C	−0.3 ~ 6.0	V
Input voltage	V_{IN}	T_a = 25°C	−0.3 ~ V_{DD}	V
Storage temperature	T_{stg}	—	−50 ~ 150	°C

OPERATING RANGE

Parameter	Symbol	Condition	Limits	Unit
Power supply voltage	V_{DD}	—	4.5 ~ 5.5	V
Operating temperature	T_{op}	—	−20 ~ 85	°C

INPUT CHARACTERISTICS

(V_{DD} = 5V ± 10%, T_a = 25°C)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit	Applicable pin
"H" Input voltage	V_{IH}	—	2.4	–	–	V	D_0 ~ D_7, REN, DAEN, CHBL, CSEN, UDEN, UDBL, DIEN
"L" Input voltage	V_{IL}	—	–	–	0.8	V	
"H" Input voltage	V_{IH}	—	3.6	–	–	V	HS_0 ~ HS_2, CS_0, CS_1, S_0 ~ S_3, OEEN
"L" Input voltage	V_{IL}	—	–	–	1.0	V	
"H" Input current	I_{IH}	—	–	–	−1	μA	D_0 ~ D_7, REN, DAEN, CHBL, CSEN, UDEN, UDBL, FS, DIEN, HS_0 ~ HS_2, CS_0, CS_1, S_0 ~ S_3, OEEN
"L" Input current	I_{IL}	—	–	–	1	μA	
"H" Input current	I_{IH}	—	–	–	−1	μA	TEST1 ~ TEST3
"L" Input current	I_{IL}	—	–	500		μA	
"H" Input current	I_{IH}	—	–	–	−1	μA	$\overline{CL}$
"L" Input current	I_{IL}	—	–	50		μA	

OUTPUT CHARACTERISTICS

(V_{DD} = 5V ± 10%, Ta = 25°C)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit	Applicable pin
"H" Output current	I_{OH}	V_{OH} = 2.8V	−500	–	–	μA	MA_0 ~ MA_{11}, LA_0 ~ LA_4, OD_1, ED_1, OD_2, ED_2, CP, BUSY, FRM, FRP, MCE, LIP
"L" Output current	I_{OL}	V_{OL} = 0.4V	2.1	–	–	mA	

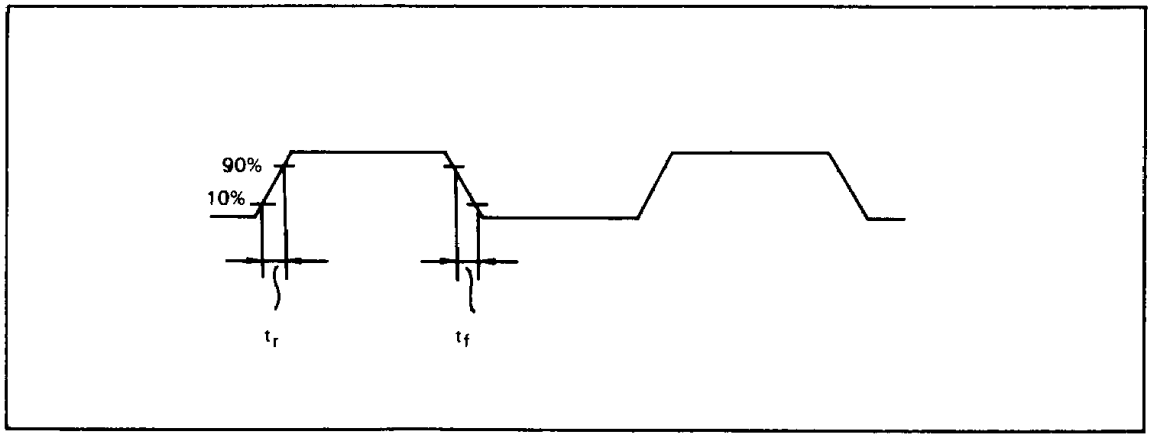
POWER CONSUMPTION

(Ta = 25°C)

Parameter	Symbol	V_{DD}	Condition	MIN	TYP	MAX	Unit	
Static current	I_{DDS}	5	f_{OSC} = 0 Hz	—	—	50	μA	No load
Operating current	I_{DD}	5	f_{OSC} = 10 MHz	—	—	14	mA	No load
Operating current	I_{DD}	5	f_{OSC} = 4 MHz	—	—	7	mA	No load

SWITCHING CHARACTERISTICS

(V_{DD} = 5V ± 10%)



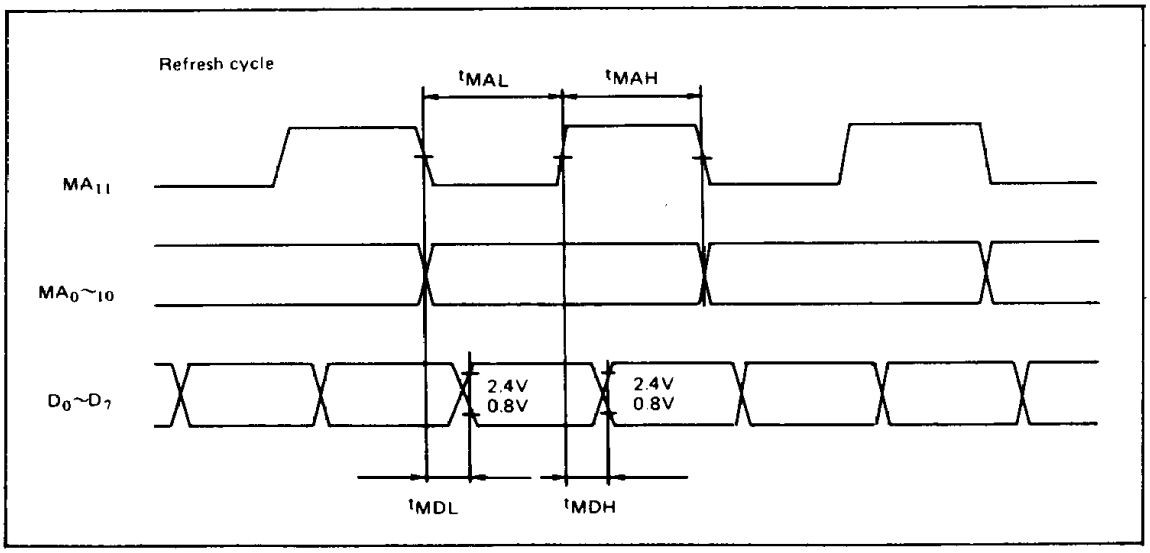
Parameter	Symbol	Load condition	MIN	TYP	MAX	Unit	Applicable terminal
Clock pulse Rise and fall time	t_r	CL = 150PF	–	–	100	ns	All output terminals
	t_f	CL = 150PF	–	–	100	ns	

MAXIMUM OPERATING FREQUENCY

(V_{DD} = 5V ± 10%)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Oscillation frequency	f_{osc}	—	10	–	–	MHz

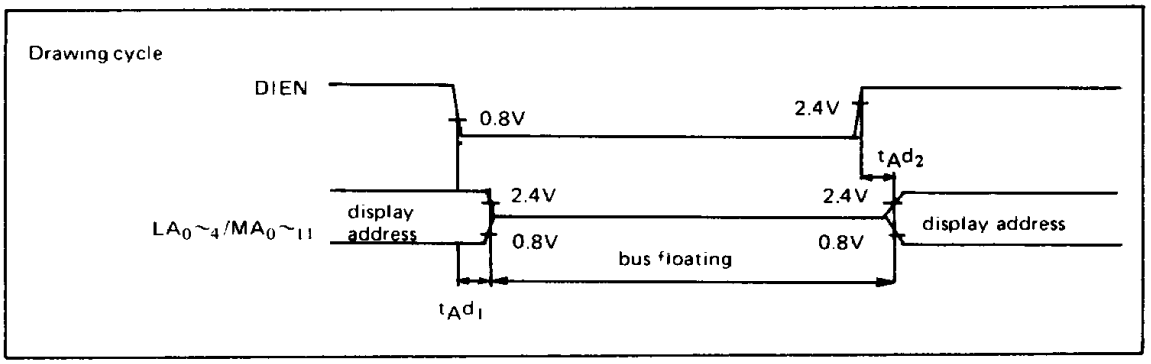
INTERFACE WITH EXTERNAL RAM, ROM



(C_L = 80pF)

Parameter	Symbol	MIN	TYP	MAX	Unit
Memory address time to the upper part	t_{MAL}	500	–	–	ns
Memory address time to the lower part	t_{MAH}	500	–	–	ns
Memory data delay time of the upper part	t_{MDL}	–	–	t_{MAL}-70	ns
Memory data delay time of the lower part	t_{MDH}	–	–	t_{MAH}-70	ns

Note: t_{MAL} and t_{MAH} is calculated by the following formula.
$t_{MAL} = t_{MAH} = 2/f_{osc} \times HP/2$
t_{MAL} and t_{MAH} become the minimum speed when HP is set at 5 and f_{osc} is 5MHz.

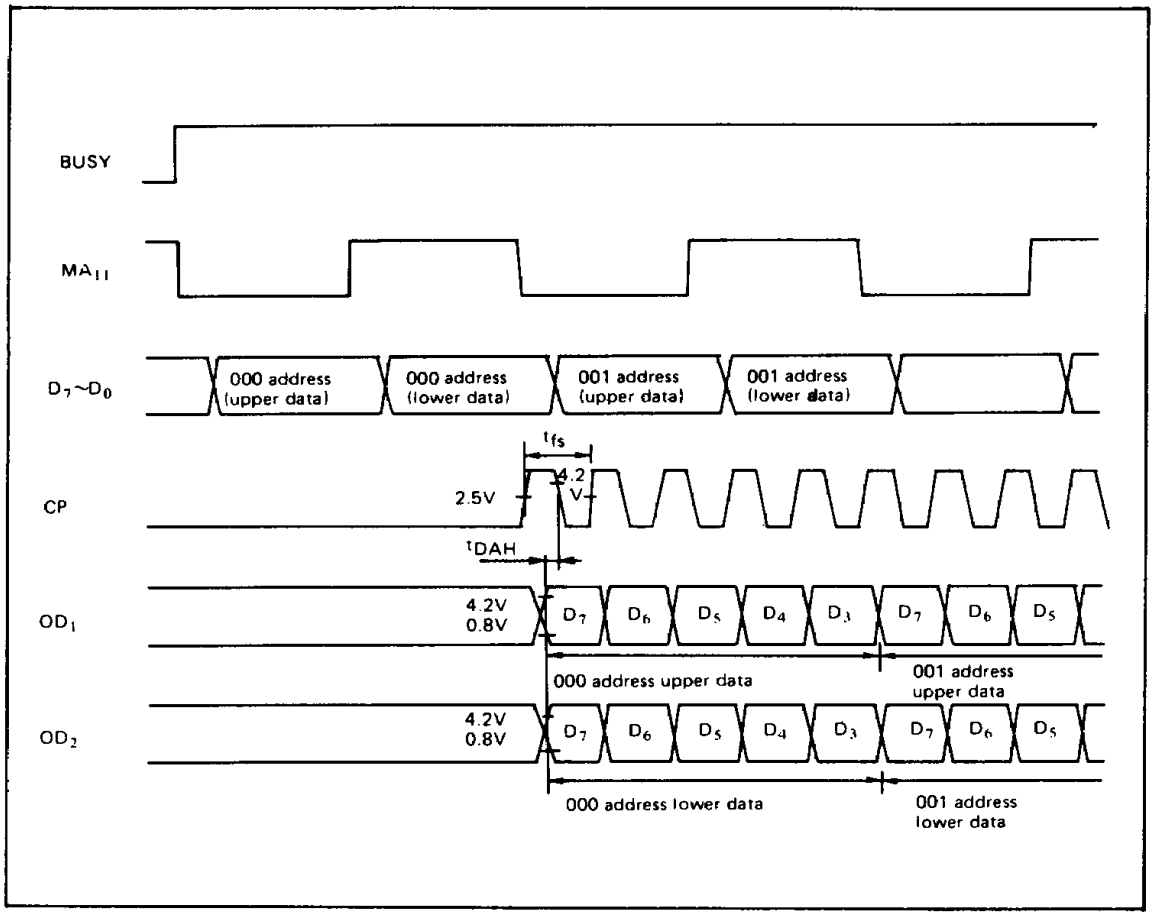


(CL = 150pF)

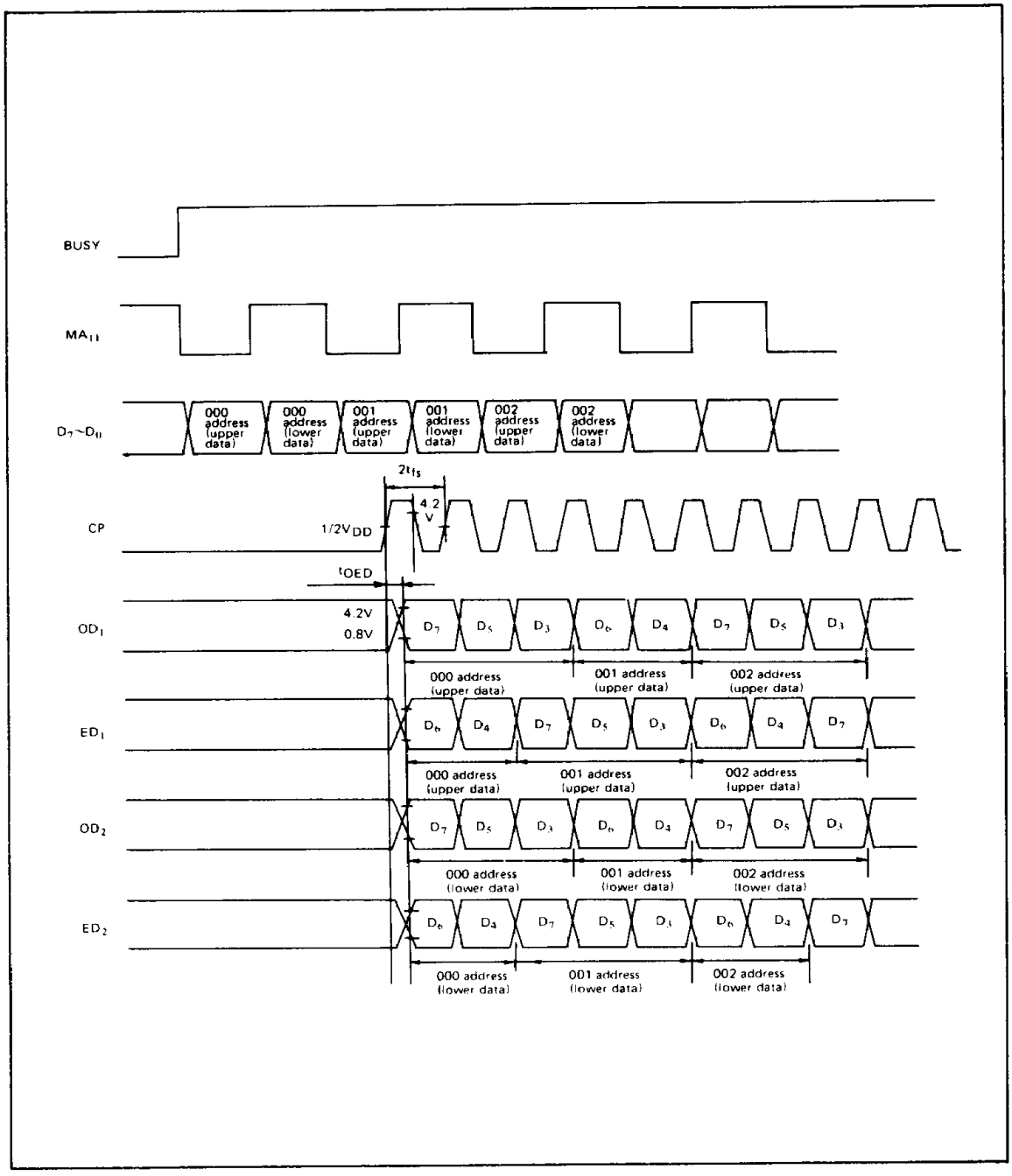
Parameter	Symbol	MIN	TYP	MAX	Unit
Drawing address delay time	t_{Ad1}			20	ns
Display address delay time	t_{Ad2}			120	ns

THE DISPLAY DATA TO LCD DRIVERS

1) Without ODD/EVEN data processing



2) Under ODD/EVEN data processing



(C_L = 80pF)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Shift clock pulse cycle time	t_{fs}	—	300	–	–	ns
Shift data delay time	t_{DAH}	—	–	–	50	ns
Shift clock pulse cycle time	$2t_{fs}$	—	400	–	–	ns
Shift clock data delay time	t_{OED}	—	–	–	80	ns

PIN DESCRIPTION

Pin name	I/O/Z	Function
OD_1 ED_1	$\bar{O}$	(Odd data) Output of serial data for X driver (Even data) Upper screen's data
OD_2 ED_2	$\bar{O}$	(Odd data) Output of serial data for X driver (Even data) Lower screen's data
LIP	$\bar{O}$	(Latch pulse) Latch pulse for one line
FRP	$\bar{O}$	(Frame pulse) Signal input to Y driver
FRM	$\bar{O}$	(Frame) Frame inversion signal
CP	$\bar{O}$	(Shift clock pulse) Shift clock pulse for X driver
BUSY	$\bar{O}$	"READY" SIGNAL L druing suspension of serial transfer
DIEN	I	(Display enable) Display enable signal; active H
MCE	$\bar{O}$	(Chip Enable) Memory chip enable control signal
$\overline{CL}$	I	(Clear) Clear terminal
XT $\overline{XT}$	I $\bar{O}$	(X'tal OSC) Crystal oscillation
V_{DD}		+5V
GND		0V
OEEN	I	Odd-number even-number data enable; active H

Pin name	I/O/Z	Function
MA_0 ∫ MA_{10}	$\overline{O}$/Z	(Memory address) Memory refresh address output, straight binary address $MA_0 \sim MA_{11}$ and $LA_0 \sim LA_4$ are at high impedance during DIEN = L
MA_{11}	$\overline{O}$/Z	Highest order bit of address signal, switching of upper and lower surfaces $MA_0 \sim MA_{11}$ and $LA_0 \sim LA_4$ are at high impedance during DIEN = L
LA_0 ∫ LA_4	$\overline{O}$/Z	(Line address) Line scan output for character generation $MA_0 \sim MA_{11}$ and $LA_0 \sim LA_4$ are at high impedance during DIEN = L
D_0 ∫ D_7	I	Display data input
S_0 ∫ S_3	I	Selection of number of VP and lines Refer to Sec. 10
CS_0 ∫ CS_1	I	Selection of number of characters to be displayed

CS_1	L	L	H	H
CS_0	L	H	L	H
No. of characters	32	40	64	80

HS_0 ∫ HS_2	I	(Horizontal select) HP programming
REN	I	(Reverse enable) Display inversion; active H
DAEN	I	Data input enable signal; active H
UDEN	I	Cursor display; active H
CHBL	I	Character blink; active H
UDBL	I	Cursor blink; active H
CSEN	I	Cursor display; active H
TEST1 ∫ TEST3	I	Test pins. On-chip pull-up resistors

FUNCTIONAL DESCRIPTION

1. Selection of HP

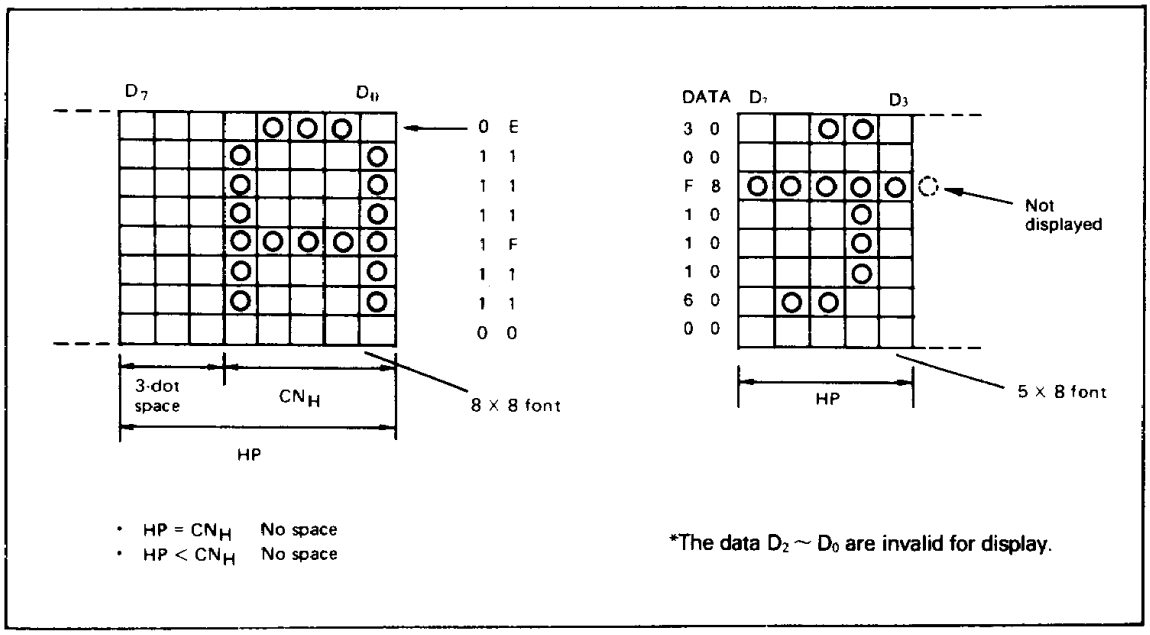
HP is determined by the logic levels of HS_2, HS_1 and HS_0.

HS_2	HS_1	HS_0	HP
L	L	L	5 dot
L	L	H	6
L	H	L	7
L	H	H	8
H	L	L	10
H	L	H	12
H	H	L	14
H	H	H	16

- **The horizontal space in a font**
  The horizontal space is determined by HP and number of horizontal dots/character (hereinafter called CN_H) in the character generator ROM.
  $HP > CN_H$ Space $= HP - CN_H$

(Example)
HP = 8 (HS_2 HS_1 HS_0:011)
CN_H = 5

(Example)
HP = 5 (HS_2 HS_1 HS_0:000)



- $HP = CN_H$ No space
- $HP < CN_H$ No space

*The data $D_2 \sim D_0$ are invalid for display.

● **The vertical space in a font**
The vertical space is determined by VP and vertical dots/character (hereinafter called CN_V) in the character ROM.

- $VP > CN_V$ Space = $VP - CN_V$
- $VP = CN_V$ No space
- $VP < CN_V$ No space

The data whose number of bits are more than the number of HP are invalid for display.

2. Selection of Number of Characters

Number of characters controlled by MSM6240GS is determined by the logic levels of CS_0 and CS_1, as follows:

CS_1	L	L	H	H
CS_0	L	H	L	H
No. of characters	32	40	64	80

8(4 X 2) lines X 80 characters
This is the case when HP is 8 or less. When HP is 10 ~ 16, the display on the LCD panel becomes 8(4 X 2) lines X 40 characters.

(Note) When HP is set to 10, 12, 14 or 16, display of characters on the LCD panel is made by accessing twice to the character generator ROM.
The memory address signal, $MA_0 \sim MA_{10}$, to the LCD panel is addressed as shown in the table below.

000	001		04E	04F
050	051		09E	09F
0A0	0A1		0EE	0EF
0F0	0F1		13E	13F
000	001		04E	04F
050	051		09E	09F
0A0	0A1		0EE	0EF
0F0	0F1		13E	13F

MA_{11} = L

MA_{11} = H

0F0 means following data.

MA 10	9	8	7	6	5	4	3	2	1	0
L	L	L	H	H	H	H	L	L	L	L

3. Selection of Number of HP and Lines

S_3 S_2	S_1 S_0	VP	No. of lines	Number of characters/line								Duty
				HP is 10 ~ 16				HP is 8 or less				
L L	L L	8	4	80	64	40	32	80	64	40	32	1/32
L L	L H	8	6	80	64	40	32	80	64	40	32	1/48
L L	H L	8	8	80	64	40	32	80	64	40	32	1/64
L L	H H	8	12	80	64	40	32	80	64	40	32	1/96
H H	H H	8	16	(80)	64	40	32	80	64	40	32	1/128
L H	L L	12	4	80	64	40	32	80	64	40	32	1/48
L H	H L	12	8	80	64	40	32	80	64	40	32	1/96
H L	L L	18	4	80	64	40	32	80	64	40	32	1/72
H L	L H	18	6	80	64	40	32	80	64	40	32	1/108
H L	H L	18	8	80	64	40	32	80	64	40	32	1/144
H H	L L	20	4	80	64	40	32	80	64	40	32	1/80

*Number of lines on above table is half of the actual number of lines on the LCD panel.
When all of $S_3 \sim S_0$ are set at high level (which means HP is 16 and number of characters/line is 80), the display on the LCD panel becomes as shown below because the capacity of the display RAM overflows.

HP = 8
Number of lines = 12
VP = 16
Number of characters/line = 80

4. Attribute Function

This function is determined by the data of the external attribute RAM. The attribute function per font is available.

- **Character Display, Blink**

DAEN	CHBL	Display
L	L	BLANK
L	H	Blink
H	L	Display
H	H	$\overline{\text{Blink}}$

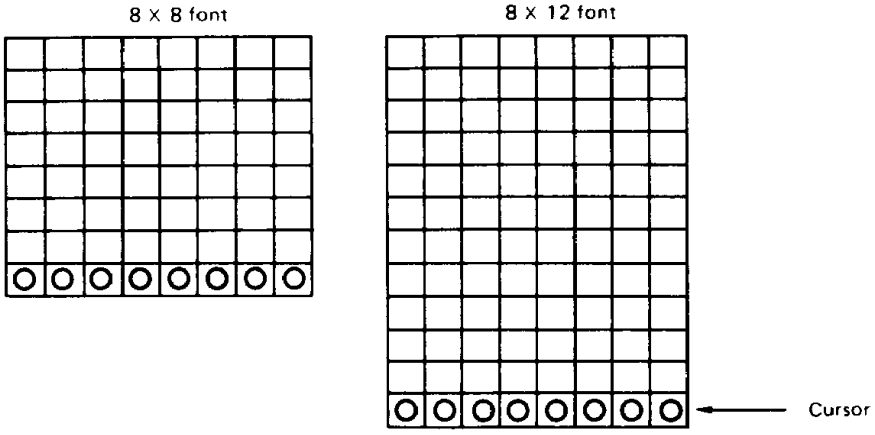
- **Cursor Display and Blink**

UDBL	CSEN	UDEN	Cursor Display
L	L	L	None
L	L	H	None
L	H	L	None
L	H	H	Cursor display
H	L	L	None
H	L	H	None
H	H	L	Cursor blink
H	H	H	$\overline{\text{Cursor blink}}$*

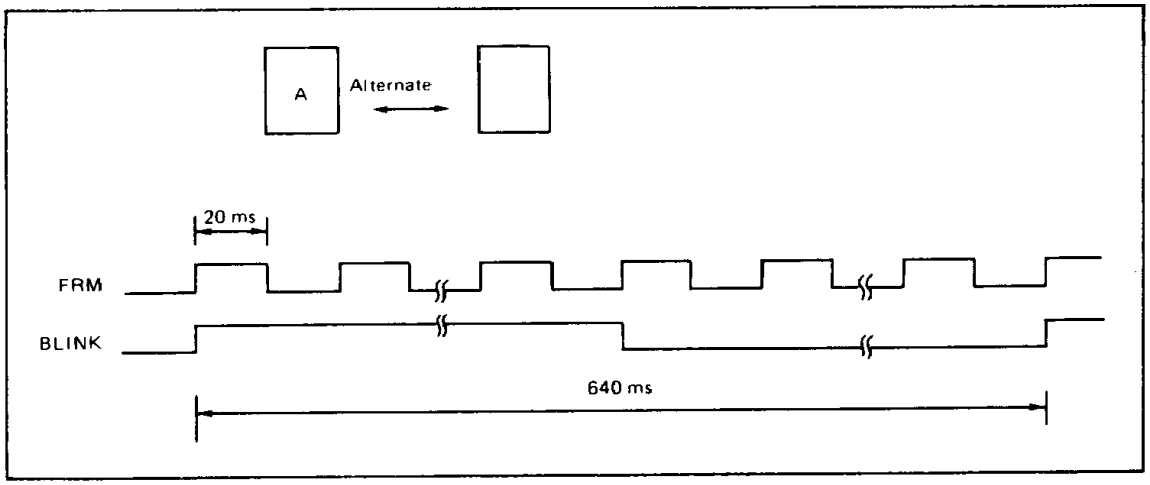
*The character and cursor blink alternately.

- **Cursor display position**
  Cursor is displayed in the bottom line of the font. The number of horizontal dots/font is same as that of HP.

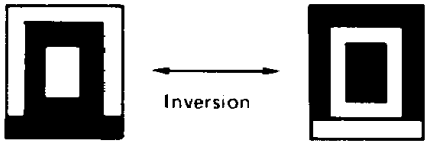
  (Example)



- **Blink**
  The blink cycle is 640 ms (FRP = 50 Hz) and is cynchronized to FRM signal.



- **Display inversion**

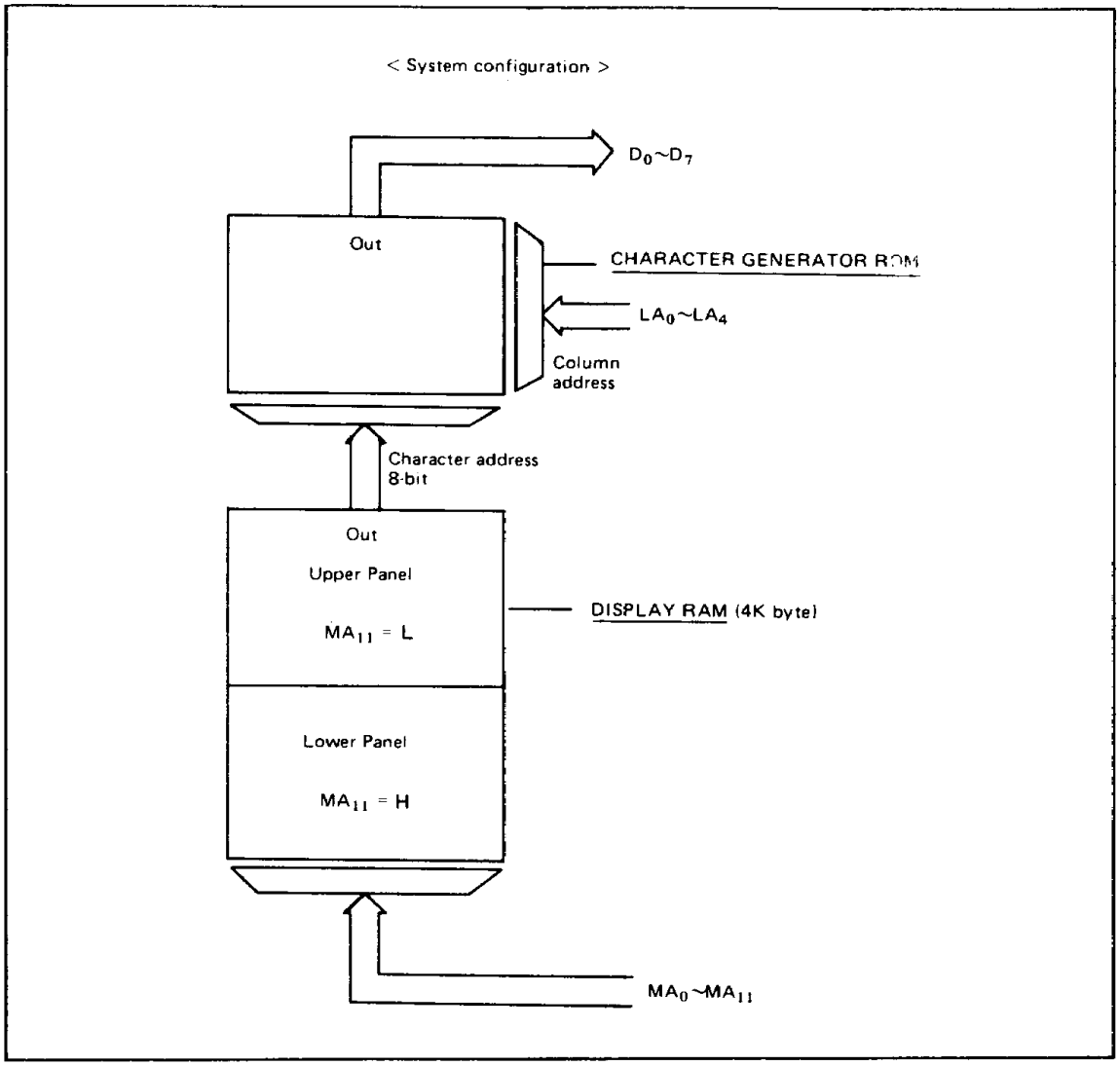


The display of character and cursor is inverted.

5. Display RAM (2K bytes)

The MSM6240GS is applicable to both character mode and graphic mode, which is only determined by system configuration, not by software.

- **When using Display RAM in the character mode**



The character code is programmed in the Display RAM in 8-bit configuration. The data of Display RAM is converted to the data necessary to display a character on the LCD, and is input to $D_0 \sim D_7$, display data input, of the MSM6240GS.

The MSM6240GS is capable of controlling 4,096 characters maximum, however, this capacity is affected, as is shown on the Sec. 13, by the LCD drivers speed.

- **Relationship between $LA_0 \sim LA_4$ and VP**
  $LA_0 \sim LA_4$ are valid for octal, duodecimal, octdicimal and vigesimal signals.

VP = 8

LA_2	LA_1	LA_0
L	L	L
L	L	H
L	H	L
L	H	H
H	L	L
H	L	H
H	H	L
H	H	H

VP = 12

LA_3	LA_2	LA_1	LA_0
L	L	L	L
L	L	L	H
L	L	H	L
L	L	H	H
L	H	L	L
L	H	L	H
L	H	H	L
L	H	H	H
H	L	L	L
H	L	L	H
H	L	H	L
H	L	H	H

VP = 18

LA_4	LA_3	LA_2	LA_1	LA_0
L	L	L	L	L
L	L	L	L	H
L	L	L	H	L
L	L	L	H	H
L	L	H	L	L
L	L	H	L	H
L	L	H	H	L
L	L	H	H	H
L	H	L	L	L
L	H	L	L	H
L	H	L	H	L
L	H	L	H	H
L	H	H	L	L
L	H	H	L	H
L	H	H	H	L
L	H	H	H	H
H	L	L	L	L

VP = 20

LA_4	LA_3	LA_2	LA_1	LA_0
L	L	L	L	L
L	L	L	L	H
L	L	L	H	L
L	L	L	H	H
L	L	H	L	L
L	L	H	L	H
L	L	H	H	L
L	L	H	H	H
L	H	L	L	L
L	H	L	L	H
L	H	L	H	L
L	H	L	H	H
L	H	H	L	L
L	H	H	L	H
L	H	H	H	L
L	H	H	H	H
H	L	L	L	L
H	L	L	L	H
H	L	L	H	L
H	L	L	H	H

- **Limitation of No. of characters and No. of lines**
  The No. of characters and the No. of lines are subject to limitation according to the RAM capacity.

When HP is set at 8 or less

No.	No. of characters/line	No. of lines	Display RAM area
1	80	16	000 ~ 4FF (H)
2	64	16	000 ~ 3FF (H)
3	40	16	000 ~ 27F (H)
4	32	16	000 ~ 1FF (H)

When HP is set at 10 ~ 16

No.	No. of characters/line	No. of lines	Display RAM area
5	80	12	000 ~ 77F (H)
6	64	16	000 ~ 7FF (H)
7	40	16	000 ~ 4FF (H)
8	32	16	000 ~ 3FF (H)

(Note) Number of lines on above table is half of the actual number of lines on the LCD panel.

(Example) RAM area 000 ~ 3BF

Memory address	MA_{11}	MA_{10}	MA_9	MA_8	MA_7	MA_6	MA_5	MA_4	MA_3	MA_2	MA_1	MA_0
Start address	L	L	L	L	L	L	L	L	L	L	L	L
End address	L	L	H	H	H	L	H	H	H	H	H	H
Start address	H	L	L	L	L	L	L	L	L	L	L	L
End address	H	L	H	H	H	L	H	H	H	H	H	H

Set HP at 8 or less

No. 1 In the case of 80 characters/line (Number of lines: 16 lines max.)

000	001	002	003		04E	04F
050	051	052	053		09E	09F
0A0	0A1	0A2	0A3		0EE	0EF
0F0	0F1	0F2	0F3		13E	13F
140	141	142	143		18E	18F
190	191	192	193		1DE	1DF
1E0	1E1	1E2	1E3		22E	22F
230	231	232	233		27E	27F
280	281	282	283		2CE	2CF
2D0	2D1	2D2	2D3		31E	31F
320	321	322	323		36E	36F
370	371	372	373		3BE	3BF
3C0	3C1	3C2	3C3		40E	40F
410	411	412	413		45E	45F
400	401	402	403		4AE	4AF
4B0	4B1	4B2	4B3		4FE	4FE

The table above shows the memory address to the LCD panel.
It only shows the address to the upper part of the LCD panel. Whether it be the upper or lower will be determined by the H/L condition of MA_{11}.

No. 2 In the case of 64 characters/line (Number of lines: 16 lines max.)

000	001	002	003		03E	03F
040	041	042	043		07E	07F
080	081	082	083		0BE	0BF
0C0	0C1	0C2	0C3		0FE	0FF
100	101	102	103		13E	13F
140	141	142	143		17E	17F
180	181	182	183		1BE	1BF
1C0	1C1	1C2	1C3		1FE	1FF
200	201	202	203		23E	23F
240	241	242	243		27E	27F
280	281	282	283		2BE	2BF
2C0	2C1	2C2	2C3		2FE	2FF
300	301	302	303		33E	33F
340	341	342	343		37E	37F
380	381	382	383		3BE	3BF
3C0	3C1	3C2	3C3		3FE	3FF

The table above shows the memory address to the LCD panel.
It only shows the address to the upper part of the LCD panel. Whether it be the upper or lower will be determined by the H/L condition of MA_{11}.

No. 3 In the case of 40 characters/line (Number of lines: 16 lines max.)

000	001	002	003		026	027
028	029	02A	02B		04E	04F
050	051	052	053		076	077
078	079	07A	07B		09E	09F
0A0	0A1	0A2	0A3		0C6	0C7
0C8	0C9	0CA	0CB		0EE	0EF
0F0	0F1	0F2	0F3		116	117
118	119	11A	11V		13E	13F
140	141	142	143		166	167
168	169	16A	16B		18E	18F
190	191	192	193		1B6	1B7
1B8	1B9	1BA	1BB		1DE	1DF
1E0	1E1	1E2	1E3		206	207
208	209	20A	20B		22E	22F
230	231	232	233		256	257
258	259	25A	25B		27E	27F

The table above shows the memory address to the LCD panel.
It only shows the address to the upper part of the LCD panel. Whether it be the upper or lower will be determined by the H/L condition of MA_{11}.

No. 4 In the case of 32 characters/line (Number of lines: 16 lines max.)

000	001	002	003		01E	01F
020	021	022	023		03E	03F
040	041	042	043		05E	05F
060	061	062	063		07E	07F
080	081	082	083		09E	09F
0A0	0A1	0A2	0A3		0BE	0BF
0C0	0C1	0C2	0C3		0DE	0DF
0E0	0E1	0E2	0E3		0FE	0FF
100	101	102	103		11E	11F
120	121	122	123		13E	13F
140	141	142	143		15E	15F
160	161	162	163		17E	17F
180	181	182	183		19E	19F
1A0	1A1	1A2	1A3		1BE	1BF
1C0	1C1	1C2	1C3		1DE	1DF
1E0	1E1	1E2	1E3		1FE	1FF

The table above shows the memory address to the LCD panel.
It only shows the address to the upper part of the LCD panel. Whether it be the upper or lower will be determined by the H/L condition of MA_{11}.

Set HP at 10 ~ 16

No. 5 In the case of 80 characters/line (Number of lines: 12 lines max.)

000	001	002	003		09E	09F
0A0	0A1	0A2	0A3		13E	13F
140	141	142	143		1DE	1DF
1E0	1E1	1E2	1E3		27E	27F
280	281	282	283		31E	31F
320	321	322	323		3BE	3BF
3C0	3C1	3C2	3C3		45E	45F
460	461	462	463		4FE	4FF
500	501	502	503		59E	59F
5A0	5A1	5A2	5A3		63E	63F
640	641	642	643		6DE	6DF
6E0	6E1	6E2	6E3		77E	77F

The table above shows the memory address to the LCD panel.
It only shows the address to the upper part of the LCD panel. Whether it be the upper or lower will be determined by the H/L condition of MA_{11}.

No. 6 In the case of 64 characters/line (Number of lines: 16 lines max.)

000	001	002	003		07E	07F
080	081	082	083		0FE	0FF
100	101	102	103		17E	17F
180	181	182	183		1FE	1FF
200	201	202	203		27E	27F
280	281	282	283		2FE	2FF
300	301	302	303		37E	37F
380	381	382	383		3FE	3FF
400	401	402	403		47E	47F
480	481	482	483		4FE	4FF
500	501	502	503		57E	57F
580	581	582	583		5FE	5FF
600	601	602	603		67E	67F
680	681	682	683		6FE	6FF
700	701	702	703		77E	77F
780	781	782	783		7FE	7FF

The table above shows the memory address to the LCD panel.
It only shows the address to the upper part of the LCD panel. Whether it be the upper or lower will be determined by the H/L condition of MA_{11}.

No. 7 In the case of 40 characters/line (Number of lines: 16 lines max.)

000	001	002	003		04E	04F
050	051	052	053		09E	09F
0A0	0A1	0A2	0A3		0EE	0EF
0F0	0F1	0F2	0F3		13E	13F
140	141	142	143		18E	18F
190	191	192	193		1DE	1DF
1E0	1E1	1E2	1E3		22E	22F
230	231	232	233		27E	27F
280	281	282	283		2CE	2CF
2D0	2D1	2D2	2D3		31E	31F
320	321	322	323		36E	36F
370	371	372	373		3BE	3BF
3C0	3C1	3C2	3C3		40E	40F
410	411	412	413		45E	45F
460	461	462	463		4AE	4AF
4B0	4B1	4B2	4B3		4FE	4FF

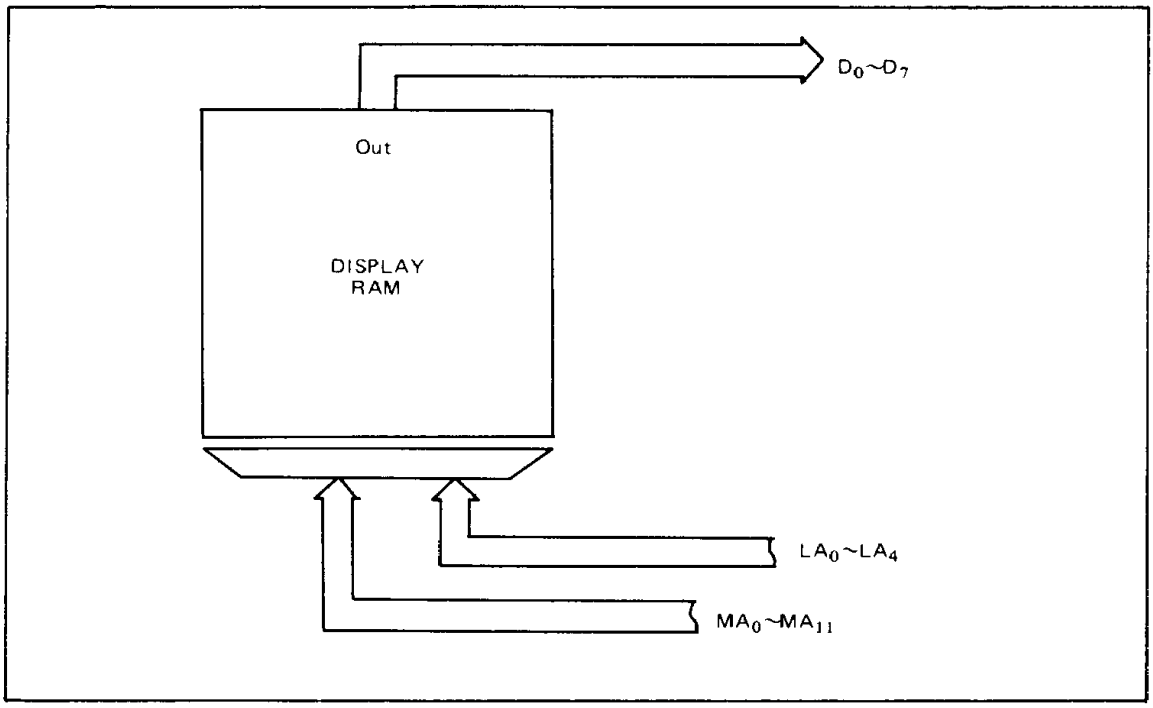
The table above shows the memoray address to the LCD panel.
It only shows the address to the upper part of the LCD panel. Whether it be the upper or lower will be determined by the H/L condition of MA_{11}.

No. 8 In the case of 32 characters/line (Number of lines: 16 lines max.)

000	001	002	003		03E	03F
040	041	042	043		07E	07F
080	081	082	083		0BE	0BF
0C0	0C1	0C2	0C3		0FE	0FF
100	101	102	103		13E	13F
140	141	142	143		17E	17F
180	181	182	183		1BE	1BF
1C0	1C1	1C2	1C3		1FE	1FF
200	201	202	203		23E	23F
240	241	242	243		27E	27F
280	281	282	283		2BE	2BF
2C0	2C1	2C2	2C3		2FE	2FF
300	301	302	303		33E	33F
340	341	342	343		37E	37F
380	381	382	383		3BE	3BF
3C0	3C1	3C2	3C3		3FE	3FF

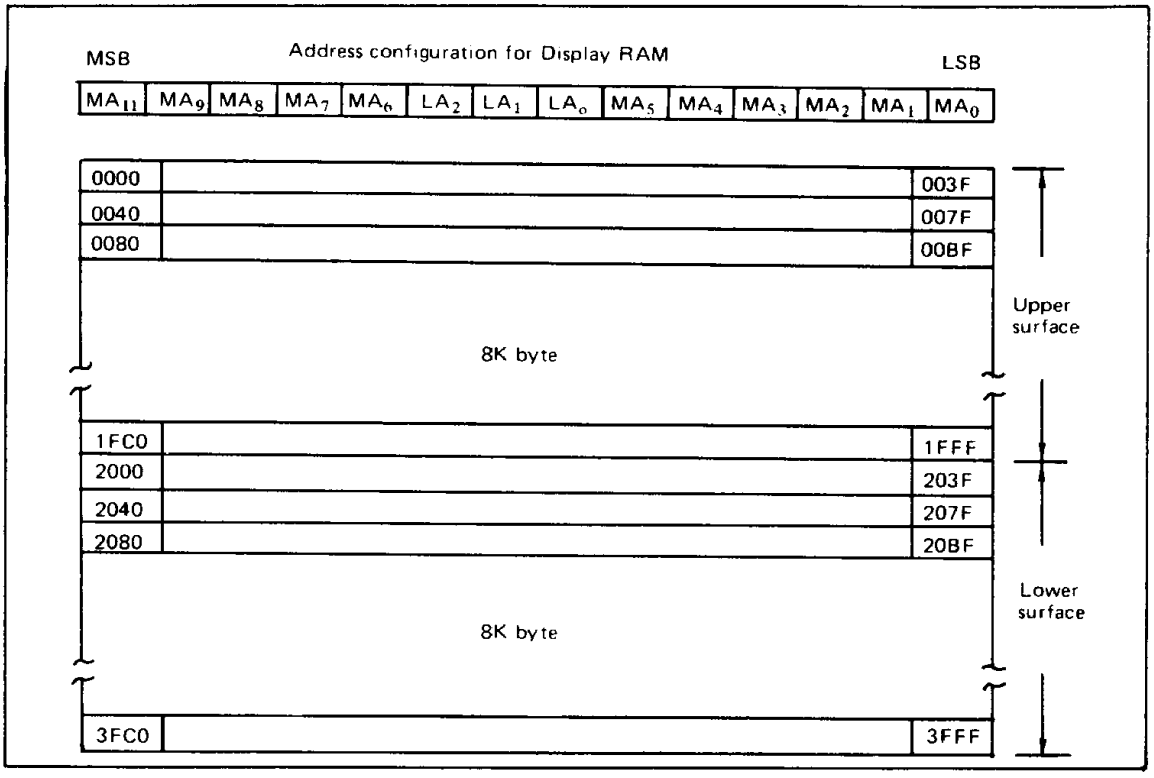
The table above shows the memory address to the LCD panel.
It only shows the address to the upper part of the LCD panel. Whether it be the upper or lower will be determined by the H/L condition of MA_{11}.

- **When using Display RAM in the graph mode**



(**Note**) The cursor display should not be used by setting CSEN at L.

(Example) HP = 8, VP = 8, 64 characters/line, 16 lines



6. Dien Signal

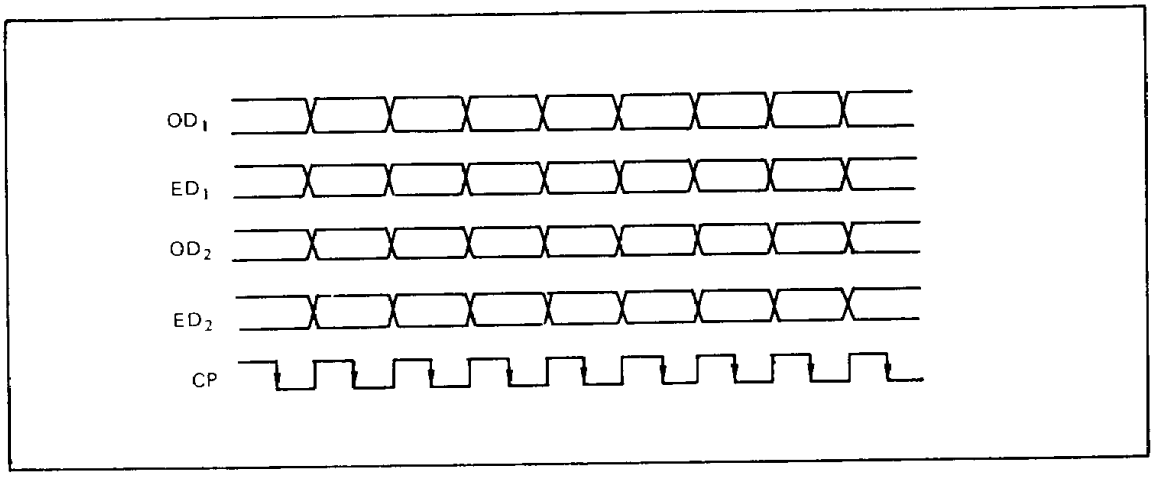
Before writing the data into DISPLAY RAM or ATTRIBUTE RAM, DIEN signal should be set at L.

7. Memory Chip Enable Signal (MCE)

Normally this signal is set at L. This signal becomes H when BUSY signal or DIEN signal become L, which reduces the current consumption of the external RAM by half.

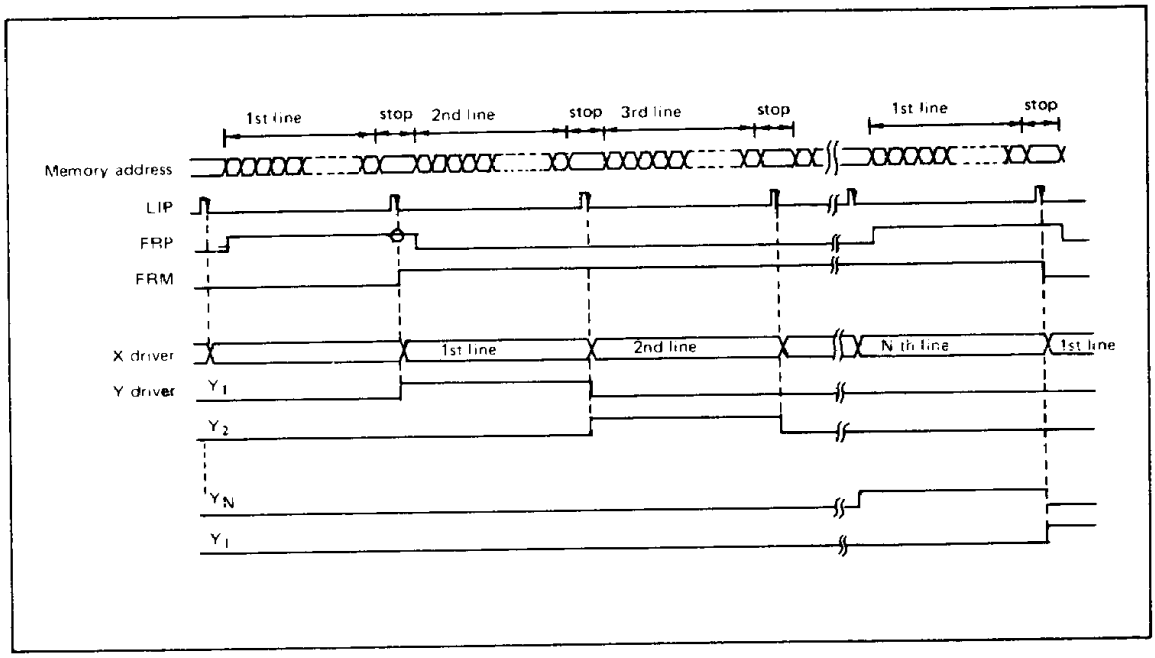
8. ODD/EVEN Number Data Processing

When OEEN is set at H, ODD/EVEN number data processing is proceeded.
The purpose of ODD/EVEN number data processing is to reduce the shift pulse "CP" speed by half. When MSM6240 is applied to wide LCD's control, the speed of shift pulse becomes high and it exceeds the maximum clock frequency of the LCD drivers, so, to reduce the shift pulse speed is required. When OEEN is set at L, ODD/EVEN number data processing is not proceeded.
OEEN may set at L only when HP is set at 8 or less. In this case, the data is sent to OD_1 (upper part) and OD_2 (lower part).



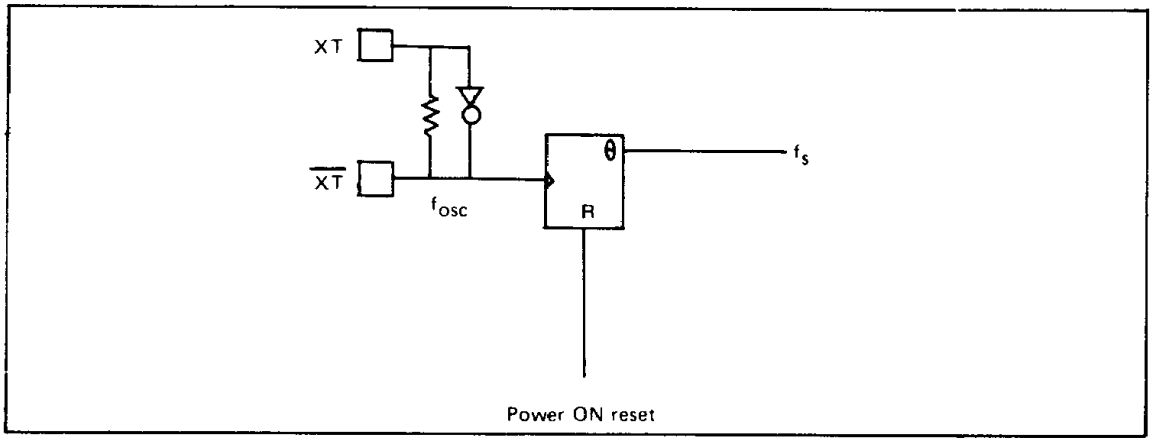
9. Frame Pulse, Frame, Latch

- **Timing chart**



The proper FRP frequency is 50 to 70 Hz. f_{osc} must be calculated so that it might match with FRP frequency.

10. X'TAL Oscillation



The frequency of the crystal is calculated by following formula.

- HP is 8 or less

  f_{osc} = (Number of characters + 8) X HP X 1/duty X FRP X 2

HP is 10 ~ 16

f_{osc} = (Number of characters X 2 + 16) X 8 X 1/duty X FRP X 2

11. Crystal Oscillation Frequency Table

HP = 8, FRP = 50 ~ 70 Hz

Duty \ No. of characters	32	40	64	80
1/128	4.1 ~ 5.7	4.9 ~ 6.9	7.4 ~ 10.3	9.0 ~ 12.6
1/96	3.1 ~ 4.3	3.7 ~ 5.2	5.5 ~ 7.7	6.8 ~ 9.5
1/64	2.0 ~ 2.9	2.5 ~ 3.5	3.7 ~ 5.18	4.5 ~ 6.3
1/48	1.5 ~ 2.1	1.8 ~ 2.5	2.8 ~ 3.9	3.4 ~ 4.8

HP = 7, FRP = 50 ~ 70 Hz

Duty \ No. of characters	32	40	64	80
1/128	3.6 ~ 5.0	4.3 ~ 6.0	6.5 ~ 9.1	7.9 ~ 11.1
1/96	2.7 ~ 3.8	3.2 ~ 4.5	4.8 ~ 6.7	5.9 ~ 8.3
1/64	1.7 ~ 2.5	2.2 ~ 3.1	3.2 ~ 4.5	3.9 ~ 5.5
1/48	1.3 ~ 1.8	1.6 ~ 2.2	2.5 ~ 3.5	3.0 ~ 4.2

HP = 6, FRP = 50 ~ 70 Hz

No. of characters / Duty	32	40	64	80
1/128	3.1 ~ 4.3	3.7 ~ 5.2	5.6 ~ 7.8	6.8 ~ 9.5
1/96	2.3 ~ 3.2	2.8 ~ 3.9	4.1 ~ 5.7	5.1 ~ 7.1
1/64	1.5 ~ 2.1	1.9 ~ 2.7	2.8 ~ 3.9	3.4 ~ 4.8
1/48	1.1 ~ 1.5	1.4 ~ 2.0	2.1 ~ 2.9	2.6 ~ 3.6

HP = 5, FRP = 50 ~ 70 Hz

No. of characters / Duty	32	40	64	80
1/128	2.6 ~ 3.6	3.1 ~ 4.3	4.6 ~ 6.4	5.6 ~ 7.8
1/96	1.9 ~ 2.7	2.3 ~ 3.2	3.4 ~ 4.8	4.3 ~ 6.0
1/64	1.3 ~ 1.8	1.6 ~ 2.2	2.3 ~ 3.2	2.8 ~ 3.9
1/48	0.9 ~ 1.3	1.1 ~ 1.5	1.8 ~ 2.5	2.1 ~ 2.9

HP = 10 ~ 16, FRP = 50 ~ 70 Hz

No. of characters / Duty	32	40	64	80
1/128	8.2 ~ 11.5	9.8 ~ 13.7	14.7 ~ 20.6	18.0 ~ 25.2
1/96	6.1 ~ 8.5	7.4 ~ 10.4	11.1 ~ 15.5	13.5 ~ 18.9
1/64	4.1 ~ 5.7	4.9 ~ 6.9	7.4 ~ 10.3	9.0 ~ 12.6
1/48	3.1 ~ 4.3	3.7 ~ 5.2	5.5 ~ 7.7	6.8 ~ 9.5

The value on above tables are affected by the maximum frequency of LCD driver's shift clock input and an maximum frequency of f_{osc}.
The relation between f_{osc} and shift clock is as follows.

- When ODD/EVEN data processing is proceeded
  $CP = f_{osc}/4$
- When ODD/EVEN data processing is not proceeded
  $CP = f_{osc}/2$

For example, the f_{osc} is limited as follows when MSM5260GS, whose maximum frequency of shift pulse is 3.3 MHz, is connected to MSM6240GS.

- When ODD/EVEN data processing is proceeded
  $f_{osc} \leq 10$ MHz
- When ODD/EVEN data processing is not proceeded
  $f_{osc} \leq 6.6$ MHz

TYPICAL SYSTEM CONFIGURATION