

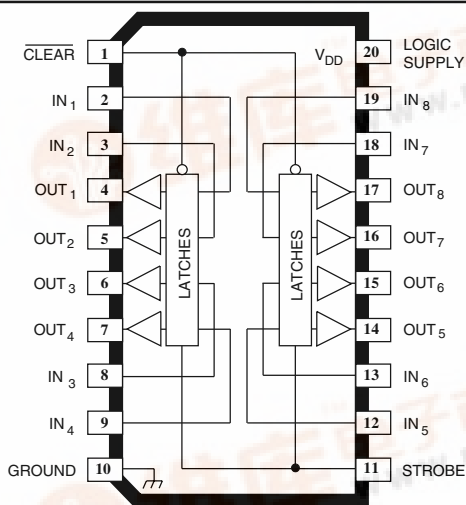
6273

Data Sheet  
26180.120

## ADVANCE INFORMATION

(Subject to change without notice)

January 24, 2000

8-BIT LATCHED  
DMOS POWER DRIVER

Dwg. PP-015-2

Note that the A6273KA (DIP) and the A6273KLW (SOIC) are electrically identical and share a common terminal number assignment.

## ABSOLUTE MAXIMUM RATINGS

at  $T_A = 25^\circ\text{C}$ 

Output Voltage, $V_O$ .....	50 V
Output Drain Current,	
Continuous, $I_O$ .....	250 mA*
Peak, $I_{OM}$ .....	750 mA*†
Peak, $I_{OM}$ .....	2.0 A†
Single-Pulse Avalanche Energy,	
$E_{AS}$ .....	75 mJ
Logic Supply Voltage, $V_{DD}$ .....	7.0 V
Input Voltage Range,	
$V_I$ .....	-0.3 V to +7.0 V
Package Power Dissipation,	
$P_D$ .....	See Graph
Operating Temperature Range,	
$T_A$ .....	-40°C to +125°C
Storage Temperature Range,	
$T_S$ .....	-55°C to +150°C

\* Each output, all outputs on.

† Pulse duration  $\leq 100 \mu\text{s}$ , duty cycle  $\leq 2\%$ .

Caution: These CMOS devices have input static protection (Class 3) but are still susceptible to damage if exposed to extremely high static electrical charges.

The A6273KA and A6273KLW combine eight (positive-edge-triggered D-type) data latches and DMOS outputs for systems requiring relatively high load power. Driver applications include relays, solenoids, and other medium-current or high-voltage peripheral power loads. The CMOS inputs and latches allow direct interfacing with microprocessor-based systems. Use with TTL may require appropriate pull-up resistors to ensure an input logic high.

The DMOS output inverts the DATA input. All of the output drivers are disabled (the DMOS sink drivers turned OFF) with the CLEAR input low. The A6273KA/KLW DMOS open-drain outputs are capable of sinking up to 750 mA. Similar devices with reduced  $r_{DS(on)}$  will be available as the A6A273.

The A6273KA is furnished in a 20-pin dual in-line plastic package. The A6273KLW is furnished in a 20-lead wide-body, small-outline plastic package (SOIC) with gull-wing leads for surface-mount applications. Copper lead frames, reduced supply current requirements, and low on-state resistance allow both devices to sink 150 mA from all outputs continuously, to ambient temperatures over 85°C.

## FEATURES

- 50 V Minimum Output Clamp Voltage
- 250 mA Output Current (all outputs simultaneously)
- 1.3  $\Omega$  Typical  $r_{DS(on)}$
- Low Power Consumption
- Replacements for TPIC6273N and TPIC6273DW

Always order by complete part number:

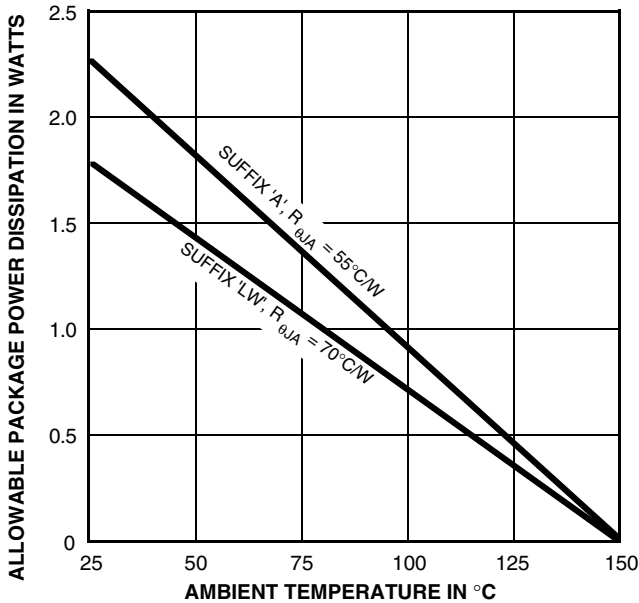
Part Number	Package	$R_{\theta JA}$	$R_{\theta JC}$
A6273KA	20-pin DIP	55°C/W	25°C/W
A6273KLW	20-lead SOIC	70°C/W	17°C/W



6273

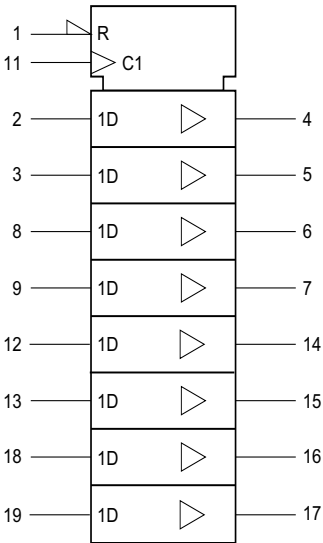
8-BIT LATCHED

DMOS POWER DRIVER

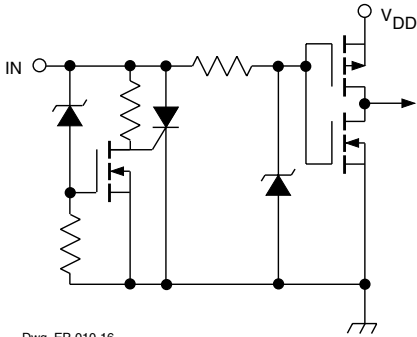


Dwg. GS-004A

LOGIC SYMBOL

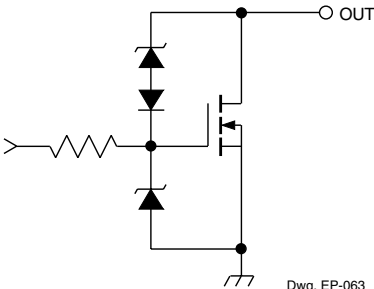


Dwg. FP-046-1



Dwg. EP-010-16

LOGIC INPUTS



Dwg. EP-063

DMOS POWER DRIVER OUTPUT

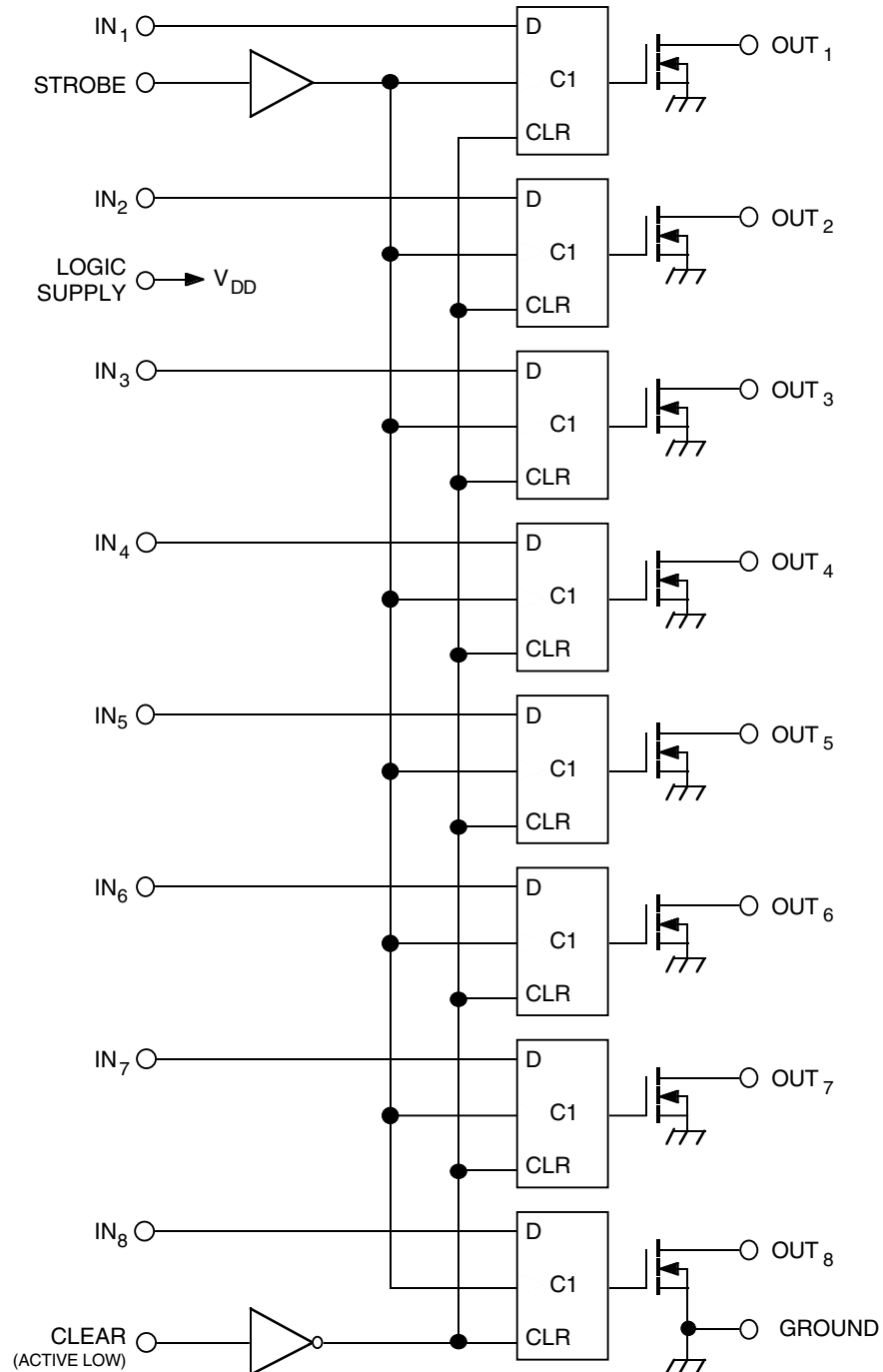
FUNCTION TABLE

Inputs			OUT <sub>x</sub>
CLEAR	STROBE	IN <sub>x</sub>	
L	X	X	H
H		H	L
H		L	H
H	L	X	R

L = Low Logic Level  
H = High Logic Level  
X = Irrelevant  
R = Previous State

**6273**  
**8-BIT LATCHED**  
**DMOS POWER DRIVER**

**FUNCTIONAL BLOCK DIAGRAM**



# 6273

## 8-BIT LATCHED

## DMOS POWER DRIVER

### RECOMMENDED OPERATING CONDITIONS

over operating temperature range

Logic Supply Voltage Range,  $V_{DD}$  ..... 4.5 V to 5.5 V

High-Level Input Voltage,  $V_{IH}$  .....  $\geq 0.85V_{DD}$

Low-level input voltage,  $V_{IL}$  .....  $\leq 0.15V_{DD}$

**ELECTRICAL CHARACTERISTICS at  $T_A = +25^\circ\text{C}$ ,  $V_{DD} = 5\text{ V}$ ,  $t_{ir} = t_{if} \leq 10\text{ ns}$  (unless otherwise specified).**

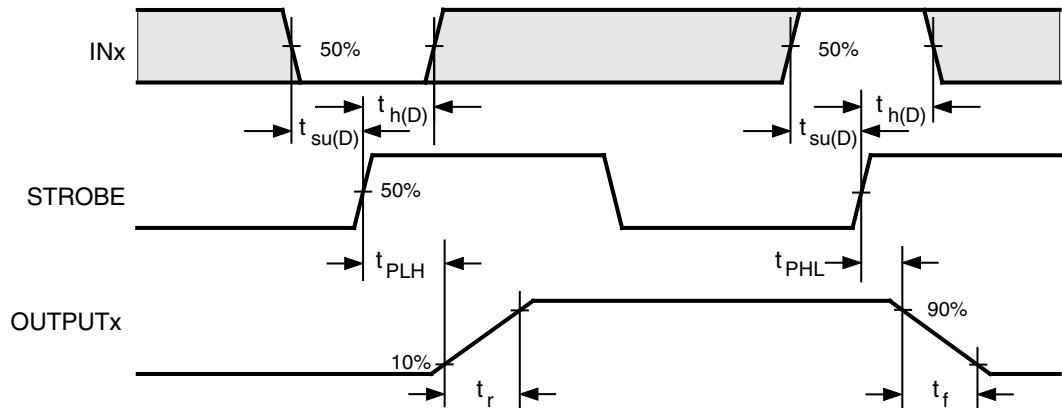
Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Logic Supply Voltage	$V_{DD}$	Operating	4.5	5.0	5.5	V
Output Breakdown Voltage	$V_{(BR)DSX}$	$I_O = 1\text{ mA}$	50	—	—	V
Off-State Output Current	$I_{DSX}$	$V_O = 40\text{ V}$	—	0.05	1.0	$\mu\text{A}$
		$V_O = 40\text{ V}$ $T_A = 125^\circ\text{C}$	—	0.15	5.0	$\mu\text{A}$
Static Drain-Source On-State Resistance	$r_{DS(on)}$	$I_O = 250\text{ mA}$ , $V_{DD} = 4.5\text{ V}$	—	1.3	2.0	$\Omega$
		$I_O = 250\text{ mA}$ , $V_{DD} = 4.5\text{ V}$ , $T_A = 125^\circ\text{C}$	—	2.0	3.2	$\Omega$
		$I_O = 500\text{ mA}$ , $V_{DD} = 4.5\text{ V}$ (see note)	—	1.3	2.0	$\Omega$
Nominal Output Current	$I_{O(nom)}$	$V_{DS(on)} = 0.5\text{ V}$ , $T_A = 85^\circ\text{C}$	—	250	—	mA
Logic Input Current	$I_{IH}$	$V_I = V_{DD} = 5.5\text{ V}$	—	—	1.0	$\mu\text{A}$
	$I_{IL}$	$V_I = 0$ , $V_{DD} = 5.5\text{ V}$	—	—	-1.0	$\mu\text{A}$
Prop. Delay Time	$t_{PLH}$	$I_O = 250\text{ mA}$ , $C_L = 30\text{ pF}$	—	625	—	ns
	$t_{PHL}$	$I_O = 250\text{ mA}$ , $C_L = 30\text{ pF}$	—	150	—	ns
Output Rise Time	$t_r$	$I_O = 250\text{ mA}$ , $C_L = 30\text{ pF}$	—	675	—	ns
Output Fall Time	$t_f$	$I_O = 250\text{ mA}$ , $C_L = 30\text{ pF}$	—	400	—	ns
Supply Current	$I_{DD(off)}$	$V_{DD} = 5.5\text{ V}$ , Outputs OFF	—	15	100	$\mu\text{A}$
	$I_{DD(on)}$	$V_{DD} = 5.5\text{ V}$ , Outputs ON	—	150	300	$\mu\text{A}$

Typical Data is at  $V_{DD} = 5\text{ V}$  and is for design information only.

NOTE — Pulse test, duration  $\leq 100\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .

# 6273 8-BIT LATCHED DMOS POWER DRIVER

## TIMING REQUIREMENTS



Dwg. WP-036-1

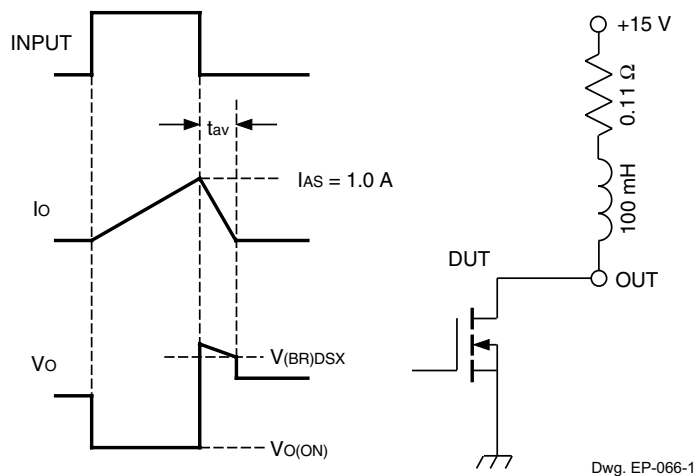
Input Active Time Before Strobe (Data Set-Up Time), $t_{su(D)}$ .....	<b>20 ns</b>
Input Active Time After Strobe (Data Hold Time), $t_{h(D)}$ .....	<b>20 ns</b>
Input Pulse Width, $t_{w(D)}$ .....	<b>40 ns</b>
Input Logic High, $V_{IH}$ .....	$\geq 0.85V_{DD}$
Input Logic Low, $V_{IL}$ .....	$\leq 0.15V_{DD}$

# 6273

## 8-BIT LATCHED

### DMOS POWER DRIVER

#### TEST CIRCUITS



$$E_{AS} = I_{AS} \times V_{(BR)DSX} \times t_{AV}/2$$

#### Single-Pulse Avalanche Energy Test Circuit and Waveforms

**6273**  
**8-BIT LATCHED**  
**DMOS POWER DRIVER**

**TERMINAL DESCRIPTIONS**

Terminal No.	Terminal Name	Function
1	CLEAR	When (active) LOW, all latches are reset and all outputs go HIGH (turn OFF).
2	IN <sub>1</sub>	CMOS data input to a latch. When strobed, the output then inverts the data input (IN <sub>1</sub> = HIGH, OUT <sub>1</sub> = LOW).
3	IN <sub>2</sub>	CMOS data input to a latch. When strobed, the output then inverts the data input (IN <sub>2</sub> = HIGH, OUT <sub>2</sub> = LOW).
4	OUT <sub>1</sub>	Current-sinking, open-drain DMOS output.
5	OUT <sub>2</sub>	Current-sinking, open-drain DMOS output.
6	OUT <sub>3</sub>	Current-sinking, open-drain DMOS output.
7	OUT <sub>4</sub>	Current-sinking, open-drain DMOS output.
8	IN <sub>3</sub>	CMOS data input to a latch. When strobed, the output then inverts the data input (IN <sub>3</sub> = HIGH, OUT <sub>3</sub> = LOW).
9	IN <sub>4</sub>	CMOS data input to a latch. When strobed, the output then inverts the data input (IN <sub>4</sub> = HIGH, OUT <sub>4</sub> = LOW).
10	GROUND	Reference terminal for all voltage measurements.
11	STROBE	A CMOS dynamic input to all latches. Data on each IN <sub>x</sub> terminal is loaded into its associated latch on a low-to-high STROBE transition.
12	IN <sub>5</sub>	CMOS data input to a latch. When strobed, the output then inverts the data input (IN <sub>5</sub> = HIGH, OUT <sub>5</sub> = LOW).
13	IN <sub>6</sub>	CMOS data input to a latch. When strobed, the output then inverts the data input (IN <sub>6</sub> = HIGH, OUT <sub>6</sub> = LOW).
14	OUT <sub>5</sub>	Current-sinking, open-drain DMOS output.
15	OUT <sub>6</sub>	Current-sinking, open-drain DMOS output.
16	OUT <sub>7</sub>	Current-sinking, open-drain DMOS output.
17	OUT <sub>8</sub>	Current-sinking, open-drain DMOS output.
18	IN <sub>7</sub>	CMOS data input to a latch. When strobed, the output then inverts the data input (IN <sub>7</sub> = HIGH, OUT <sub>7</sub> = LOW).
19	IN <sub>8</sub>	CMOS data input to a latch. When strobed, the output then inverts the data input (IN <sub>8</sub> = HIGH, OUT <sub>8</sub> = LOW).
20	LOGIC SUPPLY	(V <sub>DD</sub> ) The logic supply voltage (typically 5 V).

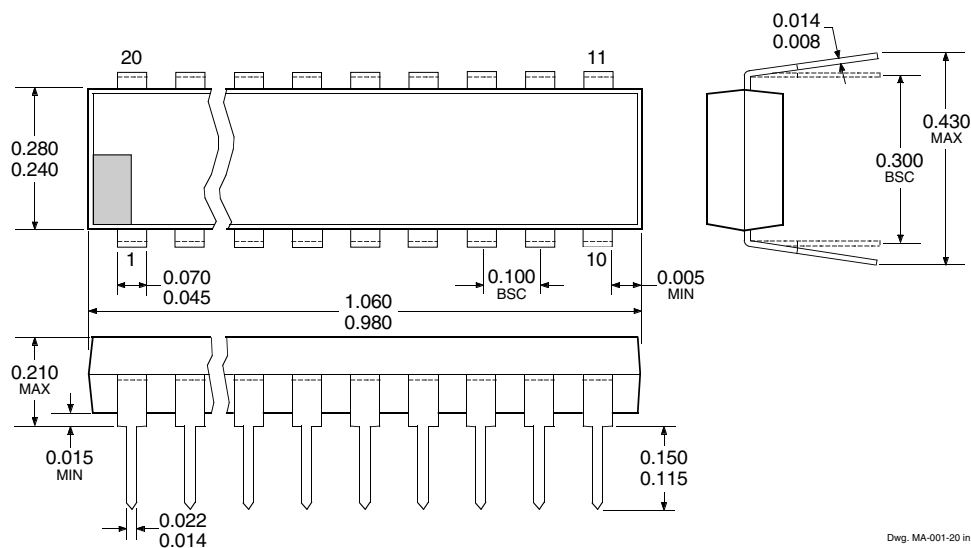
# 6273

## 8-BIT LATCHED

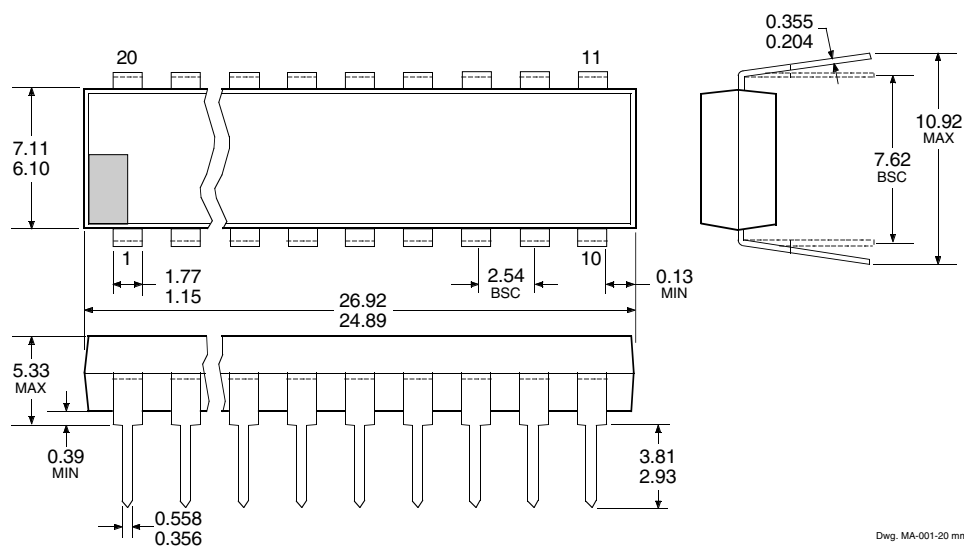
## DMOS POWER DRIVER

### A6273KA

Dimensions in Inches  
(controlling dimensions)



### Dimensions in Millimeters (for reference only)

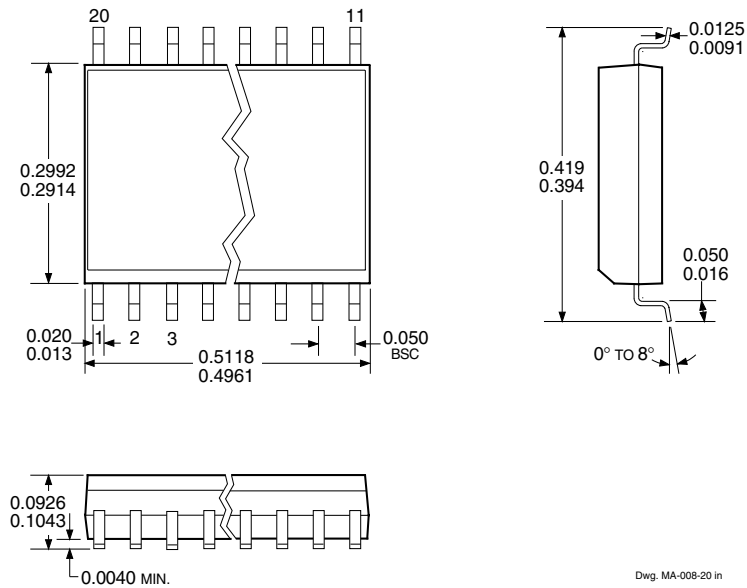


- NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.  
2. Lead spacing tolerance is non-cumulative.  
3. Lead thickness is measured at seating plane or below.

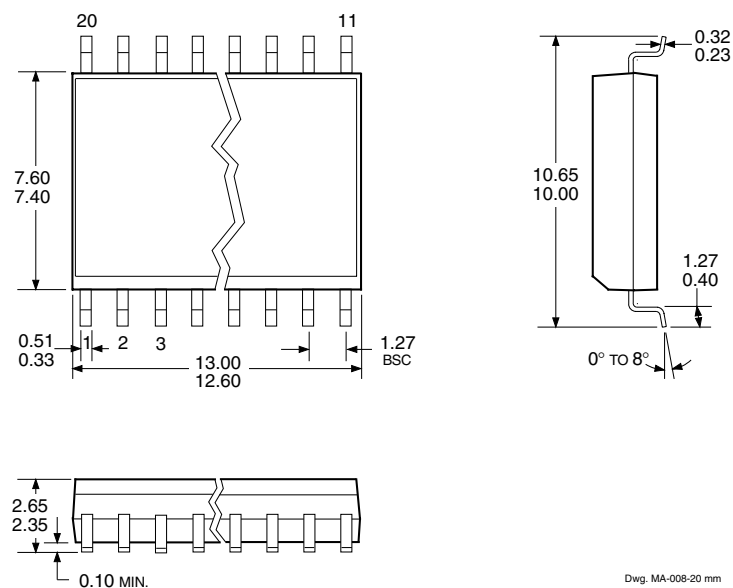


# **6273** **8-BIT LATCHED** **DMOS POWER DRIVER**

## **A6273KLW** Dimensions in Inches (for reference only)



## Dimensions in Millimeters (controlling dimensions)



- NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.  
2. Lead spacing tolerance is non-cumulative.

**6273**  
**8-BIT LATCHED**  
**DMOS POWER DRIVER**

*The products described here are manufactured under one or more U.S. patents or U.S. patents pending.*

*Allegro MicroSystems, Inc. reserves the right to make, from time to time, such departures from the detail specifications as may be required to permit improvements in the performance, reliability, or manufacturability of its products. Before placing an order, the user is cautioned to verify that the information being relied upon is current.*

*Allegro products are not authorized for use as critical components in life-support devices or systems without express written approval.*

*The information included herein is believed to be accurate and reliable. However, Allegro MicroSystems, Inc. assumes no responsibility for its use; nor for any infringement of patents or other rights of third parties which may result from its use.*