12-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER WITH INTERNAL PULL DOWN RESISTORS

SCDS053C - MARCH 1998 - REVISED FEBRUARY 1999

- 4-Ω Switch Connection Between Two Ports
- TTL-Compatible Control Input Levels
- Make-Before-Break Feature
- Internal 500- Ω Pulldown Resistors to Ground
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Package Options Include Plastic Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV), and 300-mil Shrink Small-Outline (DL) Packages

description

The SN74CBT16292 is a 12-bit 1-of-2 high-speed TTL-compatible FET multiplexer/ demultiplexer. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

When the select (S) input is low, port A is connected to port B1 and R_{INT} is connected to port B2. When S is high, port A is connected to port B2 and R_{INT} is connected to port B1.

The SN74CBT16292 is characterized for operation from –40°C to 85°C.

DGG, DGV, OR DL PACKAGE (TOP VIEW)

1				1
s[1	\cup	56	NC
1A [2		55	NC
NC [3		54]1B1
2A [4		53] 1B2
NC [5		52	2B1
3A [6		51	2B2
NC [7		50	3B1
GND [8		49	GND
4A 🛚	9		48	3B2
NC	10		47	4B1
5A 🛚	11		46	4B2
NC [12		45	5B1
6A 🛚	13		44	5B2
NC	14		43	6B1
7A	15		42	6B2
NC [16		41] 7B1
v _{cc} [17		40	7B2
8A 🛚	18		39	8B1
GND [19		38	GND
NC [20		37	8B2
9A 🛚	21		36	9B1
NC [22		35] 9B2
10A 🛚	23		34	10B1
NC [24		33	10B2
11A	25		32	11B1
NC [26		31] 11B2
12A	27		30	12B1
NC [28		29	12B2

NC - No internal connection

FUNCTION TABLE

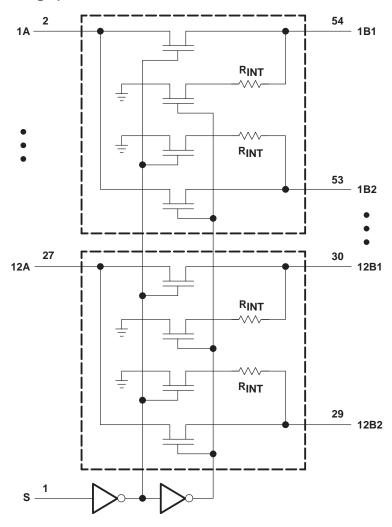
INPUT S	FUNCTION
L	A port = B1 port R _{INT} = B2 port
Н	A port = B2 port R _{INT} = B1 port

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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}		0.5 V to 7 V
Input voltage range, V _I (see Note 1)		0.5 V to 7 V
Continuous channel current		128 mA
Input clamp current, I_{IK} ($V_I < 0$)		–50 mA
Package thermal impedance, θ _{JA} (see Note 2)	: DGG package	81°C/W
	DGV package	86°C/W
	DL package	74°C/W
Storage temperature range, T _{stq}		. −65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.



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recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
VCC	Supply voltage	4	5.5	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		0.8	V
TA	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at VCC or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAI	RAMETER	TEST CONDITIONS		MIN	TYP [†]	MAX	UNIT	
VIK		$V_{CC} = 4.5 \text{ V},$	$I_{I} = -18 \text{ mA}$				-1.2	V
ΙĮ		$V_{CC} = 5.5 \text{ V},$	$V_I = V_{CC}$ or GND				±5	μΑ
Icc		V _{CC} = 5.5 V,	I _O = 0,	$V_I = V_{CC}$ or GND			3	μΑ
∆lcc [‡]	Control input	V _{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V _{CC} or GND			2.5	mA
Ci	Control input	V _I = 3 V or 0				3		pF
C _{io}		$V_{CC} = 0$,	$V_O = 3 V \text{ or } 0$			8		pF
		$V_{CC} = 4 \text{ V},$ TYP at $V_{CC} = 4 \text{ V}$	V _I = 2.4 V,	I _I = 15 mA		10	20	
r _{on} §			V ₁ = 0	I _I = 64 mA		3	7	Ω
		V _{CC} = 4.5 V		I _I = 30 mA		3	7	
			V _I = 2.4 V,	I _I = 15 mA		5	15	

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4 V	V _{CC} = 5 V ± 0.5 V		UNIT
	(INFOT)	(001701)	MIN MAX	MIN	MAX	
$t_{\sf pd}\P$	A or B	B or A	0.5		0.25	ns
t _{en}	S	A or B	6.8	1	6	ns
^t dis	S	A or B	7	1	6.3	ns

[¶] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	PARAMETER DESCRIPTION	V _{CC} = 4 V		V _{CC} = 5 V ± 0.5 V		UNIT
			MAX	MIN	MAX	
tmbb#	Make-before-break time	0	2	0	2	ns

[#]The make-before-break time is the time interval between make and break, during the transition from one selected port to the other.

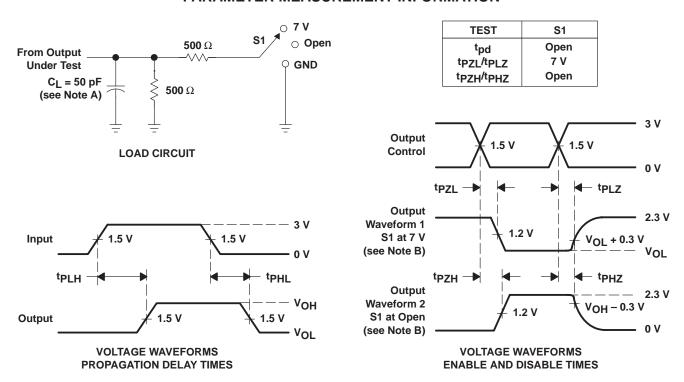


[‡]This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

[§] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

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PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when connected to the internal 500-Ω pulldown resistor. Waveform 2 is for an output with internal conditions such that the output is high except when connected to the internal 500-Ω pulldown resistor.
- C. All pulse inputs and DC inputs are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis. Z = RINT = 500 Ω
- F. tpzL and tpzH are the same as t_{en} . Z = R_{INT} = 500 Ω
- G. tplH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

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