16-BIT TRANSPARENT D-TYPE LATCH
WITH 3-STATE OUTPUTS

SCES156F – DECEMBER 1998 – REVISED FEBRUARY 2000

- **Member of the Texas Instruments** *Widebus*™ **Family**
- *EPIC*™ **(Enhanced-Performance Implanted CMOS) Submicron Process**
- *DOC*™ **(Dynamic Output Control) Circuit Dynamically Changes Output Impedance, Resulting in Noise Reduction Without Speed Degradation**
- **Dynamic Drive Capability Is Equivalent to Standard Outputs With I_{OH} and I_{OL} of $\pm$24 mA at 2.5-V V_{CC}**
- **Overvoltage-Tolerant Inputs/Outputs Allow Mixed-Voltage-Mode Data Communications**

- I_{off} **Supports Partial-Power-Down Mode Operation**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **Package Options Include Plastic Thin Shrink Small-Outline (DGG) and Thin Very Small-Outline (DGV) Packages**

description

A Dynamic Output Control (DOC) circuit is implemented, which, during the transition, initially lowers the output impedance to effectively drive the load and, subsequently, raises the impedance to reduce noise. Figure 1 shows typical V_{OL} vs I_{OL} and V_{OH} vs I_{OH} curves to illustrate the output impedance and drive capability of the circuit. At the beginning of the signal transition, the DOC circuit provides a maximum dynamic drive that is equivalent to a high-drive standard-output device. For more information, refer to the TI application reports, *AVC Logic Family Technology and Applications*, literature number SCEA006, and *Dynamic Output Control (DOC*™*) Circuitry Technology and Applications*, literature number SCEA009.
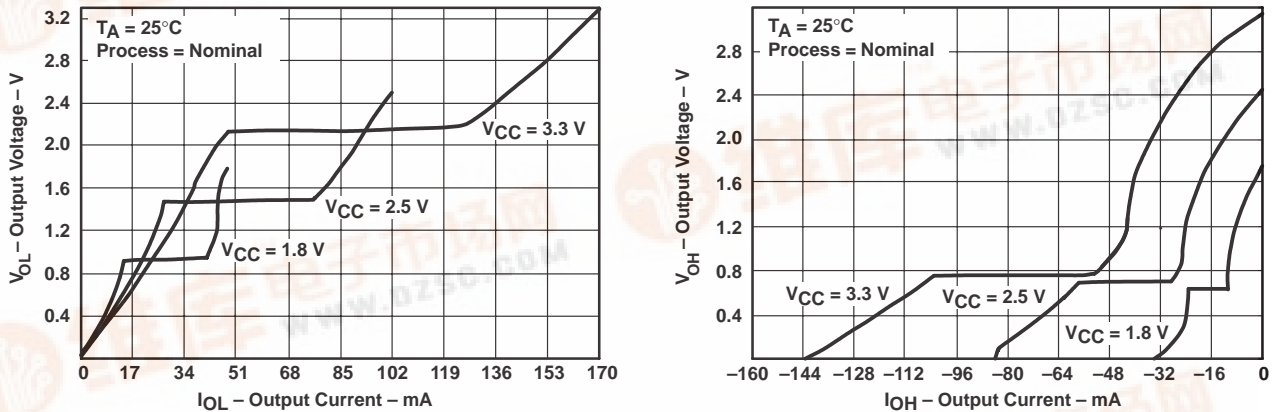

Figure 1. Output Voltage vs Output Current

This 16-bit transparent D-type latch is operational at 1.2-V to 3.6-V V_{CC}, but is designed specifically for 1.65-V to 3.6-V V_{CC} operation.

The SN74AVC16373 is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. This device can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

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SN74AVC16373
16-BIT TRANSPARENT D-TYPE LATCH
WITH 3-STATE OUTPUTS

description (continued)

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components. $\overline{OE}$ does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.
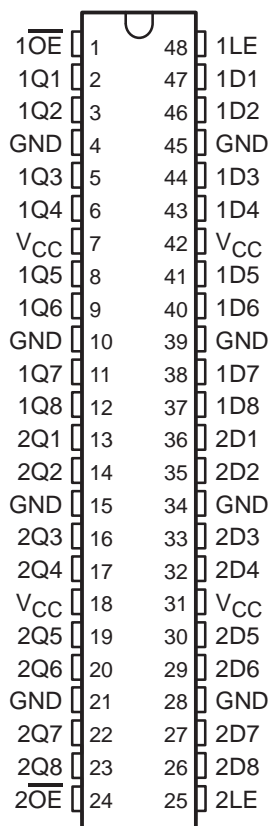
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The SN74AVC16373 is characterized for operation from $-40°C$ to $85°C$.

terminal assignments

DGG OR DGV PACKAGE
(TOP VIEW)

1$\overline{OE}$	1		48	1LE
1Q1	2		47	1D1
1Q2	3		46	1D2
GND	4		45	GND
1Q3	5		44	1D3
1Q4	6		43	1D4
V_{CC}	7		42	V_{CC}
1Q5	8		41	1D5
1Q6	9		40	1D6
GND	10		39	GND
1Q7	11		38	1D7
1Q8	12		37	1D8
2Q1	13		36	2D1
2Q2	14		35	2D2
GND	15		34	GND
2Q3	16		33	2D3
2Q4	17		32	2D4
V_{CC}	18		31	V_{CC}
2Q5	19		30	2D5
2Q6	20		29	2D6
GND	21		28	GND
2Q7	22		27	2D7
2Q8	23		26	2D8
2$\overline{OE}$	24		25	2LE

FUNCTION TABLE
(each 8-bit latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol[†]
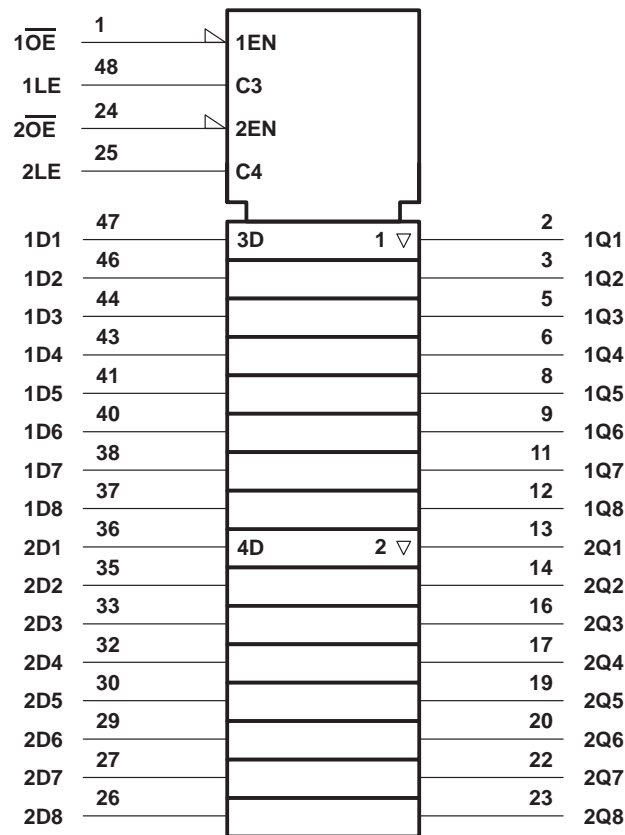
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)
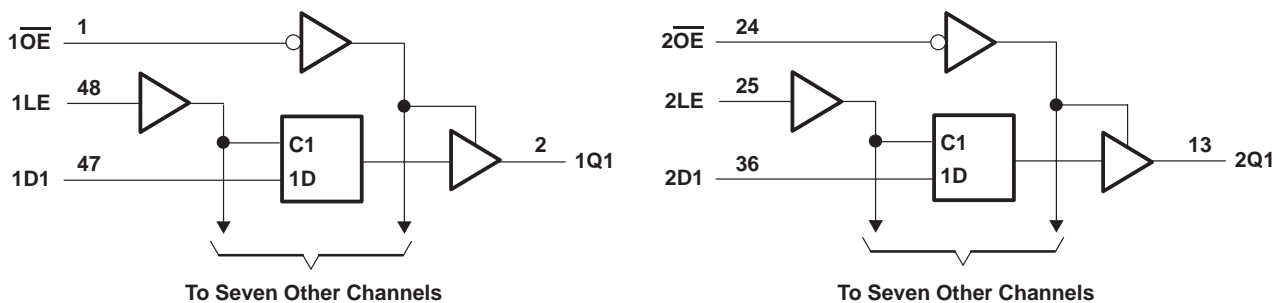
To Seven Other Channels

To Seven Other Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... –0.5 V to 4.6 V

Input voltage range, V_I (see Note 1) .... –0.5 V to 4.6 V

Voltage range applied to any output in the high-impedance or power-off state, V_O
   (see Note 1) .... –0.5 V to 4.6 V

Voltage range applied to any output in the high or low state, V_O
   (see Notes 1 and 2) .... –0.5 V to V_{CC} + 0.5 V

Input clamp current, I_{IK} (V_I < 0) .... –50 mA

Output clamp current, I_{OK} (V_O < 0) .... –50 mA

Continuous output current, I_O .... ±50 mA

Continuous current through each V_{CC} or GND .... ±100 mA

Package thermal impedance, θ_{JA} (see Note 3): DGG package .... 70°C/W
                                            DGV package .... 58°C/W

Storage temperature range, T_{stg} .... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
         2. The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.
         3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.4	3.6	V
		Data retention only	1.2		
V_{IH}	High-level input voltage	V_{CC} = 1.2 V	V_{CC}		V
		V_{CC} = 1.4 V to 1.6 V	$0.65 \times V_{CC}$		
		V_{CC} = 1.65 V to 1.95 V	$0.65 \times V_{CC}$		
		V_{CC} = 2.3 V to 2.7 V	1.7		
		V_{CC} = 3 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 1.2 V		GND	V
		V_{CC} = 1.4 V to 1.6 V		$0.35 \times V_{CC}$	
		V_{CC} = 1.65 V to 1.95 V		$0.35 \times V_{CC}$	
		V_{CC} = 2.3 V to 2.7 V		0.7	
		V_{CC} = 3 V to 3.6 V		0.8	
V_I	Input voltage		0	3.6	V
V_O	Output voltage	Active state	0	V_{CC}	V
		3-state	0	3.6	
I_{OHS}	Static high-level output current†	V_{CC} = 1.4 V to 1.6 V		−2	mA
		V_{CC} = 1.65 V to 1.95 V		−4	
		V_{CC} = 2.3 V to 2.7 V		−8	
		V_{CC} = 3 V to 3.6 V		−12	
I_{OLS}	Static low-level output current†	V_{CC} = 1.4 V to 1.6 V		2	mA
		V_{CC} = 1.65 V to 1.95 V		4	
		V_{CC} = 2.3 V to 2.7 V		8	
		V_{CC} = 3 V to 3.6 V		12	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 1.4 V to 3.6 V		5	ns/V
T_A	Operating free-air temperature		−40	85	°C

† Dynamic drive capability is equivalent to standard outputs with I_{OH} and I_{OL} of ±24 mA at 2.5-V V_{CC}. See Figure 1 for V_{OL} vs I_{OL} and V_{OH} vs I_{OH} characteristics. Refer to the TI application reports, **AVC Logic Family Technology and Applications**, literature number **SCEA006**, and **Dynamic Output Control (DOC™) Circuitry Technology and Applications**, literature number **SCEA009**.

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
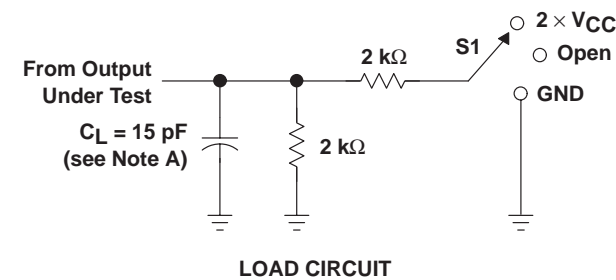
SN74AVC16373
16-BIT TRANSPARENT D-TYPE LATCH
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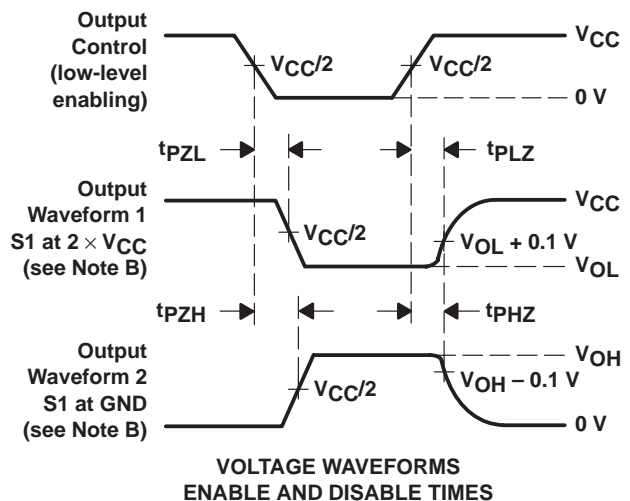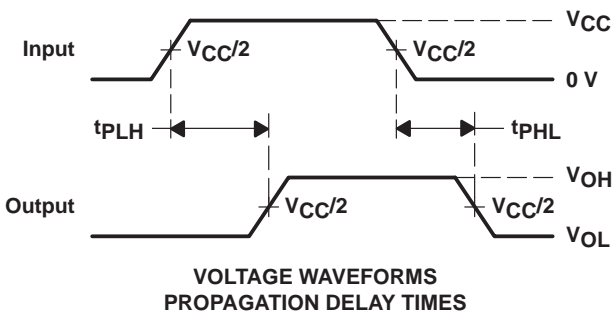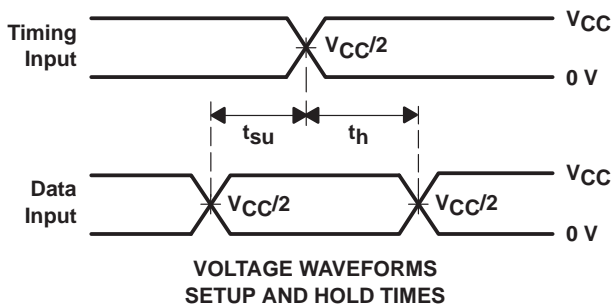## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP†	MAX	UNIT
V_{OH}		$I_{OHS} = -100\ \mu A$		1.4 V to 3.6 V	$V_{CC}-0.2$			V
		$I_{OHS} = -2\ mA,$	$V_{IH} = 0.91\ V$	1.4 V	1.05			
		$I_{OHS} = -4\ mA,$	$V_{IH} = 1.07\ V$	1.65 V	1.2			
		$I_{OHS} = -8\ mA,$	$V_{IH} = 1.7\ V$	2.3 V	1.75			
		$I_{OHS} = -12\ mA,$	$V_{IH} = 2\ V$	3 V	2.3			
V_{OL}		$I_{OLS} = 100\ \mu A$		1.4 V to 3.6 V			0.2	V
		$I_{OLS} = 2\ mA,$	$V_{IL} = 0.49\ V$	1.4 V			0.4	
		$I_{OLS} = 4\ mA,$	$V_{IL} = 0.57\ V$	1.65 V			0.45	
		$I_{OLS} = 8\ mA,$	$V_{IL} = 0.7\ V$	2.3 V			0.55	
		$I_{OLS} = 12\ mA,$	$V_{IL} = 0.8\ V$	3 V			0.7	
I_I	Control inputs	$V_I = V_{CC}$ or GND		3.6 V			±2.5	μA
I_{off}		V_I or $V_O = 3.6\ V$		0			±10	μA
I_{OZ}		$V_O = V_{CC}$ or GND		3.6 V			±10	μA
I_{CC}		$V_I = V_{CC}$ or GND,	$I_O = 0$	3.6 V			40	μA
C_i	Control inputs	$V_I = V_{CC}$ or GND		2.5 V		3		pF
				3.3 V		3		
	Data inputs	$V_I = V_{CC}$ or GND		2.5 V		2.5		
				3.3 V		2.5		
C_o	Outputs	$V_O = V_{CC}$ or GND		2.5 V		6.5		pF
				3.3 V		6.5		

† Typical values are measured at V_{CC} = 2.5 V and 3.3 V, T_A = 25°C.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 2 through 5)

		$V_{CC} = 1.2\ V$		$V_{CC} = 1.5\ V$ $\pm 0.1\ V$		$V_{CC} = 1.8\ V$ $\pm 0.15\ V$		$V_{CC} = 2.5\ V$ $\pm 0.2\ V$		$V_{CC} = 3.3\ V$ $\pm 0.3\ V$		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high					2.2		2		1.8		ns
t_{su}	Setup time, data before LE↓	1.7		1.2		1.1		0.9		0.8		ns
t_h	Hold time, data after LE↓	2		1.1		1.1		1.1		1		ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 2 through 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.2\ V$	$V_{CC} = 1.5\ V$ $\pm 0.1\ V$		$V_{CC} = 1.8\ V$ $\pm 0.15\ V$		$V_{CC} = 2.5\ V$ $\pm 0.2\ V$		$V_{CC} = 3.3\ V$ $\pm 0.3\ V$		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	Q	5.8	1.2	6.8	1	5.7	0.8	3.3	0.7	2.8	ns
	LE		7.2	1.4	8.3	1.1	6.6	0.8	4	0.7	3.2	
t_{en}	$\overline{OE}$	Q	7.4	1.6	8.8	1.6	6.7	1.4	4.3	0.7	3.4	ns
t_{dis}	$\overline{OE}$	Q	8.4	2.5	9.4	2.3	7.8	1.3	4.2	1.2	3.9	ns

operating characteristics, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		$V_{CC} = 1.8$ V	$V_{CC} = 2.5$ V	$V_{CC} = 3.3$ V	UNIT
				TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	Outputs enabled	$C_L = 0$, f = 10 MHz	40	43	47	pF
		Outputs disabled		20	22	24	

PARAMETER MEASUREMENT INFORMATION
$V_{CC} = 1.2$ V AND 1.5 V $\pm$ 0.1 V
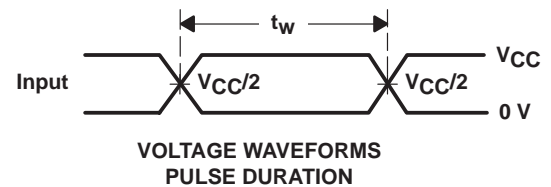
LOAD CIRCUIT

TEST	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open $2 \times V_{CC}$ GND
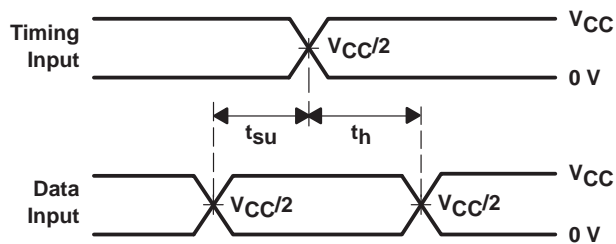
**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**
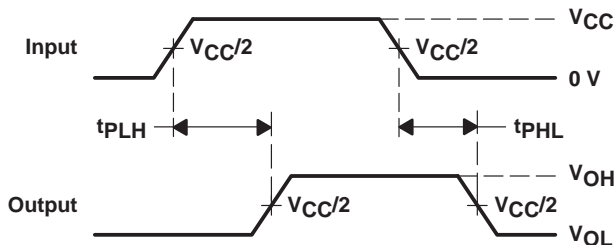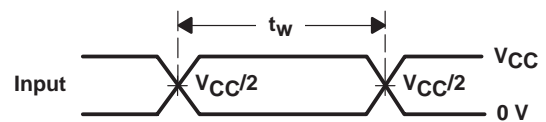
**VOLTAGE WAVEFORMS
PULSE DURATION**

**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES**

**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES**

NOTES: A. C_L includes probe and jig capacitance.
      B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
         Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
      C. All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2$ ns, $t_f \leq 2$ ns.
      D. The outputs are measured one at a time with one transition per measurement.
      E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
      F. t_{PZL} and t_{PZH} are the same as t_{en}.
      G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 2. Load Circuit and Voltage Waveforms

Texas
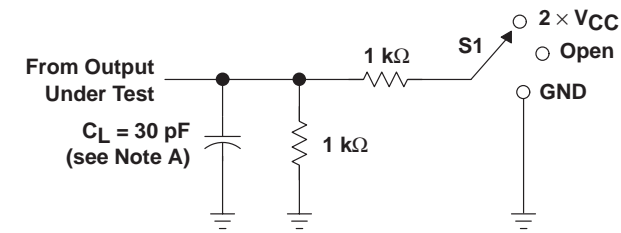Instruments

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 1.8 V $\pm$ 0.15 V

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PULSE DURATION

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

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Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 10 MHz, Z_O = 50 Ω, $t_r \leq$ 2 ns, $t_f \leq$ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
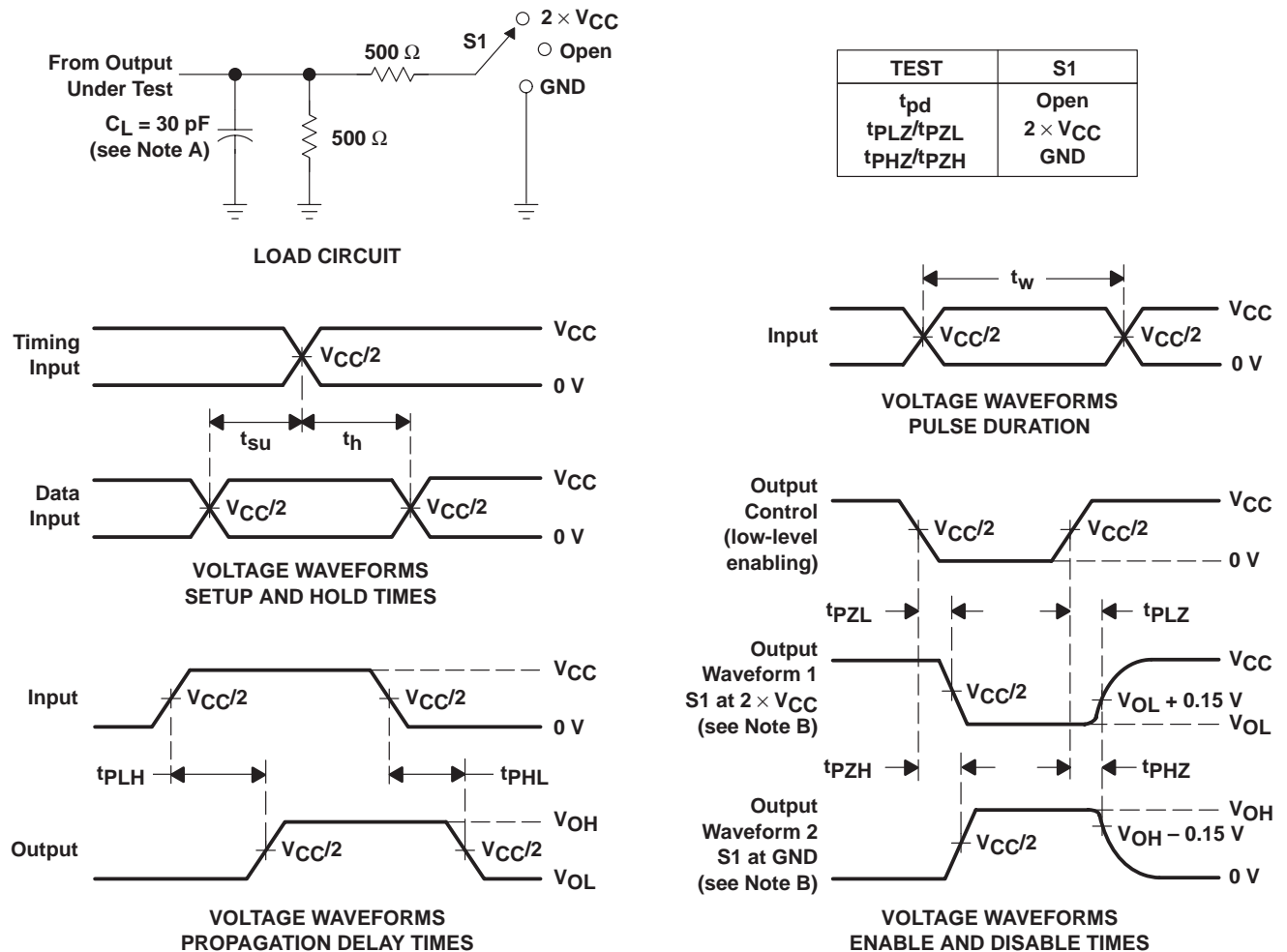
Figure 3. Load Circuit and Voltage Waveforms

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PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.5 V $\pm$ 0.2 V

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT

VOLTAGE WAVEFORMS
PULSE DURATION

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
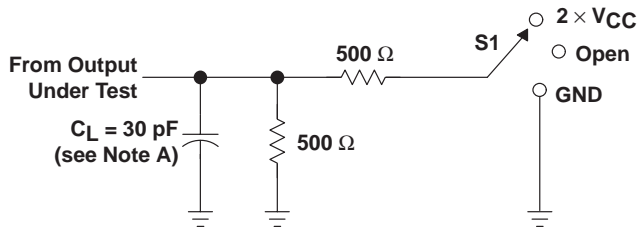G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 4. Load Circuit and Voltage Waveforms

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PARAMETER MEASUREMENT INFORMATION
V_{CC} = 3.3 V $\pm$ 0.3 V

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PULSE DURATION

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

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B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 10 MHz, Z_O = 50 Ω, $t_r \leq$ 2 ns, $t_f \leq$ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 5. Load Circuit and Voltage Waveforms

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