Aimtron
圓創科技股份有限公司

AT6392

4-Channel BTL Drive for CD Players

Features

- HSOP-28 package enables the smallest configuration.
- PWM input is filtered by the internal primary filter, eliminating the need for attached resistors and capacitors, thereby helping reduce the number of components. Resistor and capacitor time constants can also be changed with attached components.
- Internal mute circuit.
- Thermal shutdown circuit is contained.
- Level-shift circuit is contained.

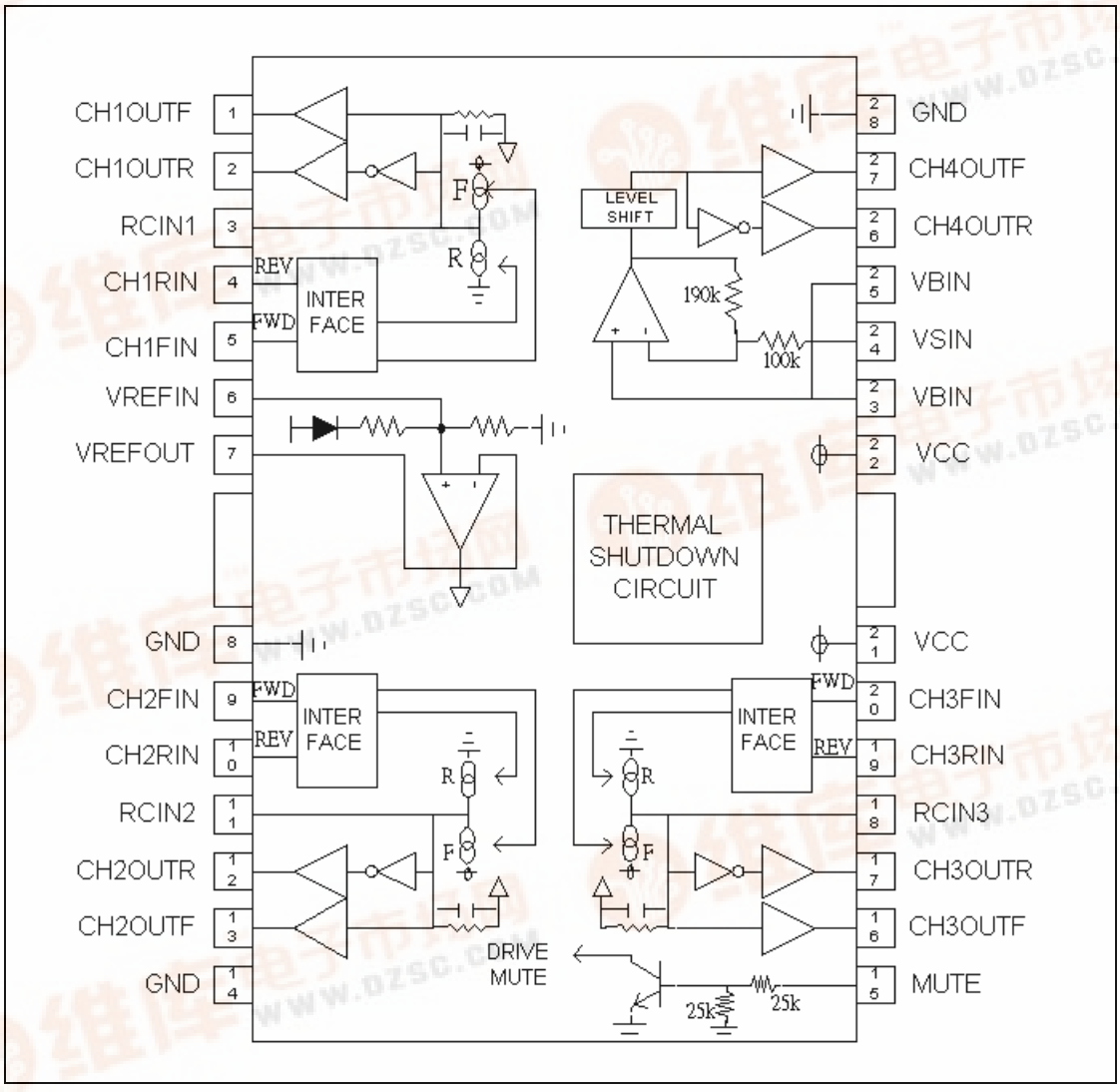
Description

The AT6392 is a 4-channel BTL driver for CD player motors and actuators. It has an internal primary filter, and can be directly connected (without attached components) to the servo PWM output of all drivers other than the spindle driver.

Applications

CD players, CD-ROM drives

Block Diagram



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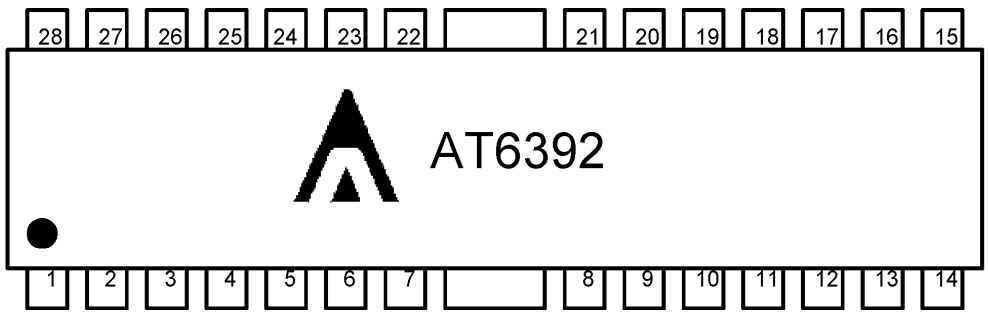
Pin Descriptions

Pin No.	Pin name	Function
1	CH1OUT F	Drive channel 1 forward output
2	CH1OUT R	Drive channel 1 reverse output
3	RC IN1	Connect to attach resistor/capacitor (1)
4	CH1 RIN	Drive channel 1 reverse input
5	CH1 FIN	Drive channel 1 forward input
6	VREF IN	Internal reference amplifier input
7	VREF OUT	Internal reference amplifier output
8	GND	Ground for internal reference and internal power circuit
9	CH2 FIN	Drive channel 2 forward input
10	CH2 RIN	Drive channel 2 reverse input
11	RC IN2	Connect to attach resistor/capacitor (2)
12	CH2OUT R	Drive channel 2 reverse output
13	CH2OUT F	Drive channel 2 forward output
14	GND	Ground for internal reference and internal power circuit
15	MUTE	Drive mute control input
16	CH3OUT F	Drive channel 3 forward output
17	CH3OUT R	Drive channel 3 reverse output
18	RC IN3	Connect to attach resistor/capacitor (3)
19	CH3 RIN	Drive channel 3 reverse input
20	CH3 FIN	Drive channel 3 forward input
21	V_{cc}	Power supply
22	V_{cc}	Power supply
23	VBIN	Drive channel 4 bias input*
24	VSIN	Drive channel 4 input
25	VBIN	Drive channel 4 bias input*
26	CH4OUT R	Drive channel 4 reverse output
27	CH4OUT F	Drive channel 4 forward output
28	GND	Ground for internal reference and internal power circuit

*Pin23 and pin25 are shorted internally.

PinOut



Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits	unit
Power supply voltage	V_{CC}	18	V
Power dissipation	P_d	1.6*1	W
Operating temperature	T_{opr}	-30~+85	°C
Storage temperature	T_{stg}	-55~+150	°C

*1 Reduce by 13.6 mW for each increase in T_a of 1°C over 25°C.
When mounted on a 50*50 *1.0 mm phenol paper PCB.

Recommended operating conditions (Ta = 25°C)

Parameter	Symbol	Limits	unit
Power supply voltage	V_{CC}	6~12*2	V

*2 Set the power supply voltage according to power dissipation.

Electrical characteristics (unless otherwise noted, Ta = 25°C, V_{CC} = 8V, f = 1kHz, R_L = 8Ω)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Quiescent current	I_Q	5	12	18	mA	No load
Bias pin voltage	V_{BIAS}	3.4	3.68	4.00	V	
Bias pin voltage variation	ΔV_{BIAS}	-30	-	30	mV	1mA Source, sink
Mute-off voltage	V_{MOFF}	2.0	-	-	V	
Mute-on voltage	V_{MON}	-	-	0.5	V	
<Drive (other than spindle)>						
Input high level voltage	V_{IH}	2.4	-	-	V	
Input low level voltage	V_{IL}	-	-	0.5	V	
Input high level current	I_{IH}	170	310	450	μA	V_{IN}=5V
Input low level current	I_{IL}	-10	-	0	μA	V_{IN}=0V
Output voltage, offset	V_{OO}	-30	-	30	mV	(same for spindle)
Output high level voltage	V_{OHD}	4.90	5.40	-	V	F_{IN}=5V, R_{IN}=0V
Output low level voltage	V_{OLD}	-	1.50	2.00	V	F_{IN}=0V, R_{IN}=5V
Constant current	I_{CONST}	14	22	30	μA	
Internal integral capacitance	C	-	24	-	pF	
Current pulse rise time1	Δtr	-	0.08	1	μS	At startup
Current pulse fall time2	Δtf	-	0.55	1	μS	At shutdown
Current pulse time differential	Δtr-f	-160	-	160	μS	
Drive linearity	LIN	90	100	110	%	V_{IN}=V_{REF}± 0.5, 1, 1.5*1
Ripple rejection	RR	-	70	-	dB	V_{IN}=100mV_{rms}, 100Hz
<Spindle driver>						
Input bias current	I_B	-	10	300	nA	
Synchronous input voltage	V_{ICM}	1.6	-	6.4	V	
Max. output voltage high	V_{OHD}	4.90	5.40	-	V	
Max. output voltage low	V_{OLD}	-	1.50	2.00	V	
Voltage gain	G_{VC}	8.0	10.5	13	dB	
Slew rate	SR	-	2	-	V/μS	
Ripple rejection	RR_S	-	70	-	dB	V_{IN}=100mV_{rms}, 100Hz

*1 if V_O=V01 when V_{IN}=V_{REF}± 0.5V, V_O=V02 when V_{IN}=V_{REF}± 1.0V, and V_O=V03 when V_{IN}=V_{REF}± 1.5V, then L_{IN}= (V03*V02)/(V02*V01)*100%

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Circuit Operation

(1) Fig. 2 shows the inputs from the digital servo IC for CH1-CH3 drivers (all drivers except the spindle). SW1 is on when the forward input signal (HIGH level, over 2.4V) is present. SW2 is on when the reverse input signal is present (Fig. 1). The constant current (I_1) at this time enters the RC and generates an integral waveform based on the duty of the input waveform. The BTL is output from BUF1 and BUF2 (Fig. 3).

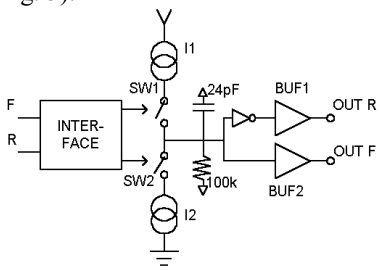


Fig. 1

To maintain the HIGH level with forward (or reverse) in-put, the DC voltage generated at point A is :

$$I_1 \times R \fallingdotseq 2.5V \text{ (reverse :- 2.5V)}$$

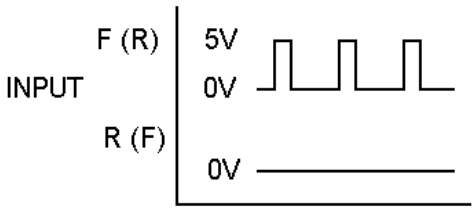


Fig. 2

This is the voltage generated relative V_{REF}. The setting is such that a voltage differential of 5V is generated be-tween output pins. The time constant is :

$$R \times C = 2.4\ \mu sec$$

This can be increased by inserting a capacitor between point A (pins 3, 11 and 18) and V_{REF} . The constant current (Iconst) given in the electrical characteristics refers to I_1 and I_2 in Fig.1.

(2) CH4 driver (spindle driver) Pins 23 and 25 are shorted inside the IC. Bias amplitudes are the primary type of inputs assumed.

F	R	SW2	SW1
L	L	OFF	OFF
L	H	OFF	ON
H	L	ON	OFF
H	H	OFF	OFF

H...2.4V Max.
L...0.5V Min.

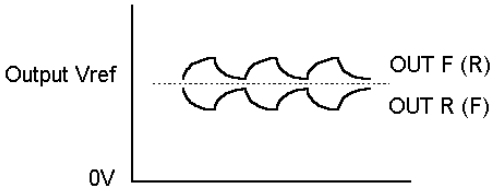


Fig. 3

The level shift circuit converts the pre-stage amplifier output (centered on the bias level and impressed on pins 23 and 25) to positive and negative amplitudes centered on V_{REF} . The level shift circuit's output is BTL-output from the buffer amplifier.
Because of the high input impedance, the IC is designed to accommodate a filter comprising attached resistors and capacitors.

(Example) For secondary filters

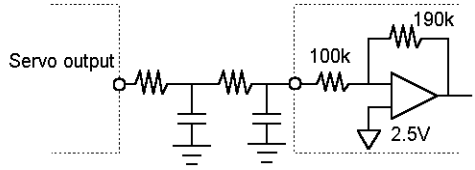
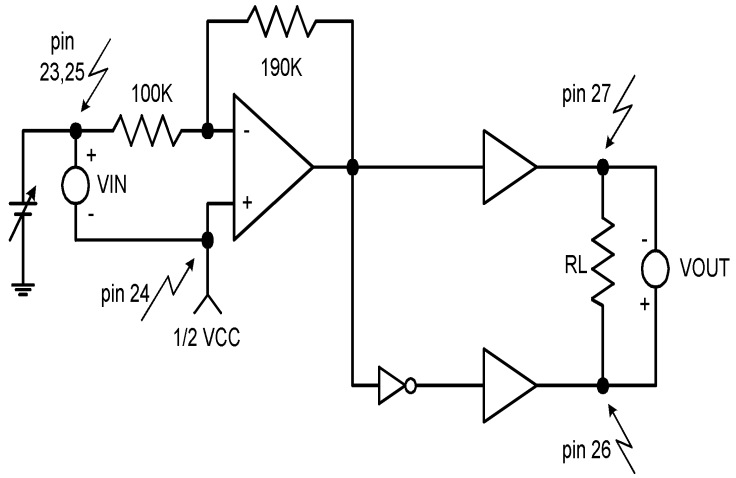


Fig. 4

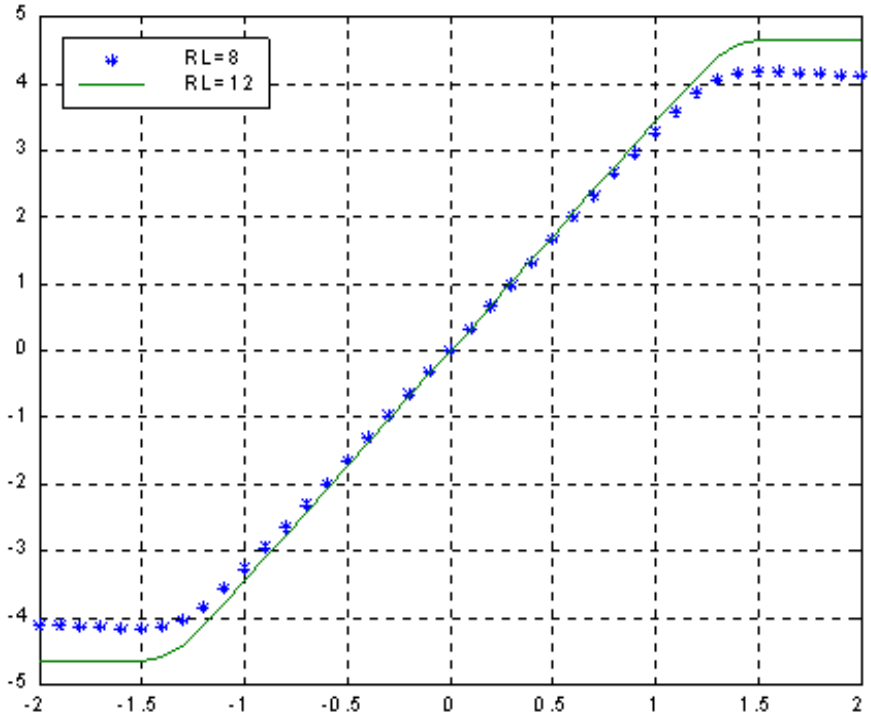
Operation notes

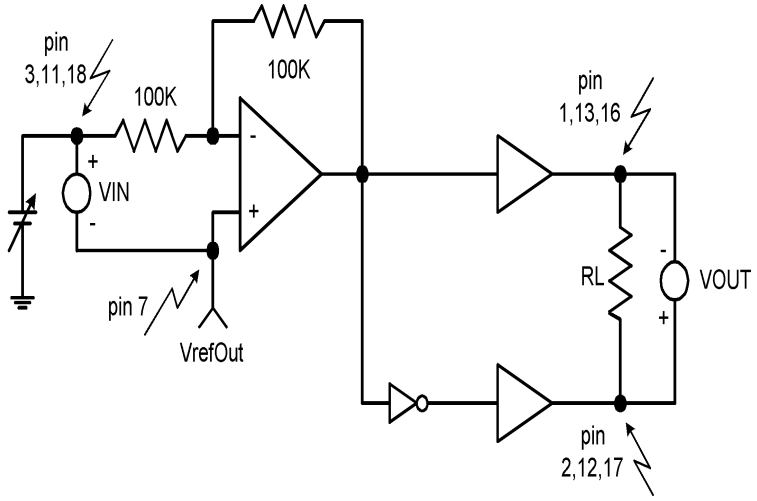
(1) The AT6392 has an internal thermal shutdown circuit. Output current is muted when the chip temperature exceeds 180^0C (typically).
(2) The output current can also be muted by lowering the mute pin (pin 15) voltage below 0.5V.
(3) All four driver output channels are muted during thermal shutdown, muting and a drop in bias pin voltage. No other components are muted.

I/O Electrical Characteristics

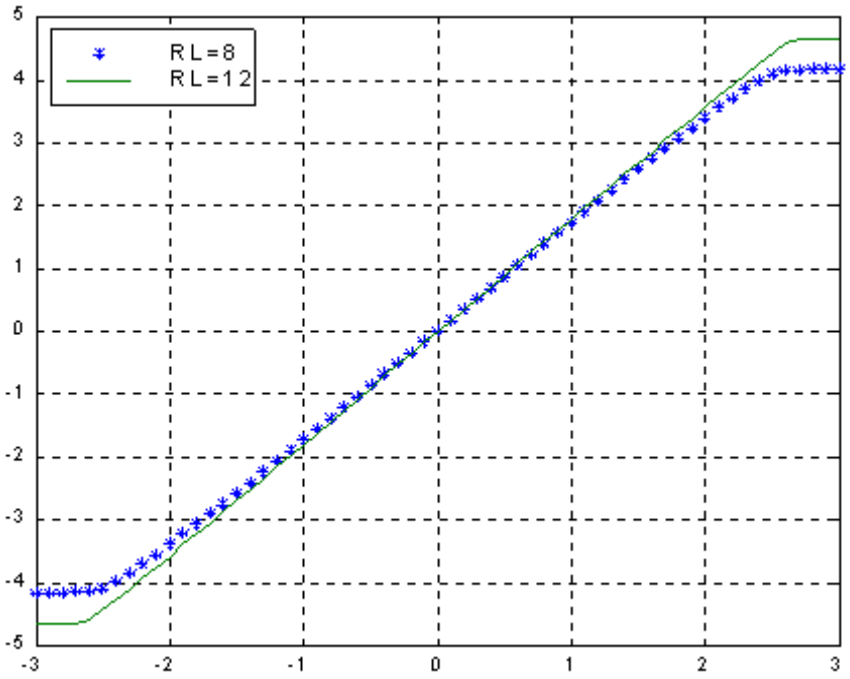


CH4 Output Drive

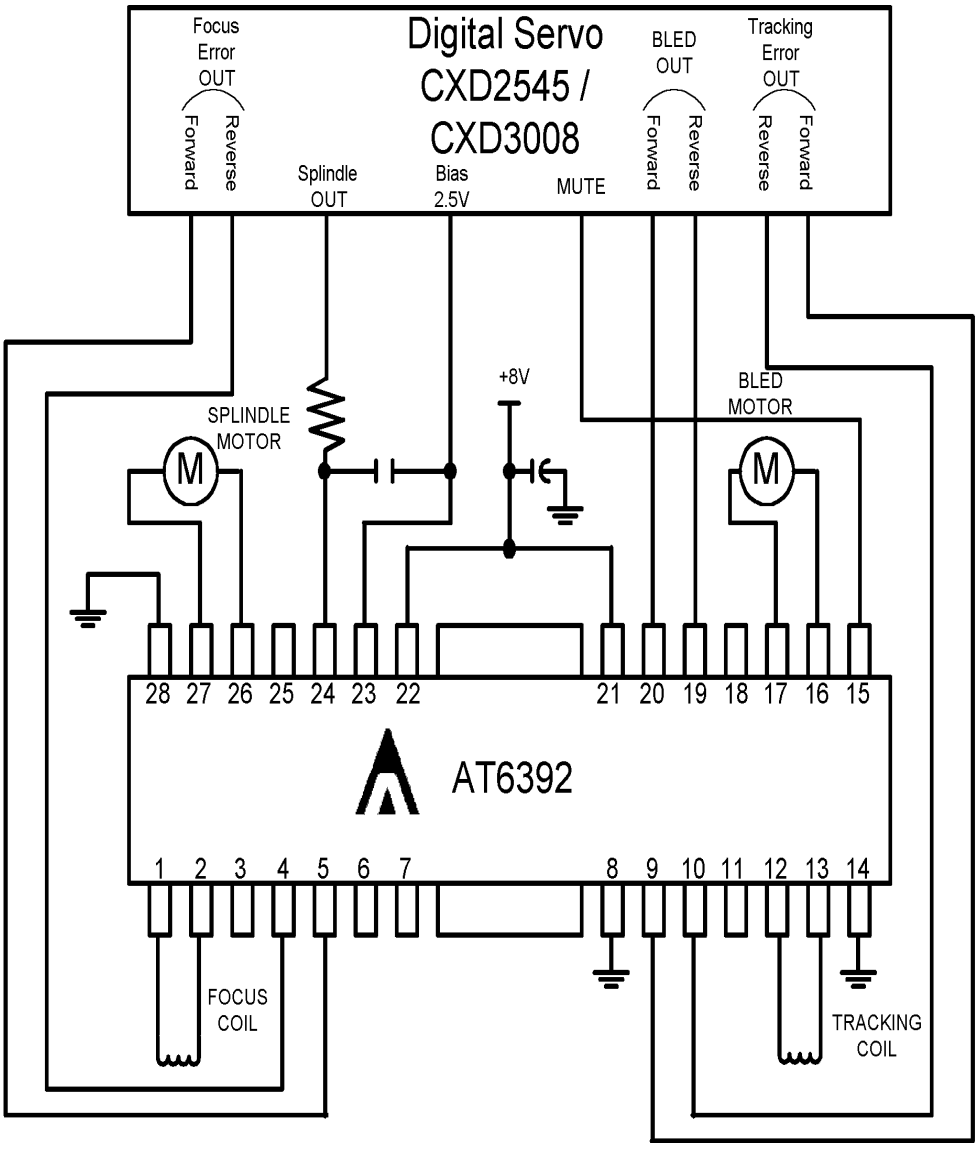




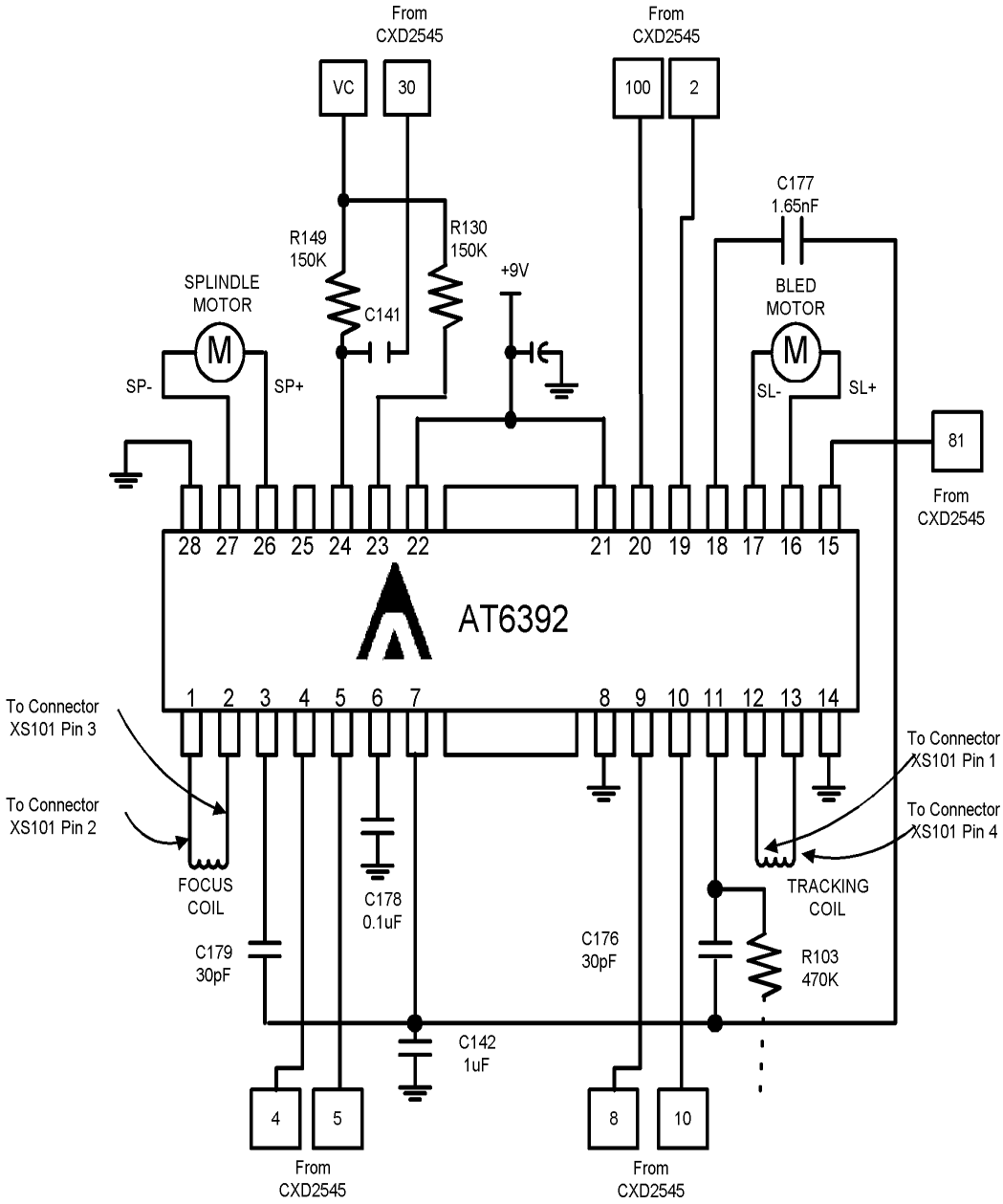
CH1/2/3 Output Drive



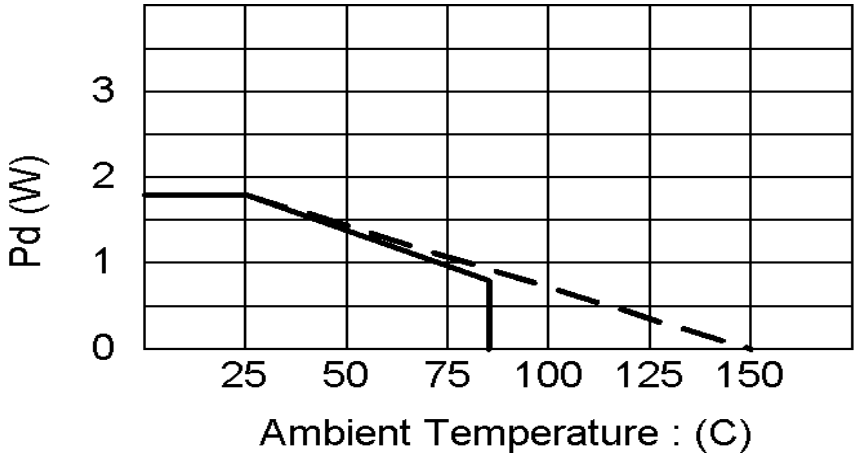
Application Circuit



VCD Player Motor Driver Circuit



Power Dissipation (Ta = 25°C) **(Pd: power dissipation)**



Condition: mount on 50x50 mm^2 t=1.0mm paper phenol PCB

Package Outlines (units:mm): HSOP-28