

SN74CBT16390
16-BIT TO 32-BIT FET MULTIPLEXER/DEMULTIPLEXER BUS SWITCH

SCDS035C – OCTOBER 1997 – REVISED OCTOBER 1998

- **5- Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input Levels**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Package Options Include Plastic Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV), and 300-mil Shrink Small-Outline (DL) Packages**

description

The SN74CBT16390 is a 16-bit to 32-bit switch used in applications in which two separate data paths must be multiplexed onto, or demultiplexed from, a single path. This device can be used for memory interleaving, in which two different banks of memory must be addressed simultaneously. This also can be used to connect or isolate the PCI bus to one or two slots simultaneously.

Two output enables ($\overline{OE1}$ and $\overline{OE2}$) control the data flow. When $\overline{OE1}$ is low, A port is connected to 1B port. When $\overline{OE2}$ is low, A port is connected to 2B port. When both $\overline{OE1}$ and $\overline{OE2}$ are low, the A port is connected to both 1B and 2B ports. The control inputs can be driven with a 5-V CMOS, 5-V TTL, or an LVTTTL driver.

The SN74CBT16390 is characterized for operation from -40°C to 85°C .

**DGG, DGV, OR DL PACKAGE
(TOP VIEW)**

A1	1	56	1B1
2B1	2	55	1B2
2B2	3	54	A2
A3	4	53	1B3
2B3	5	52	1B4
2B4	6	51	A4
A5	7	50	1B5
2B5	8	49	1B6
2B6	9	48	A6
A7	10	47	1B7
2B7	11	46	1B8
2B8	12	45	A8
GND	13	44	GND
V _{CC}	14	43	V _{CC}
A9	15	42	1B9
2B9	16	41	1B10
2B10	17	40	A10
A11	18	39	1B11
2B11	19	38	1B12
2B12	20	37	A12
A13	21	36	1B13
2B13	22	35	1B14
2B14	23	34	A14
A15	24	33	1B15
2B15	25	32	1B16
2B16	26	31	A16
NC	27	30	$\overline{OE1}$
NC	28	29	$\overline{OE2}$

NC – No internal connection

FUNCTION TABLE

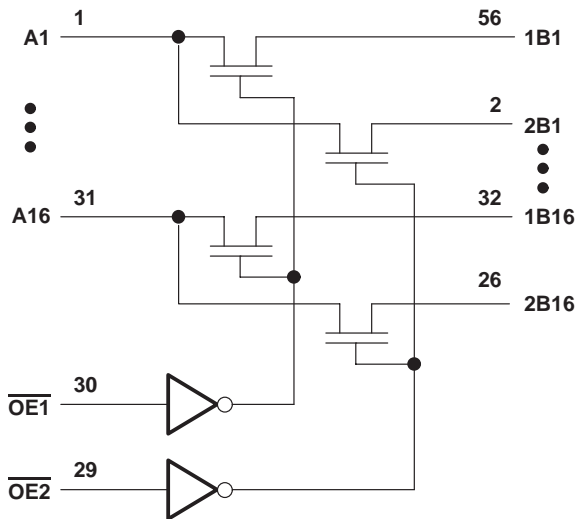
INPUTS		FUNCTION
$\overline{OE1}$	$\overline{OE2}$	
L	L	A = 1B and A = 2B
L	H	A = 1B
H	L	A = 2B
H	H	Isolation

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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Continuous channel current	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	
DGG package	81°C/W
DGV package	86°C/W
DL package	74°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

	MIN	MAX	UNIT
V_{CC} Supply voltage	4.5	5.5	V
V_{IH} High-level control input voltage	2		V
V_{IL} Low-level control input voltage		0.8	V
T_A Operating free-air temperature	–40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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SCDS035C – OCTOBER 1997 – REVISED OCTOBER 1998

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		$V_{CC} = 4.5\text{ V}$,	$I_I = -18\text{ mA}$			-1.2	V
I_I		$V_{CC} = 0$,	$V_I = 5.5\text{ V}$			10	μA
		$V_{CC} = 5.5\text{ V}$,	$V_I = 5.5\text{ V or GND}$			± 1	
I_{CC}		$V_{CC} = 5.5\text{ V}$,	$I_O = 0$,			3	μA
		$V_I = V_{CC} \text{ or GND}$					
ΔI_{CC}^\ddagger	Control inputs	$V_{CC} = 5.5\text{ V}$,	One input at 3.4 V,			2.5	mA
		Other input at V_{CC} or GND					
C_i	Control inputs	$V_I = 3\text{ V or 0}$				5	pF
$C_{io}(\text{OFF})$		$V_O = 3\text{ V or 0}$				5.5	pF
r_{on}^\S		$V_{CC} = 4.5\text{ V}$	$V_I = 0$			5	Ω
			$I_I = 64\text{ mA}$			7	
			$I_I = 30\text{ mA}$			5	
		$V_I = 2.4\text{ V}$,				7	12
		$I_I = 15\text{ mA}$					

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{pd}^\P	A or B	B or A		0.25	ns
t_{en}	\overline{OE}	A or B	1.3	5.9	ns
t_{dis}	\overline{OE}	A or B	1	5.3	ns

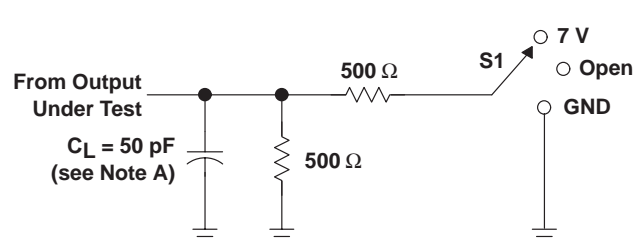
¶ The propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF, when driven by an ideal voltage source (zero output impedance).

SN74CBT16390

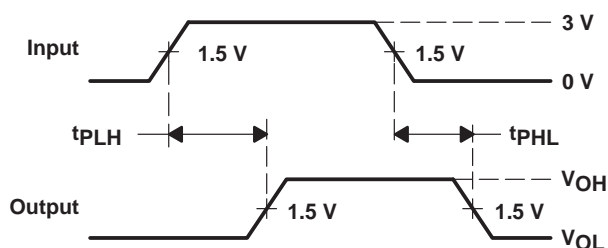
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PARAMETER MEASUREMENT INFORMATION

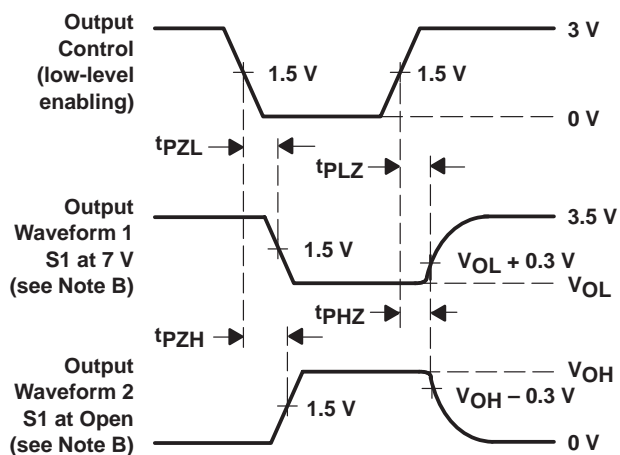


LOAD CIRCUIT



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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