19-2738; Rev 0; 1/03

MAXIM

3.3V Single LVDS Driver/Receiver

General Description

The MAX9164 high-speed LVDS driver/receiver is designed specifically for low-power point-to-point applications. The MAX9164 operates from a single 3.3V power supply, and is pin compatible with DS90LV019. The device features an independent differential driver and receiver.

The MAX9164 driver output uses a current-steering configuration to generate a 3.1mA drive current. The driver accepts a single-ended input and translates it to LVDS signals at speeds up to 200Mbps over controlled-impedance media of approximately 100Ω. The transmission media may be printed circuit board traces or cables. The enable logic input, DE, is used to enable or disable the driver.

The MAX9164 receiver detects a differential input as low as 100mV and translates it to single-ended output at speeds up to 200Mbps. The enable logic input, $\overline{RE}$, is used to enable or disable the receiver.

Inputs and outputs conform to the ANSI TIA/EIA-644 LVDS standard. The MAX9164 is offered in 14-lead SO and TSSOP packages, and is specified for operation from -40°C to +85°C.

Applications

Cell-Phone Base Stations
Add/Drop Muxes
Digital Cross-Connects
DSLAMs
Network Switches/Routers
Backplane Interconnect
Clock Distribution

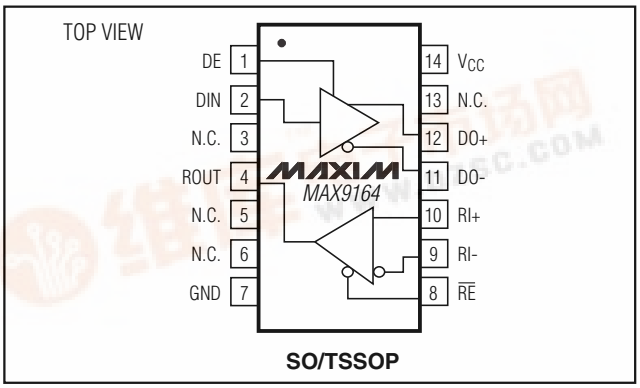
Features

- ♦ 3.3V Operation
- ♦ 35% Lower Power than DS90LV019
- ♦ 200Mbps Data Signaling Rate
- ♦ ±1V Common-Mode Range
- ♦ ±100mV Receiver Sensitivity
- ♦ Flow-Through Pinout
- ♦ Receiver Output High for Open Input

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9164ESD	-40°C to +85°C	14 SO
MAX9164EUD	-40°C to +85°C	14 TSSOP

Pin Configuration



SO/TSSOP

Typical Application Circuit

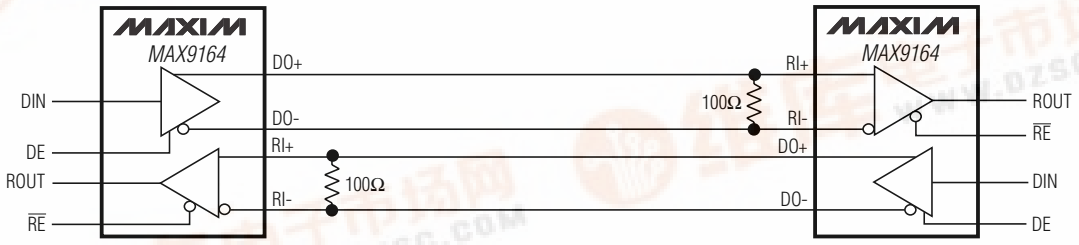


TABLE 1. DRIVER FUNCTION TABLE

INPUTS		OUTPUTS	
DE	DIN	DO+	DO-
H	L (≤ 0.8V)	L	H
H	H (≥ 2.0V)	H	L
H	(> 0.8V and < 2.0V)	Undefined	Undefined
L	X	Z	Z

X: High or low
Z: High impedance

TABLE 2. RECEIVER FUNCTION TABLE

INPUTS		OUTPUT
$\overline{RE}$	RI+ - RI-	ROUT
L	L (≤ -100mV)	L
L	H(≥ 100mV)	H
L	(> -100mV and < 100mV)	Undefined
L	Open	H
H	X	Z

X: High or low
Z: High impedance

3.3V Single LVDS Driver/Receiver

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +4.0V
DO+, DO-, RI+, RI- to GND .....-0.3V to +4.0V
DIN, ROUT, DE, $\overline{RE}$ to GND .....-0.3V to (V_{CC} + 0.3V)
Driver Short-Circuit Current .....Continuous
Continuous Power Dissipation (T_A = +70°C)
14-Pin SO (derate 8.3mW/°C above +70°C).....667mW
14-Pin TSSOP (derate 9.1mW/°C above +70°C) 727mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
ESD Protection
HBM (1.5kΩ, 100pF), DO+, DO-, RI+, RI-, DE, $\overline{RE}$, DIN, ROUT .....> ±2kV
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.0V to 3.6V, $|V_{ID}|$ = 0.1V to 2.4V, common-mode input voltage (V_{CM}) = $|V_{ID}/2|$ to 2.4V - $|V_{ID}|/2$, R_L = 100Ω ±1%, T_A = -40°C to +85°C. Typical values are at V_{CC} = 3.3V, $|V_{ID}|$ = 0.2V, V_{CM} = 1.2V, T_A = +25°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SINGLE-ENDED INPUTS (DIN, DE, $\overline{RE}$)						
Input High Voltage	V_{IH}		2.0		V_{CC}	V
Input Low Voltage	V_{IL}		0		0.8	V
Input Current	I_{IN}	$\overline{RE}$, DE, DIN = high or low	-10		+10	µA
Input Diode Clamp Voltage	V_{CL}	I_{CLAMP} = -18mA	-1.5			V
DRIVER OUTPUT (DO+, DO-)						
Differential Output Voltage	V_{OD}	Figure 1	250	310	450	mV
Change in Magnitude of V_{OD} Between Complementary Output States	ΔV_{OD}	Figure 1		0.02	25	mV
Offset Voltage	V_{OS}	Figure 1	1.0	1.29	1.7	V
Change in Magnitude of V_{OS} Between Complementary Output States	ΔV_{OS}	Figure 1		0.8	25	mV
High-Impedance Leakage Current	I_{OZD}	DE = 0; DO+, DO- = V_{CC} or 0	-1		+1	µA
Power-Off Leakage Current	I_{OXD}	DO+, DO- = 3.6V or 0; V_{CC} = 0	-1		+1	µA
Output Short-Circuit Current	I_{OSD}	DO+ = 0 at DIN = V_{CC}		-3	-10	mA
		DO- = 0 at DIN = 0		-3	-10	
Output Capacitance	C_{DO}	Capacitance from DO+ or DO- to 0		3.7		pF
RECEIVER INPUT (RI+, RI-)						
Differential Input High Threshold	V_{TH}				100	mV
Differential Input Low Threshold	V_{TL}		-100			mV
Input Current	I_{IN}	V_{CC} = 3.6V or 0; RI+, RI- = 2.4V or 0	-10		+10	µA
Input Capacitance	C_{RI}	RI+ or RI- to 0		5		pF
RECEIVER OUTPUT (ROUT)						
Output High Voltage	V_{OH}	I_{OH} = -400µA, V_{ID} = 100mV	2.9	3.28		V
		I_{OH} = -400µA, RI+, RI- open	2.9	3.28		V
Output Low Voltage	V_{OL}	I_{OL} = +2.0mA, V_{ID} = -100mV		0.025	0.4	V
Output Short-Circuit Current	I_{OS}	V_{ID} = +100mV, ROUT = 0	-20	-28	-75	mA

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 3.0V to 3.6V, $|V_{ID}|$ = 0.1V to 2.4V, common-mode input voltage (V_{CM}) = $|V_{ID}/2|$ to 2.4V - $|V_{ID}|/2$, R_L = 100Ω ±1%, T_A = -40°C to +85°C. Typical values are at V_{CC} = 3.3V, $|V_{ID}|$ = 0.2V, V_{CM} = 1.2V, T_A = +25°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY CURRENT						
Supply Current	I_{CC}	DE = V_{CC}, $\overline{RE}$ = 0		7.4	12.5	mA
Driver Supply Current	I_{CCD}	DE = $\overline{RE}$ = V_{CC}		7.4	12.5	mA
Receiver Supply Current	I_{CCR}	DE = $\overline{RE}$ = 0		4.4	7.0	mA
Disable Supply Current	I_{CCZ}	DE = 0, $\overline{RE}$ = V_{CC}		4.4	7.0	mA

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.0V to 3.6V, $|V_{ID}|$ = 0.2V, V_{CM} = 1.2V, R_L = 100Ω ±1%, C_L = 10pF, T_A = -40°C to +85°C. Typical values are at V_{CC} = 3.3V, $|V_{ID}|$ = 0.2V, V_{CM} = 1.2V, T_A = +25°C, unless otherwise noted.) (Notes 3, 4, 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DRIVER						
Differential High-to-Low Propagation Delay	t_{PHLD}	Figure 2	2.0	4.4	6.5	ns
Differential Low-to-High Propagation Delay	t_{PLHD}	Figure 2	1.0	4.2	7.0	ns
Differential Skew $\|t_{PHLD} - t_{PLHD}\|$	t_{SKD}	Figure 2		0.2	1.0	ns
Rise Time	t_{TLHD}	Figure 2	0.2	0.9	3.0	ns
Fall Time	t_{THLD}	Figure 2	0.2	0.8	3.0	ns
Disable Time High to Z	t_{PHZ}	Figure 3	1.5	6.0	8.0	ns
Disable Time Low to Z	t_{PLZ}	Figure 3	2.5	5.5	9.0	ns
Enable Time Z to High	t_{PZH}	Figure 3	4.0	5.5	8.0	ns
Enable Time Z to Low	t_{PZL}	Figure 3	3.8	5.0	8.0	ns
RECEIVER						
Differential High-to-Low Propagation Delay	t_{PHL}	Figure 4	3.0	5.4	7.0	ns
Differential Low-to-High Propagation Delay	t_{PLH}	Figure 4	3.0	5.3	9.0	ns
Differential Skew $\|t_{PHL} - t_{PLH}\|$	T_{SK}	Figure 4		0.14	1.5	ns
Rise Time	t_{TLH}	Figure 4	0.15	0.8	3.0	ns
Fall Time	t_{THL}	Figure 4	0.15	0.4	3.0	ns
Disable Time High to Z	t_{PHZ}	Figure 5	3.0	5.4	6.0	ns
Disable Time Low to Z	t_{PLZ}	Figure 5	3.0	5.1	6.0	ns
Enable Time Z to High	t_{PZH}	Figure 5	3.0	5.4	8.0	ns
Enable Time Z to Low	t_{PZL}	Figure 5	3.0	5.1	8.0	ns

Note 1: Maximum and minimum limits over temperature are guaranteed by design and characterization. Devices are 100% tested at T_A = +25°C.

Note 2: Current into a pin is defined as positive. Current out of a pin is defined as negative. All voltages are referenced to device ground except V_{TH}, V_{TL}, V_{ID}, V_{OD}, and ΔV_{OD}.

Note 3: C_L includes probe and jig capacitance.

Note 4: AC parameters are guaranteed by design and characterization.

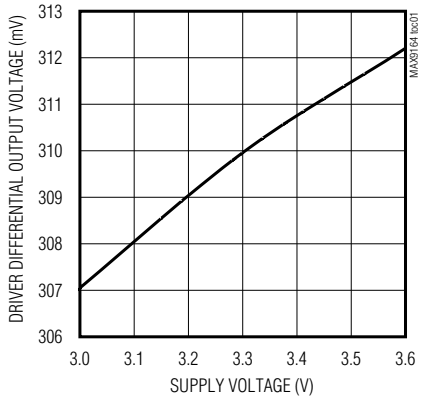
Note 5: Generator waveforms for all tests unless otherwise specified: f = 100MHz, Z_0 = 50Ω, t_R = t_F = 6.0ns (0 to 3V, 0% to 100%) for DE and $\overline{RE}$, t_R = t_F = 3.0ns (0 to 3V, 0% to 100%) for DIN, and t_R = t_F = 1.0ns ($|V_{ID}|$ = 0.2V, 20% to 80%) for RI+/RI- inputs.

3.3V Single LVDS Driver/Receiver

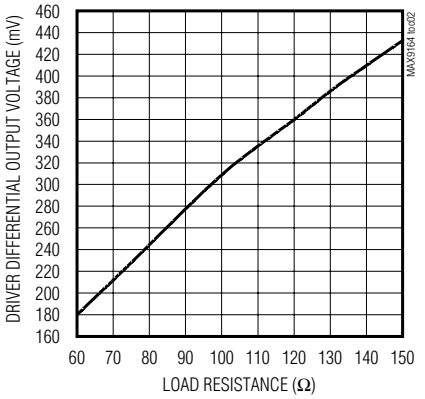
Typical Operating Characteristics

(V_{CC} = 3.3V, $|V_{ID}|$ = 0.2V, V_{CM} = 1.2V, R_L = 100Ω ±1%, FREQ = 100MHz, C_L = 10pF, T_A = +25°C, unless otherwise noted.)

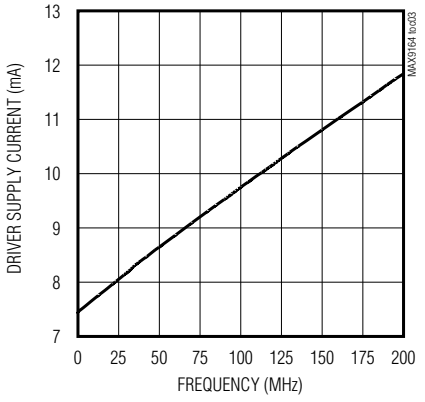
DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



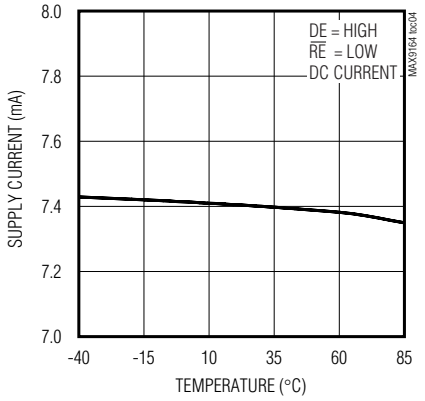
DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs. LOAD RESISTANCE



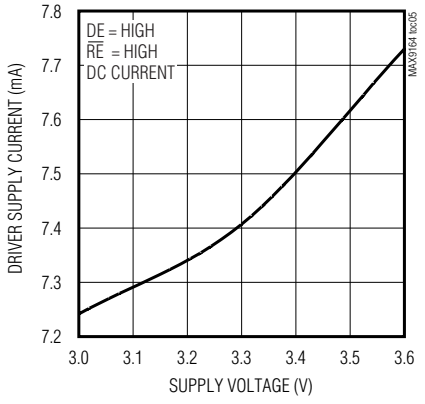
DRIVER SUPPLY CURRENT vs. FREQUENCY



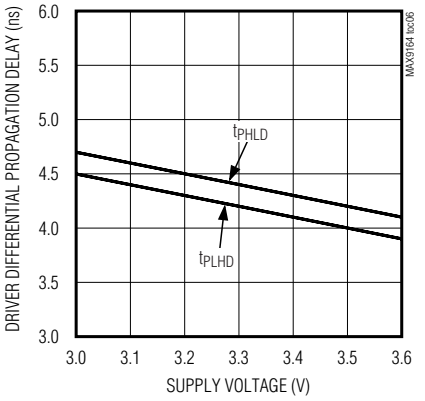
SUPPLY CURRENT (I_{CC}) vs. TEMPERATURE



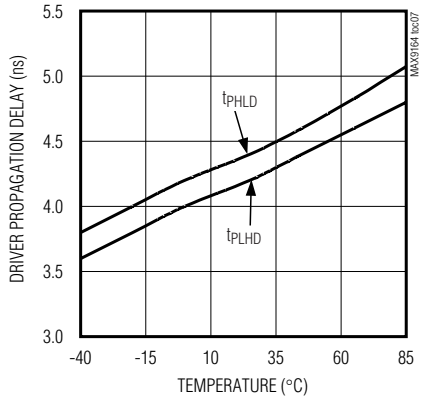
DRIVER SUPPLY CURRENT (I_{CC}) vs. SUPPLY VOLTAGE



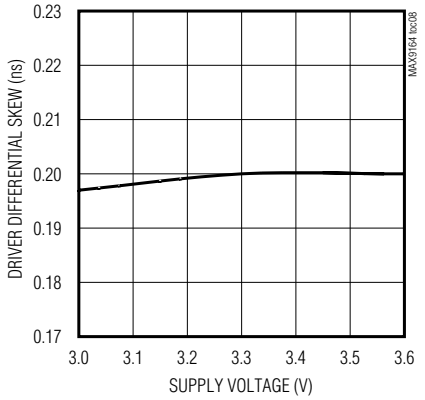
DRIVER DIFFERENTIAL PROPAGATION DELAY vs. SUPPLY VOLTAGE



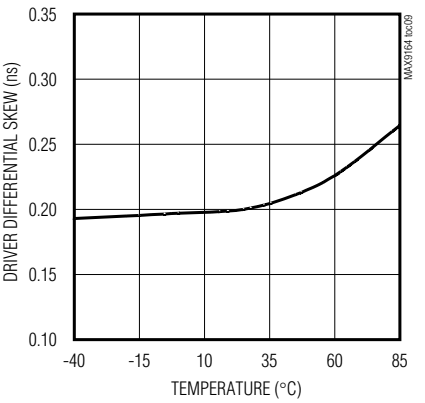
DRIVER DIFFERENTIAL PROPAGATION DELAY vs. TEMPERATURRE



DRIVER DIFFERENTIAL SKEW vs. SUPPLY VOLTAGE



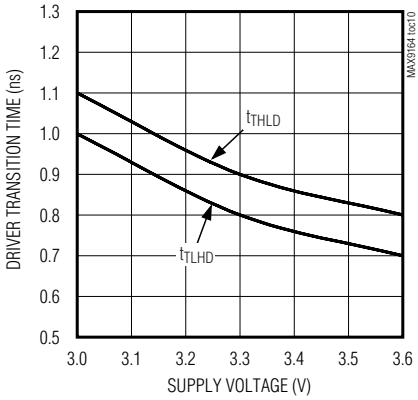
DRIVER DIFFERENTIAL SKEW vs. TEMPERATURE



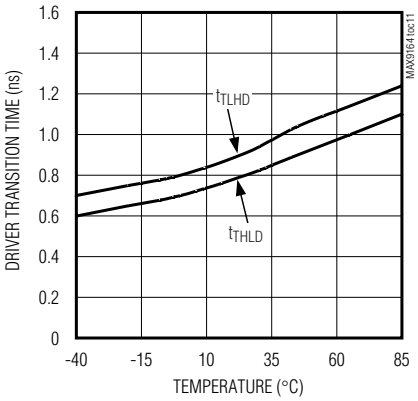
Typical Operating Characteristics (continued)

(V_{CC} = 3.3V, $|V_{ID}|$ = 0.2V, V_{CM} = 1.2V, R_L = 100Ω ±1%, FREQ = 100MHz, C_L = 10pF, T_A = +25°C, unless otherwise noted.)

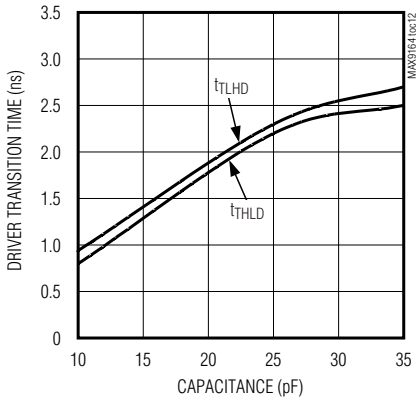
DRIVER TRANSITION TIME vs. SUPPLY VOLTAGE



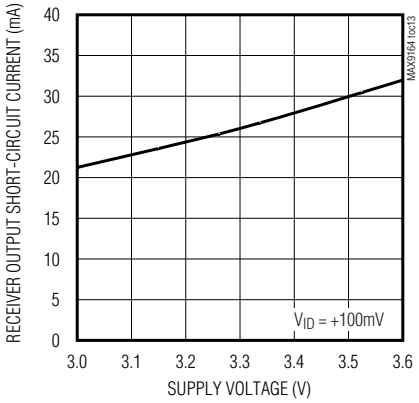
DRIVER TRANSITION TIME vs. TEMPERATURE



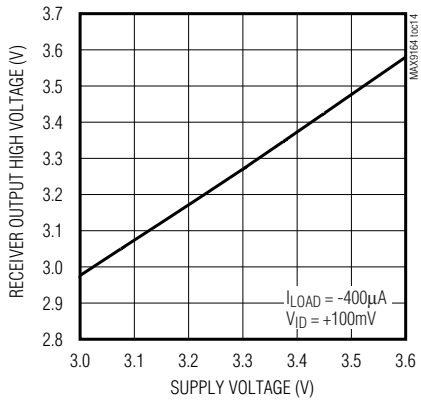
DRIVER TRANSITION TIME vs. TOTAL LOAD CAPACITANCE



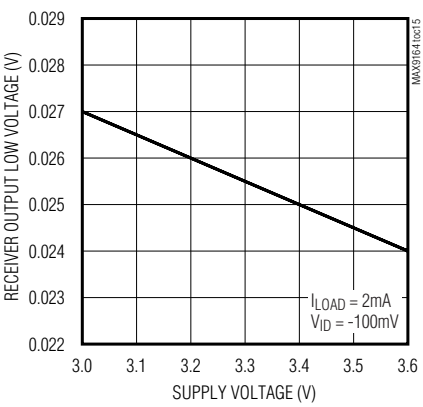
RECEIVER OUTPUT SHORT-CIRCUIT CURRENT vs. SUPPLY VOLTAGE



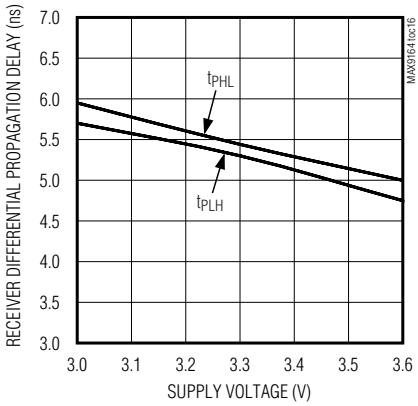
RECEIVER OUTPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE



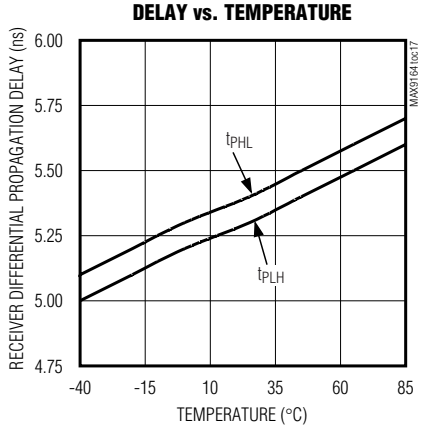
RECEIVER OUTPUT LOW VOLTAGE vs. SUPPLY VOLTAGE



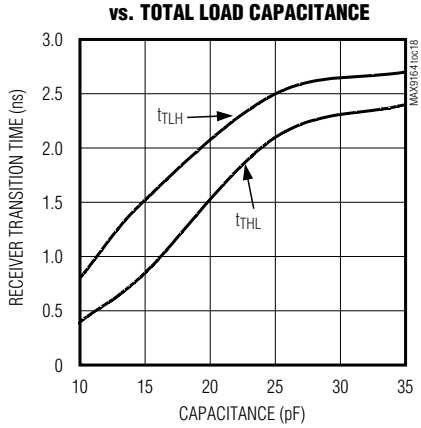
RECEIVER DIFFERENTIAL PROPAGATION DELAY vs. SUPPLY VOLTAGE



RECEIVER DIFFERENTIAL PROPAGATION DELAY vs. TEMPERATURE



RECEIVER TRANSITION TIME vs. TOTAL LOAD CAPACITANCE



3.3V Single LVDS Driver/Receiver

Pin Description

PIN	NAME	FUNCTION
1	DE	LVTTL/LVCMOS Driver Enable Input. The driver is enabled when DE is high. When DE is low, the driver outputs, DO+ and DO-, are disabled and are high impedance.
2	DIN	LVTTL/LVCMOS Driver Input
3, 5, 6, 13	N.C.	No Connection. Not internally connected.
4	ROUT	LVTTL/LVCMOS Receiver Output
7	GND	Ground
8	$\overline{RE}$	LVTTL/LVCMOS Receiver Enable Input. The receiver is enabled when $\overline{RE}$ is low. When $\overline{RE}$ is high, the receiver output is disabled and is high impedance.
9	RI-	Inverting LVDS Receiver Input. RI- has an integrated pulldown to GND.
10	RI+	Noninverting LVDS Receiver Input. RI+ has an integrated pullup to V_{CC}.
11	DO-	Inverting LVDS Driver Output
12	DO+	Noninverting LVDS Driver Output
14	V_{CC}	Power-Supply Input. Bypass V_{CC} to GND with 0.1µF and 0.001µF ceramic capacitors.

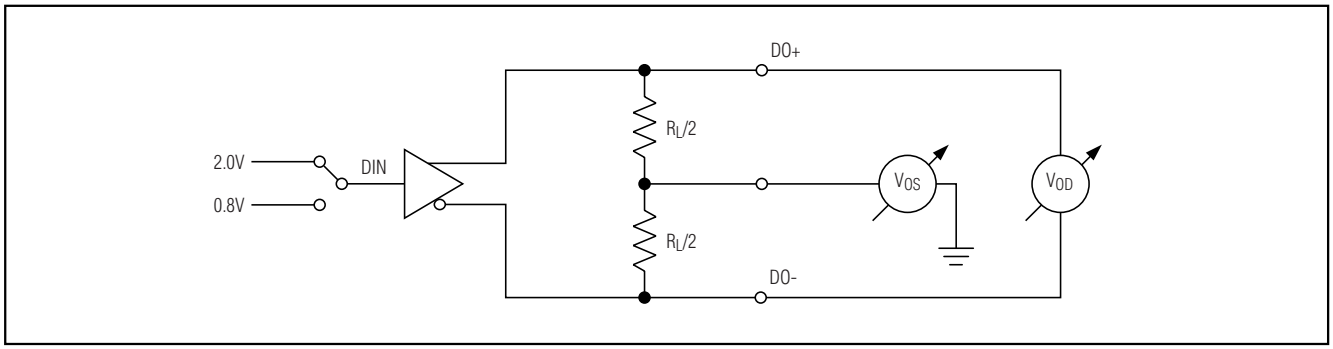


Figure 1. Differential Driver DC Test Circuit

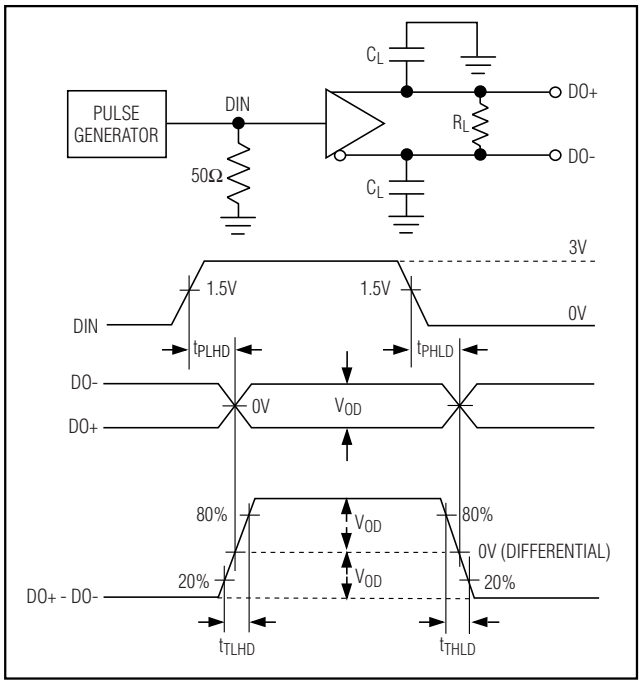


Figure 2. Driver Differential Propagation Delay and Transition Time Test Circuit and Waveforms

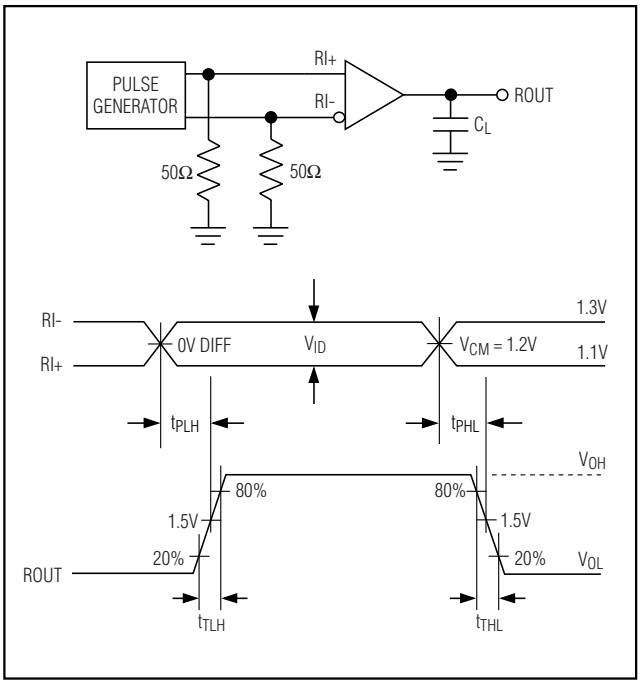


Figure 4. Receiver Propagation Delay and Transition Time Test Circuit and Waveforms

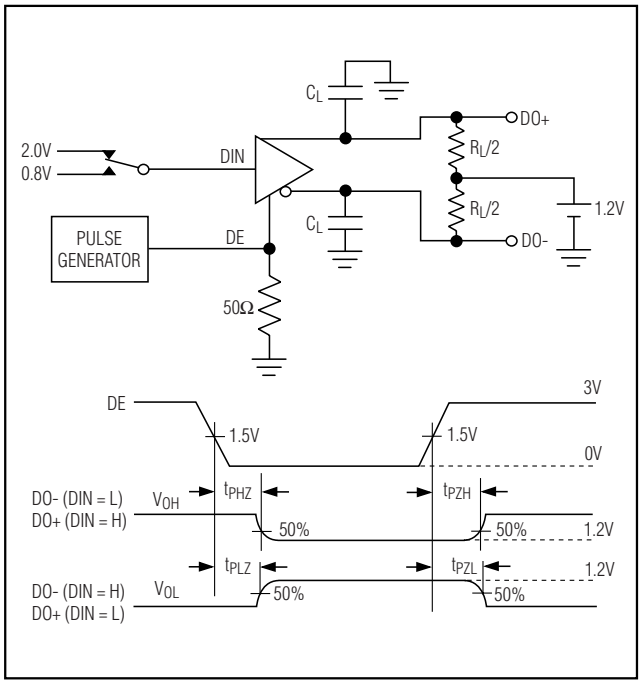


Figure 3. Driver High-Impedance Delay Test Circuit and Waveforms

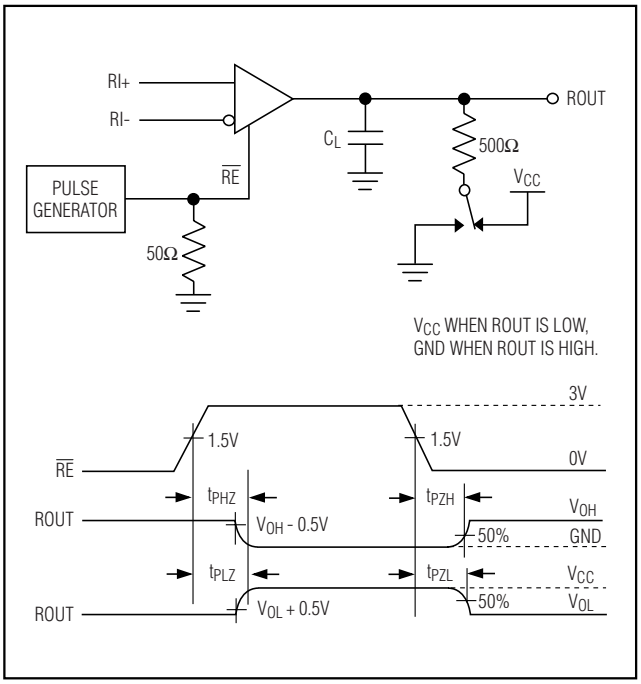


Figure 5. Receiver High-Impedance Delay Test Circuit and Waveforms

3.3V Single LVDS Driver/Receiver

Detailed Description

The MAX9164 high-speed LVDS driver/receiver is designed specifically for low-power point-to-point applications. The MAX9164 operates from a single 3.3V power supply, and is pin compatible with the DS90LV019. The device features an independent differential driver and receiver.

The MAX9164 driver outputs use a current-steering configuration to generate a 3.1mA (typ) output current. This current-steering approach induces less ground bounce and no shoot-through current, enhancing noise margin and system speed performance. The outputs are short-circuit current limited. The MAX9164 output requires a resistive load to terminate the signal and complete the transmission loop. With a typical 3.1mA output current, the MAX9164 produces a 310mV output voltage when driving a bus terminated with a 100Ω resistor (3.1mA x 100Ω = 310mV).

The MAX9164 receiver detects a differential input as low as 100mV and translates it to single-ended output. The device features input biasing that drives the output high if the inputs are left open.

Power-On Reset

The power-on reset voltage of the MAX9164 is typically 2.2V. When the supply falls below this voltage, the device is disabled and the outputs (DO+, DO-, and ROUT) are high impedance.

Applications Information

Power-Supply Bypassing

Bypass V_{CC} with high-frequency, surface-mount ceramic 0.1µF and 0.001µF capacitors in parallel as close to the device as possible, with the smaller valued capacitor closest to V_{CC}.

Termination

The MAX9164 requires an external termination resistor at the differential input. This termination resistor should match the differential impedance of the input transmission line.

The differential output requires a termination resistor at the far end of the transmission line. This termination resistor should match the differential impedance of the output transmission line.

These termination resistors are typically 100Ω. Minimize the distance between the input termination resistor and the MAX9164 receiver input.

Traces, Cables, and Connectors

The characteristics of differential input and output connections affect the performance of the device. Use controlled-impedance traces, cables, and connectors with matched characteristic impedance.

Ensure that noise couples as common mode by running the traces of a differential pair close together. Reduce within-pair skew by matching the electrical length of the conductors within a differential pair. Excessive skew can result in a degradation of magnetic field cancellation.

Maintain the distance between conductors within a differential pair to avoid discontinuities in differential impedance. Minimize the number of vias to further prevent impedance discontinuities.

Board Layout

For LVDS applications, a four-layer PC board with separate power, ground, LVDS, and logic signal layers is recommended. Separate the LVTTL/LVCMOS and LVDS signals to prevent coupling.

Chip Information

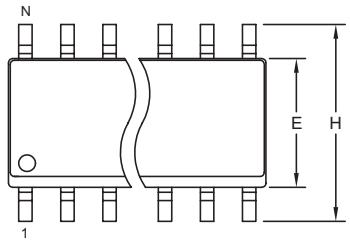
TRANSISTOR COUNT: 901

PROCESS: CMOS

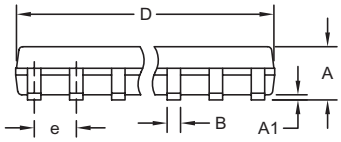
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

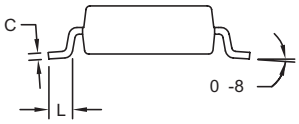
SOICN .EPS



TOP VIEW



FRONT VIEW



SIDE VIEW

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050 BSC		1.27 BSC	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27

VARIATIONS:

	INCHES		MILLIMETERS			
DIM	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	AA
D	0.337	0.344	8.55	8.75	14	AB
D	0.386	0.394	9.80	10.00	16	AC

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.
5. MEETS JEDEC MS012.
6. N = NUMBER OF PINS.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, .150" SOIC

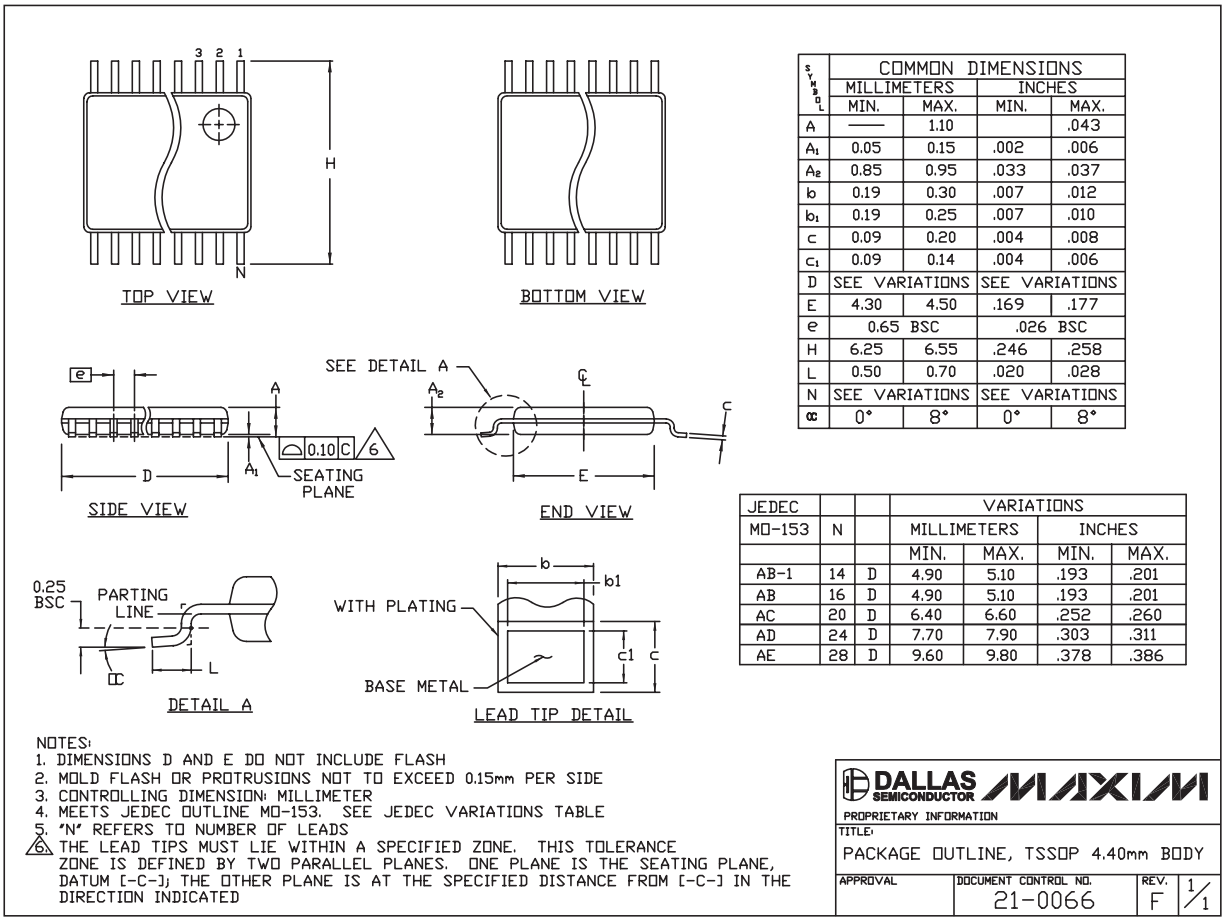
APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0041	B	1/1

3.3V Single LVDS Driver/Receiver

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

TSSOP4.40mm.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	——	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b_1	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c_1	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB-1	14	D	4.90	5.10	.193	.201
AB	16	D	4.90	5.10	.193	.201
AC	20	D	6.40	6.60	.252	.260
AD	24	D	7.70	7.90	.303	.311
AE	28	D	9.60	9.80	.378	.386

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
5. "N" REFERS TO NUMBER OF LEADS
6. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, TSSOP 4.40mm BODY

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0066	F	1/1