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Advance Information

256K/512K Pipelined BurstRAM™ Secondary Cache Module for Pentium™

The MCM64PD32 (256K) and MCM64PD64 (512K) are designed to provide a burstable, high performance, L2 cache for the Pentium microprocessor in conjunction with Intel's Triton II chip set. The MCM64PD32 is configured as 32K x 64 bits and the MCM64PD64 is configured as 64K x 64 bits. Both are packaged in a 160 pin card edge memory module. Each module uses Motorola's 3.3 V 32K x 32 BurstRAMs and two Motorola 3.3 V 32K x 8 FSRAM for the tag RAM.

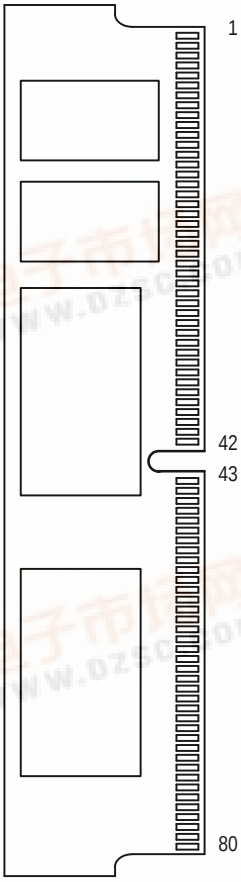
Bursts can be initiated with either address status processor (ADSP) or cache address status (CADS). Subsequent burst addresses are generated internal to the BurstRAM by the cache burst advance (CADV) input pin.

Write cycles are internally self timed and are initiated by the rising edge of the clock (CLK0) input. Eight write enables are provided for byte write control.

PD0 – PD3 map into the Triton II chip set for auto–configuration of the cache control.

- Pentium–Style Burst Counter on Chip
- Pipelined Data Out
- 160 Pin Card Edge Module
- Address Pipeline Supported by $\overline{\text{ADSP}}$ Disabled with $\overline{\text{Ex}}$
- All Cache Data and Tag I/Os are TTL Compatible
- Three State Outputs
- Byte Write Capability
- Fast Module Clock Rate: 66 MHz
- Fast SRAM Access Times: 15 ns for Tag RAM
  8 ns for Data RAMs
- One–cycle Deselect Data RAMs
- Decoupling Capacitors for Each Fast Static RAM
- High Quality Multi–Layer FR4 PWB with Separate Power and Ground Planes
- Single 3.3 V +10%, – 5% Power Supply
- Burndy Connector, Part Number: CELP2X80SC3Z48
- Intel COAST 3.0 Option III Compliant
- Burst Order Select (BOSEL) Option

160–LEAD CARD EDGE
CASE TBD, TOP VIEW



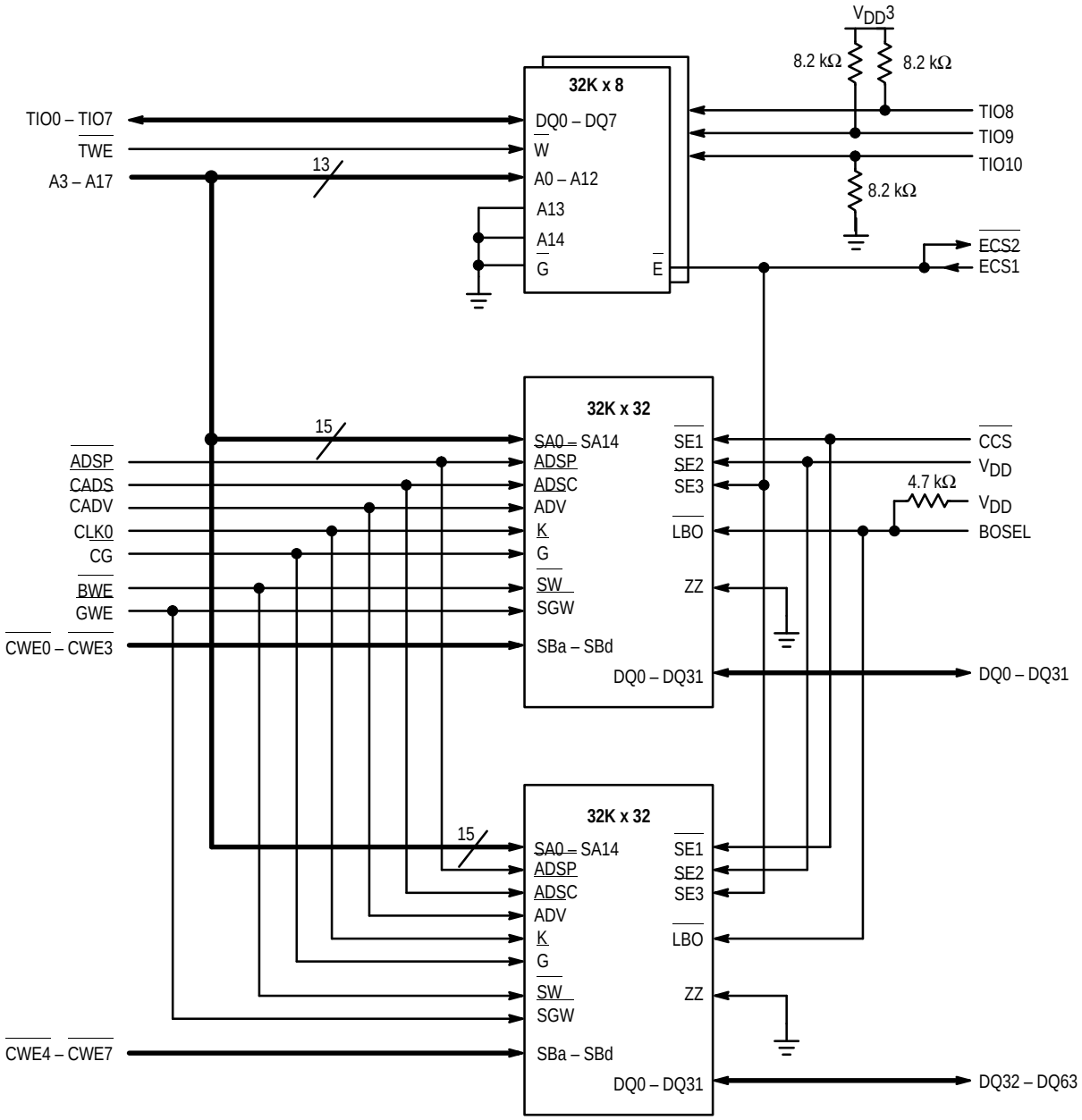
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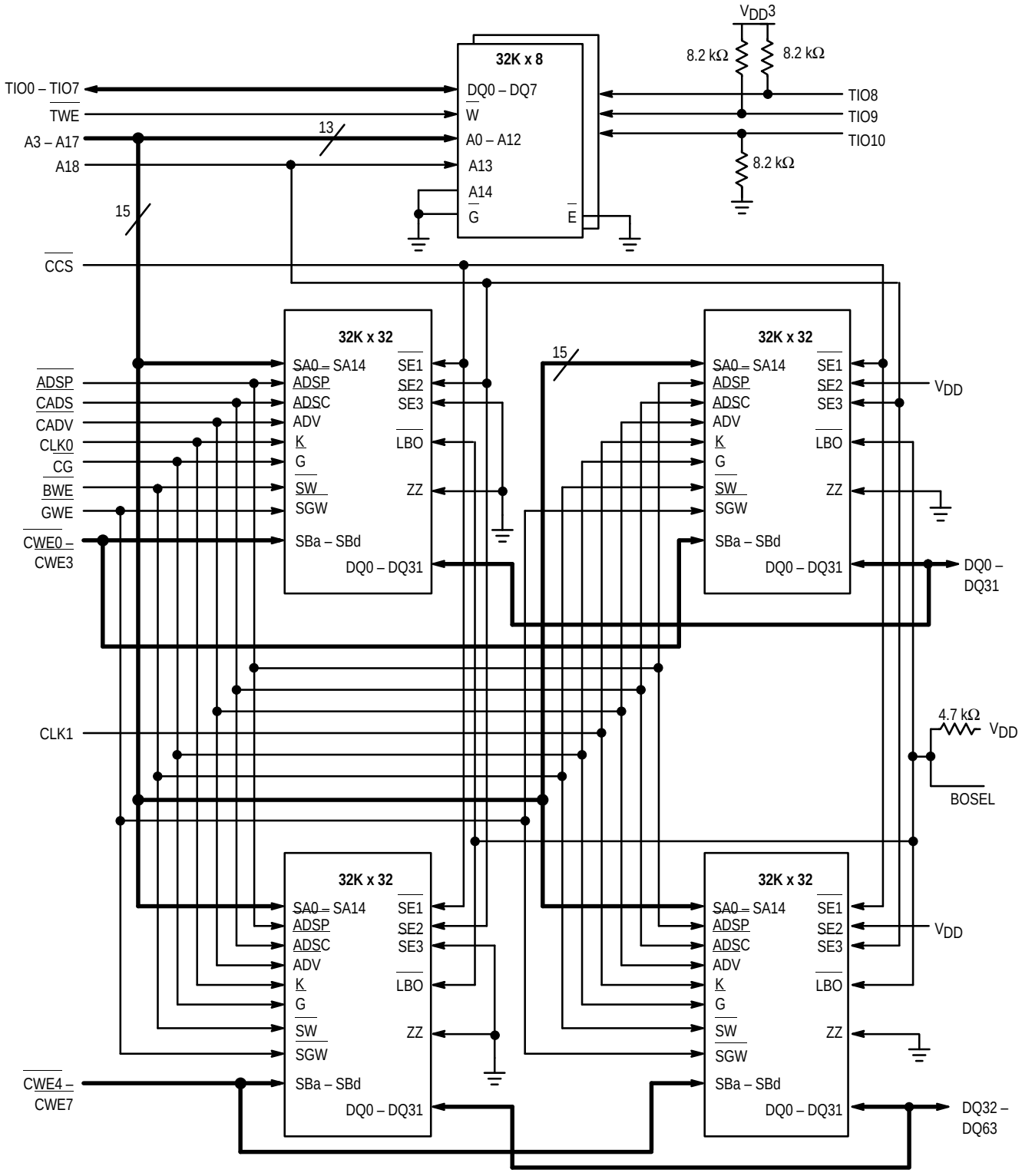
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MCM64PD32 BLOCK DIAGRAM



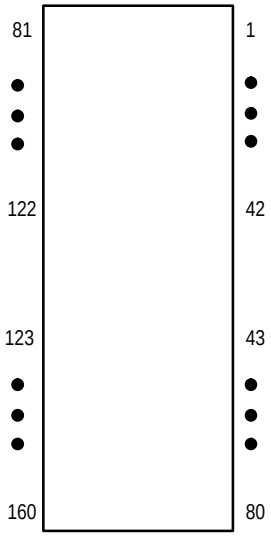
MCM64PD64 BLOCK DIAGRAM



PIN ASSIGNMENT 160–LEAD CARD EDGE MODULE (DIMM)

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{SS}	33	PD1	65	DQ22	97	NC	129	DQ47
2	TIO0	34	PD3	66	DQ20	98	NC	130	DQ45
3	TIO2	35	V_{SS}	67	DQ18	99	V_{SS}	131	DQ43
4	TIO6	36	CLK1	68	$V_{DD}3$	100	RSVD	132	$V_{DD}5$
5	TIO4	37	V_{SS}	69	DQ16	101	A4	133	DQ41
6	TIO8	38	DQ62	70	DQ14	102	A6	134	DQ39
7	$V_{DD}3$	39	$V_{DD}3$	71	DQ12	103	A8	135	DQ37
8	TWE	40	DQ60	72	V_{SS}	104	A10	136	V_{SS}
9	CADS	41	DQ58	73	DQ10	105	$V_{DD}5$	137	DQ35
10	V_{SS}	42	DQ56	74	DQ8	106	A17	138	DQ33
11	CWE4	43	V_{SS}	75	DQ6	107	V_{SS}	139	DQ31
12	CWE6	44	DQ54	76	$V_{DD}3$	108	A9	140	$V_{DD}5$
13	CWE0	45	DQ52	77	DQ4	109	A14	141	DQ29
14	CWE2	46	DQ50	78	DQ2	110	A15	142	DQ27
15	$V_{DD}3$	47	DQ48	79	DQ0	111	RSVD	143	DQ25
16	CCS	48	V_{SS}	80	V_{SS}	112	PD0	144	V_{SS}
17	GWE	49	DQ46	81	V_{SS}	113	PD2	145	DQ23
18	BWE	50	DQ44	82	TIO1	114	BOSEL	146	DQ21
19	V_{SS}	51	DQ42	83	TIO7	115	V_{SS}	147	DQ19
20	A3	52	$V_{DD}3$	84	TIO5	116	CLK0	148	$V_{DD}5$
21	A7	53	DQ40	85	TIO3	117	V_{SS}	149	DQ17
22	A5	54	DQ38	86	TIO9	118	DQ63	150	DQ15
23	A11	55	DQ36	87	$V_{DD}5$	119	$V_{DD}5$	151	DQ13
24	A16	56	V_{SS}	88	TIO10	120	DQ61	152	V_{SS}
25	$V_{DD}3$	57	DQ34	89	CADV	121	DQ59	153	DQ11
26	A18	58	DQ32	90	V_{SS}	122	DQ57	154	DQ9
27	V_{SS}	59	DQ30	91	CG	123	V_{SS}	155	DQ7
28	A12	60	$V_{DD}3$	92	CWE5	124	DQ55	156	$V_{DD}5$
29	A13	61	DQ28	93	CWE7	125	DQ53	157	DQ5
30	ADSP	62	DQ26	94	CWE1	126	DQ51	158	DQ3
31	ECS1	63	DQ24	95	$V_{DD}5$	127	DQ49	159	DQ1
32	ECS2	64	V_{SS}	96	CWE3	128	V_{SS}	160	V_{SS}

TOP VIEW – CASE TBD



PRESENCE DETECT TABLE

Cache Size and Functionality	PD0	PD1	PD2	PD3
256K Pipe Burst	NC	NC	V_{SS}	NC
512K Pipe Burst	V_{SS}	V_{SS}	NC	V_{SS}

PIN DESCRIPTIONS

160–Lead Card Edge Pin Locations	Symbol	Type	Description
20, 21, 22, 23, 24, 26, 28, 29, 101, 102, 103, 104, 106, 108, 109, 110	A3 – A18	Input	Address Inputs: These inputs are registered into data RAMs and must meet setup and hold times. The tag RAM addresses are not registered.
30	$\overline{\text{ADSP}}$	Input	Address Status Processor: Initiates READ, WRITE, or chip deselect cycle (Exception–chip deselect dGs not occur when ADSP is asserted and CCS is high.
114	BOSEL	Input	Burst Order Select: NC for interleaved burst counter. Tie to ground for linear burst counter.
18	BWE	Input	Byte Write Enable: To be used in future modules.
9	CADS	Input	Cache Address Status: Initiates READ, WRITE, or chip deselect cycle.
89	CADV	Input	Cache Burst Advance: Increments address count in accordance with interleaved count style.
16	CCS	Input	Chip Select: Active low chip enable for data RAMs.
91	CG	Input	Cache Output Enable: Active low asynchronous input. Low – enables output buffers (DQ pins) High – DQx pins are high impedance.
36, 116	CLK0, CLK1	Input	Clock: This signal registers the address, data in, and all control signals except CG.
11, 12, 13, 14, 92, 93, 94, 96	$\overline{\text{CWE0}}$ – $\overline{\text{CWE7}}$	Input	Cache Data Byte Write Enable: Active low write signal for data RAMs.
38, 40, 41, 42, 44, 45, 46, 47, 49, 50, 51, 53, 54, 55, 57, 58, 59, 61, 62, 63, 65, 66, 67, 69, 70, 71, 73, 74, 75, 77, 78, 79, 118, 120, 121, 122, 124, 125, 126, 127, 129, 130, 131, 133, 134, 135, 137, 138, 139, 141, 142, 143, 145, 146, 147, 149, 150, 151, 153, 154, 155, 157, 158, 159	DQ0 – DQ63	I/O	Synchronous Data I/O: Drives data out of data RAMs during READ cycles. Stores data to data RAMs during WRITE cycles.
31, 32	$\overline{\text{ECS1}}$, $\overline{\text{ECS2}}$	Input	Expansion Chip Select
17	GWE	Input	Global Write Enable: To be used in future modules.
33, 34, 112, 113	PD0 – PD3	—	Presence Detect: See Presence Detect Table
2, 3, 4, 5, 6, 82, 83, 84, 85, 86, 88	TIO0 – TIO10	I/O	Tag RAM I/O: Drives data out during tag compare cycles. Stores data to tag RAM during tag WRITE cycles.
8	TWE	Input	Tag Write Enable: Active low write signal for tag RAMs.
7, 15, 25, 39, 52, 60, 68, 76	$V_{DD}3$	Supply	Power Supply: 3.3 V + 10%, – 5%.
87, 95, 105, 119, 132, 140, 148, 156	$V_{DD}5$	Supply	Power Supply: 5.0 V $\pm$ 5%.
1, 10, 19, 27, 35, 37, 43, 48, 56, 64, 72, 80, 81, 90, 99, 107, 115, 117, 123, 128, 136, 144, 152, 160	V_{SS}	Supply	Ground.
100, 111	RSVD	—	No Connection: Reserved for future use.
97, 98	NC	—	No Connection: There is no connection to the module.

SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, and 3)

CCS	ADSP	CADS	CADV	CWEx	CLK0	Address Used	Operation
H	X	L	X	X	L–H	N/A	Deselected
L	L	X	X	X	L–H	External Address	Read Cycle, Begin Burst
L	H	L	X	L	L–H	External Address	Write Cycle, Begin Burst
L	H	L	X	H	L–H	External Address	Read Cycle, Begin Burst
X	H	H	L	L	L–H	Next Address	Write Cycle, Continue Burst
X	H	H	L	H	L–H	Next Address	Read Cycle, Continue Burst
X	H	H	H	L	L–H	Current Address	Write Cycle, Suspend Burst
X	H	H	H	H	L–H	Current Address	Read Cycle, Suspend Burst
H	X	H	L	L	L–H	Next Address	Write Cycle, Continue Burst
H	X	H	L	H	L–H	Next Address	Read Cycle, Continue Burst
H	X	H	H	L	L–H	Current Address	Write Cycle, Suspend Burst
H	X	H	H	H	L–H	Current Address	Read Cycle, Suspend Burst

NOTES:
1. X means Don't Care.
2. All inputs except CG must meet setup and hold times for the low–to–high transition of clock (CLK0/1).
3. Wait states are inserted by suspending burst.

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

Operation	$\overline{CG}$	I/O Status
Read	L	Data Out
Read	H	High–Z
Write	X	High–Z — Data In
Deselected	X	High–Z

NOTES:
1. X means Don't Care.
2. For a write operation following a read operation, $\overline{G}$ must be high before the input data required setup time and held high through the input data hold time.

DC ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	$V_{DD}3$	– 0.5 to + 4.6	V
Voltage Relative to V_{SS}	V_{in}, V_{out}	V_{SS} – 0.5 to $V_{DD}3$ + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	– 65 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V + 10%, – 5%, T_J = 20 to + 110°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage (Operating Voltage Range)	V_{DD}	3.135	3.6	V	1
Input High Voltage	V_{IH}	2.0	V_{DD} + 0.3	V	2
Input Low Voltage	V_{IL}	– 0.5	0.8	V	3

NOTES:
1. JEDEC specification 8–1A specifies ± 0.3 V tolerance for V_{DD}.
2. V_{IH} (max) = V_{DD} + 0.3 V dc; V_{IH} (max) = V_{DD} + 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.
3. V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Notes
Input Leakage Current (All Inputs, V_{in} = 0 to V_{DD}3)	$I_{lkg(I)}$	—	± 1.0	μA	
Output Leakage Current (CG = V_{IH})	$I_{lkg(O)}$	—	± 1.0	μA	
TTL Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V	1
TTL Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V	1

NOTES:
1. Champing diodes exist to V_{SS} and V_{DD}.

POWER SUPPLY CURRENTS

Parameter		Symbol	Max	Unit
AC Supply Current (CG = V_{IH}, $\overline{CCS}$ = V_{IL}, I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	MCM64PD32 MCM64PD64	I_{DDA}	720 880	mA
AC Standby Current (CG = V_{IH}, $\overline{CCS}$ = V_{IL}, I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	MCM64PD32 MCM64PD64	I_{SB1}	200 490	mA

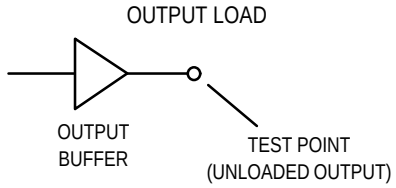
CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_J = 20 to 110°C, Periodically Sampled Rather Than 100% Tested)

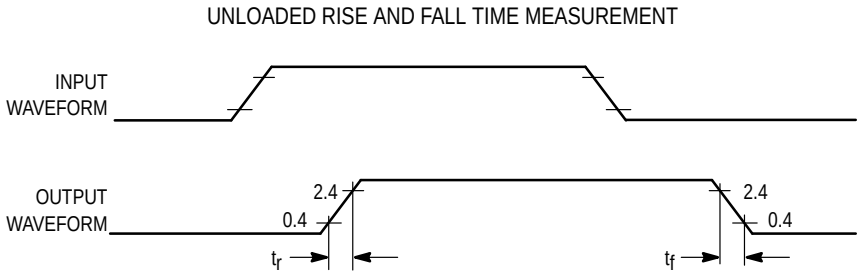
Parameter		Symbol	Max	Unit
Input Capacitance	MCM64PD32 MCM64PD64	C_{in}	22 32	pF
Input/Output Capacitance (DQ0 – DQ63)	MCM64PD32 MCM64PD64	$C_{I/O}$	8 16	pF

DATA RAMs AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V + 10%, – 5% T_J = 20 to + 110°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V	Output Timing Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V	Output Load . . . . . See Figure 3 Unless Otherwise Noted
Input Rise/Fall Time . . . . . 2 ns	





NOTES:
1. Input waveform has a slew rate of 1 V/ns.
2. Rise time is measured from 0.4 V to 2.4 V unloaded.
3. Fall time is measured from 2.4 V to 0.4 V unloaded.

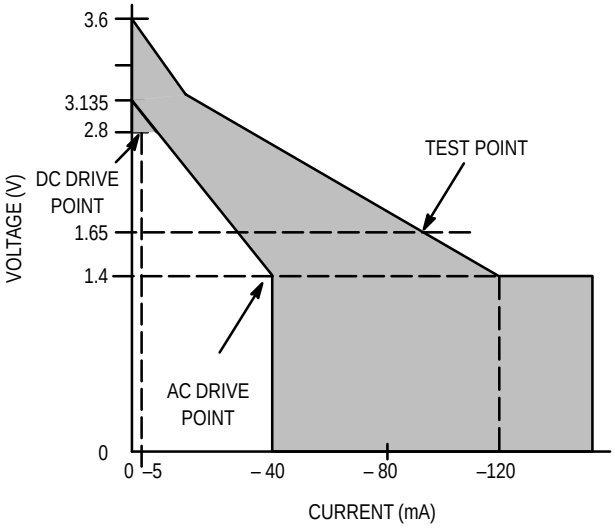
Figure 1. Unloaded Rise and Fall Time Characterization

DATA RAMs READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	MCM64PD32–66		Unit	Notes
		Min	Max		
Cycle Time	t_{KHKH}	15	—	ns	
Clock Access Time	t_{KHQV}	—	8	ns	5
Output Enable to Output Valid	t_{GLQV}	—	6	ns	5
Clock High to Output Active	t_{KHQX1}	0	—	ns	5, 7
Clock High to Output Change	t_{KHQX2}	2	—	ns	5, 7
Output Enable to Output Active	t_{GLQX}	0	—	ns	5, 7
Output Disable to Q High–Z	t_{GHQZ}	—	8	ns	6, 7
Clock High to Q High–Z	t_{KHQZ}	2	8	ns	6, 7
Clock High Pulse Width	t_{KHKL}	5	—	ns	
Clock Low Pulse Width	t_{KLKH}	5	—	ns	
Setup Times: Address Address Status Data In Write Address Advance Chip Enable	t_{AVKH} t_{ADSVKH} t_{DVKH} t_{WVKH} t_{ADVVKH} t_{EVKH}	2.5	—	ns	4
Hold Times: Address Address Status Data In Write Address Advance Chip Enable	t_{KHAX} t_{KHADSX} t_{KHDX} t_{KHWX} t_{KHADVX} t_{KHEX}	0.5	—	ns	4

NOTES:
1. Write applies to all SBx, SW, and SGW signals when the chip is selected and ADSP high.
2. Chip Enable applies to all SE1, SE2 and SE3 signals whenever ADSP or ADSC is asserted.
3. All read and write cycle timings are referenced from K or G.
4. G is a don't care after write cycle begins. To prevent bus contention, G should be negated prior to start of write cycle.
5. Tested per AC Test Load.
6. Measured at ± 200 mV from steady state. Tested per High–Z Test Load.
7. This parameter is sampled and is not 100% tested.

PULL–UP		
VOLTAGE (V)	I (mA) Min	I (mA) Max
– 0.5	– 40	– 120
0	– 40	– 120
1.4	– 40	– 120
1.65	– 37	– 104
2	–28	– 81
3.135	0	– 20
3.6	0	0

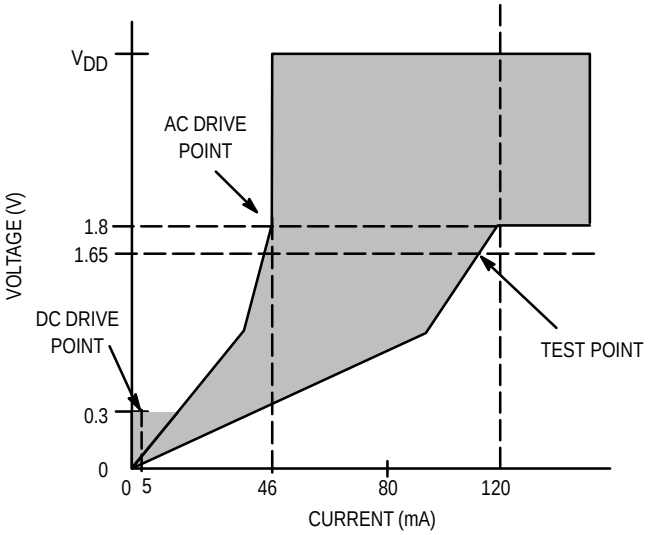


NOTES:

1. Driver impedance @ 1.65 V = 15.9 to 44.6 Ω.
2. Meets the temperature and voltage range specified in DC Characteristics tables.
3. This drawing is not to scale. Comparisons should be made to the table in Figure 2a.

(a) Pull–Up

PULL–DOWN		
VOLTAGE (V)	I (mA) Min	I (mA) Max
– 0.5	– 34	– 126
0	0	0
0.5	17	47
1	35	90
1.65	45	114
1.8	46	120
3.6	46	120
4	46	120



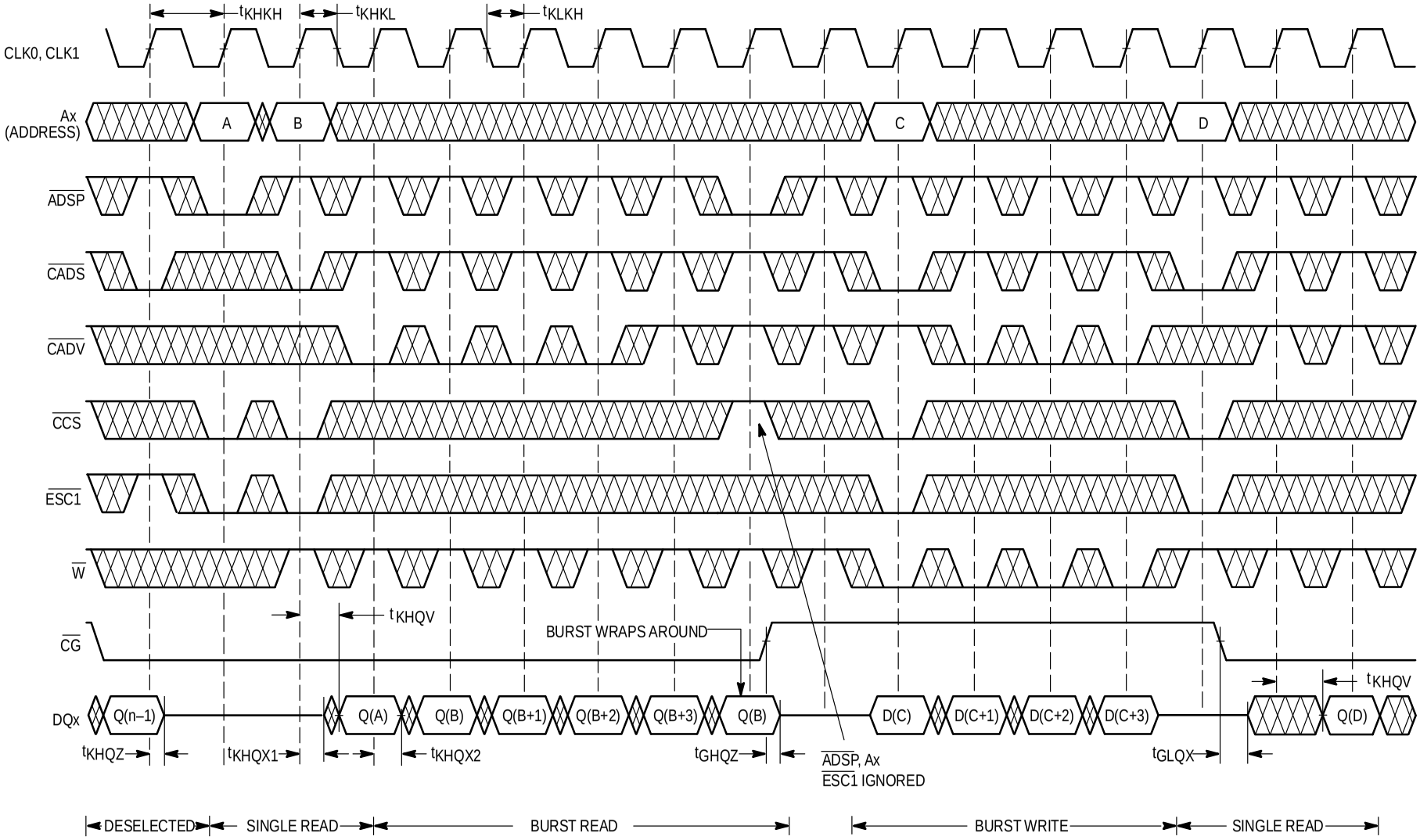
NOTES:

1. Driver impedance @ 1.65 V = 15.9 to 44.6 Ω.
2. Meets the temperature and voltage range specified in DC Characteristics tables.
3. This drawing is not to scale. Comparisons should be made to the table in Figure 2b.

(b) Pull–Down

Figure 2. Output Buffer Characteristics

DATA RAMs READ/WRITE CYCLES



Note: $\overline{W}$ low = $\overline{GWE}$ low and/or $\overline{BWE}$ and $\overline{CWEx}$ low.

TAG RAM AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V ± 0.3 V, T_J = 20 to + 110°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 3 ns

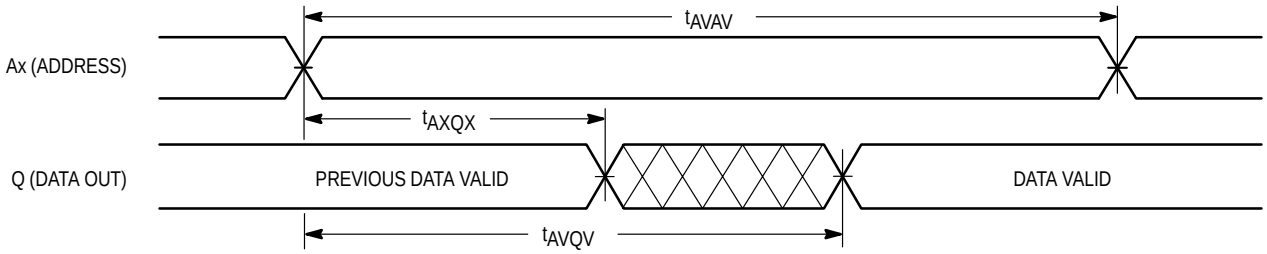
Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load . . . . . Figure 3a Unless Otherwise Noted

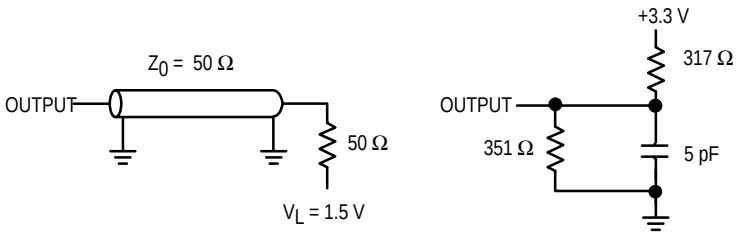
TAG RAM READ CYCLE (See Note 1 and 5)

Parameter	Symbol	– 15		Unit	Notes
		Min	Max		
Read Cycle Time	t_{AVAV}	15	—	ns	2
Address Access Time	t_{AVQV}	—	15	ns	
Output Hold from Address Change	t_{AXQX}	4	—	ns	3, 4

NOTES:
1. CWE is high for read cycle.
2. All timings are referenced from the last valid address to the first address transition.
3. Transition is measured ±500 mV from steady–state voltage with load of Figure 3b.
4. This parameter is sampled and not 100% tested.
5. Device is continuously selected (CG = V_{IL}).

TAG RAM READ CYCLE (See Note 5)





(a) (b)

Figure 3. AC Test Loads

TIMING LIMITS

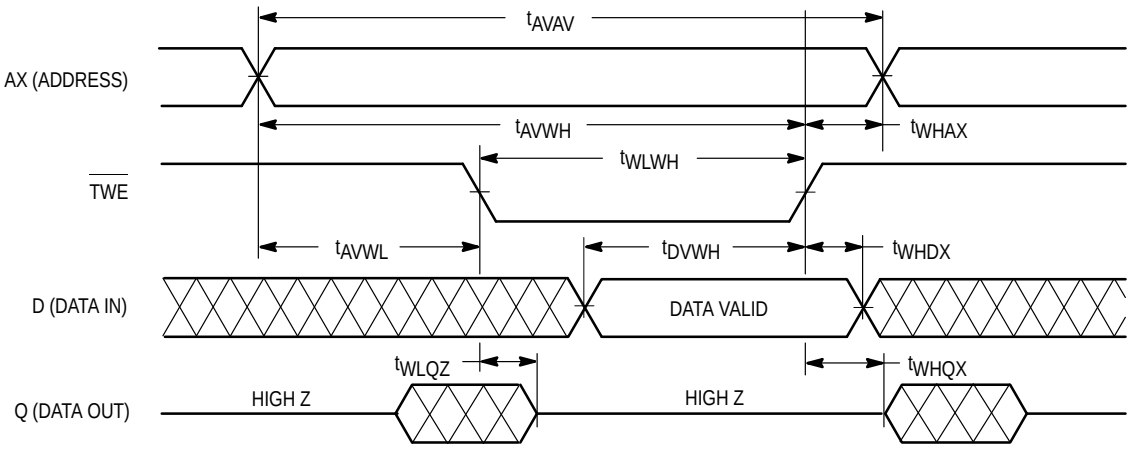
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

TAG RAM WRITE CYCLE (See Notes 1 and 2)

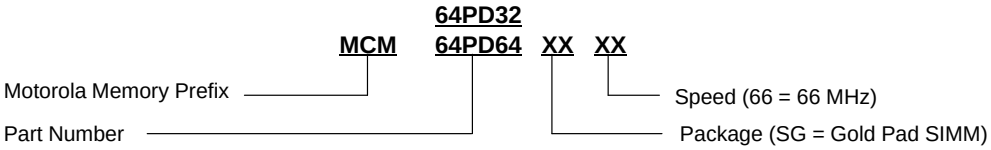
Parameter	Symbol	– 15		Unit	Notes
		Min	Max		
Write Cycle Time	t_{AVAV}	15	—	ns	3
Address Setup Time	t_{AVWL}	0	—	ns	
Address Valid to End of Write	t_{AVWH}	12	—	ns	
Data Valid to End of Write	t_{DVWH}	7	—	ns	
Data Hold Time	t_{WHDX}	0	—	ns	
Write Low to Output High–Z	t_{WLQZ}	0	7	ns	5,6,7
Write High to Output Active	t_{WHQX}	4	—	ns	5,6,7
Write Recovery Time	t_{WHAX}	0	—	ns	

NOTES:
1. A write occurs when $\overline{CWE}$ is low.
2. If CG goes low coincident with or after $\overline{CWE}$ goes low, the output will remain in a high impedance state.
3. All timings are referenced from the last valid address to the first address transition.
4. If CG ≥ V_{IH}, the output will remain in a high impedance state.
5. At any given voltage and temperature, t_{WLQZ} (max) is less than t_{WHQX} (min), both for a given device and from device to device.
6. Transition is measured ±500 mV from steady–state voltage with load of Figure 3B.
7. This parameter is sampled and not 100% tested.

TAG RAM WRITE CYCLE (See Notes 1 and 2)



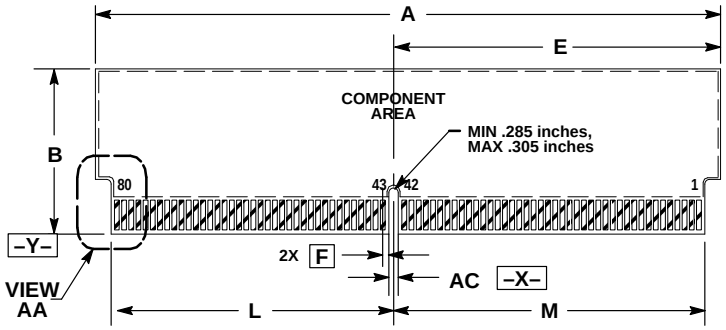
ORDERING INFORMATION
(Order by Full Part Number)



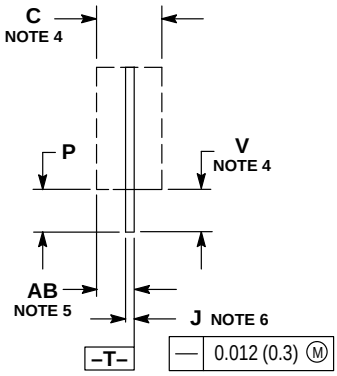
Full Part Number — MCM64PD32SG66 MCM64PD64SG66

PACKAGE DIMENSIONS

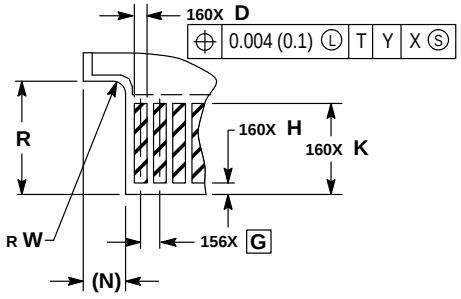
160–LEAD
CARD EDGE MODULE
CASE TBD



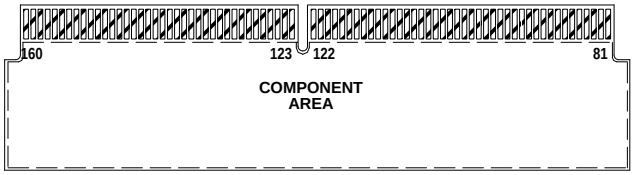
FRONT VIEW



SIDE VIEW



VIEW AA



BACK VIEW

NOTE: Case Outline number to be determined.

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CARD THICKNESS APPLIES ACROSS TABS AND INCLUDES PLATING AND/OR METALLIZATION.
4. DIMENSIONS C AND V DEFINE A DOUBLE–SIDED MODULE.
5. DIMENSION AB DEFINES OPTIONAL SINGLE–SIDED MODULE.
6. STRAIGHTNESS CALLOUT APPLIES TO TAB AREA ONLY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	4.330	4.350	109.98	110.49
B	1.120	1.140	28.45	28.96
C	—	0.454	—	11.53
D	0.033	0.037	0.84	0.94
E	2.265	2.275	57.53	57.79
F	0.075 BSC		1.91 BSC	
G	0.050 BSC		1.27 BSC	
H	—	0.030	—	0.51
J	0.055	0.069	1.40	1.75
K	0.210	—	5.33	—
L	1.955	1.965	49.66	49.91
M	2.155	2.165	54.74	54.99
N	0.110 REF		2.79 REF	
P	0.300	—	7.62	—
R	0.492	0.512	7.24	7.75
V	0.300	—	7.62	—
W	0.040	0.060	1.02	1.52
AB	—	0.262	—	6.66
AC	0.072	0.076	1.83	1.93

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How to reach us:

USA / EUROPE / Locations Not Listed: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036. 1–800–441–2447 or 602–303–5454

MFAX: RMFAX0@email.sps.mot.com – TOUCHTONE 602–244–6609

INTERNET: http://Design–NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, 6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–81–3521–8315

ASIA / PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298