

Am27S191/S191A/S191SA/PS191/PS191A

Am27S291/S291A/S291SA/PS291/PS291A

16,384-Bit (2048x8) Bipolar PROM



DISTINCTIVE CHARACTERISTICS

- Fast access time allows high system speed
- 50% power savings on deselected parts — enhances reliability through total system heat reduction (27PS devices)
- Plug in replacement for industry standard product — no board changes required
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ > 98%)
- Voltage and temperature compensated providing extremely flat AC performance over military range
- Rapid recovery from power-down state provides minimum delay (27PS devices)

GENERAL DESCRIPTION

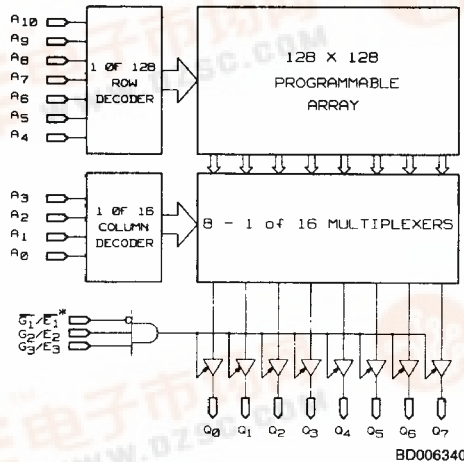
The Am27S191 (2048 words by 8 bits) is a Schottky TTL Programmable Read-Only Memory (PROM).

This device has three-state outputs which are compatible with low-power Schottky bus standards capable of satisfying the requirements of a variety of microprogrammable controls, mapping functions, code conversion, or logic

replacement. Easy word-depth expansion is facilitated by both active LOW (\bar{G}_1) and active HIGH (G_2 and G_3) output enables.

This device is also available in 300-mil, lateral center DIP (Am27S291). Additionally, this device is offered in a power-switched, three-state version (Am27PS191/Am27PS291).

BLOCK DIAGRAM



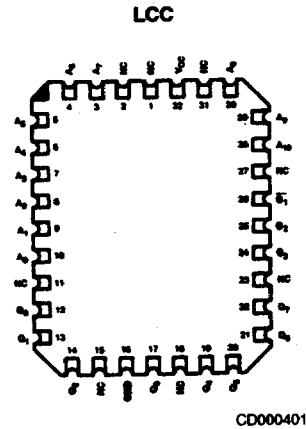
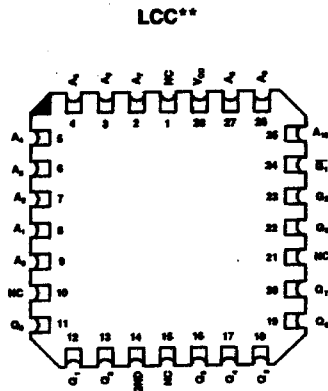
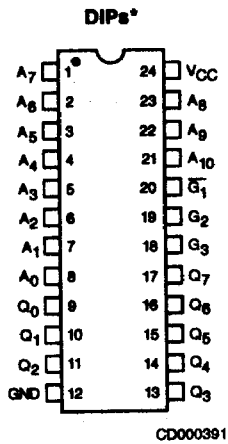
*E nomenclature applies to the power-switched versions only (Am27PSXXX).

PRODUCT SELECTOR GUIDE

| Three-State Part Number | Am27S191SA, Am27S291SA | | Am27S191A, Am27S291A | | Am27S191, Am27S291 | | Am27PS191A, Am27PS291A | | Am27PS191, Am27PS291 | |
|--------------------------|------------------------|----|----------------------|----|--------------------|----|------------------------|----|----------------------|----|
| Address Access Time (ns) | 25 | 30 | 35 | 50 | 50 | 65 | 50 | 65 | 65 | 75 |
| Operating Range | C | M | C | M | C | M | C | M | C | M |



CONNECTION DIAGRAMS Top View

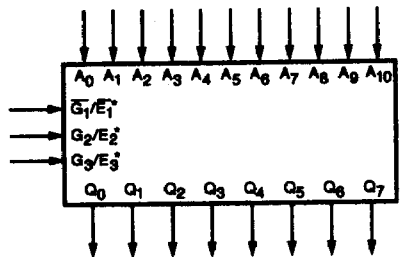


*Also available in a 24-pin Flatpack.
Pinout identical to DIPs.

**Also available in a 28-pin Square PLCC. Pinout identical to LCC.

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



LS000033

*E nomenclature applies to the power-switched versions only (Am27PSXXX).

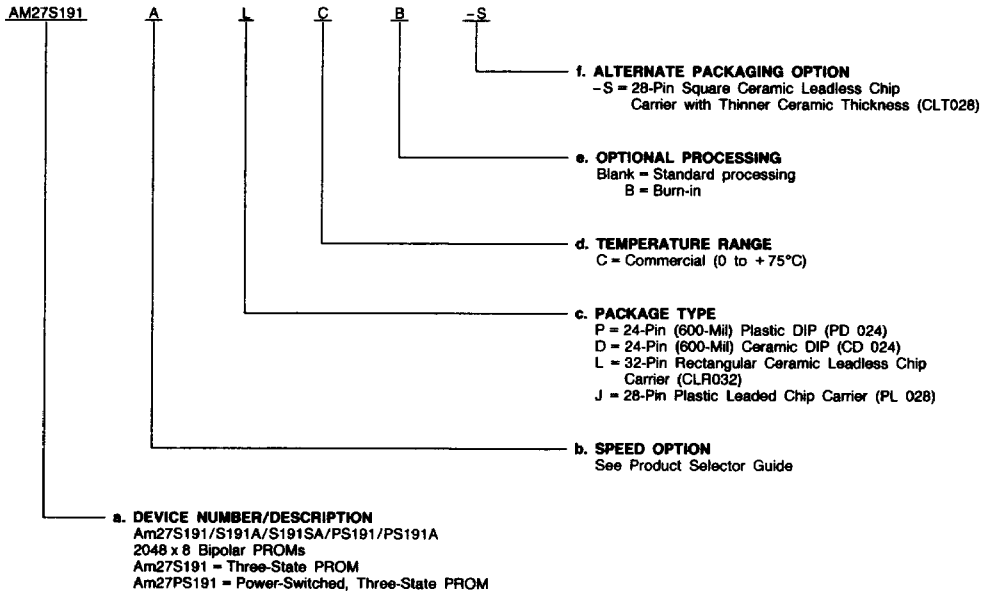
ORDERING INFORMATION

(Am27S191/27PS191)

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Speed Option (if applicable)
- c. Package Type
- d. Temperature Range
- e. Optional Processing
- f. Alternate Packaging Option



| Valid Combinations | |
|--------------------|---|
| AM27S191 | PC, PCB, DC, DCB, LC, LCB, LC-S, LCB-S, JC, JCB |
| AM27S191A | |
| AM27S191SA | |
| AM27PS191 | |
| AM27PS191A | |

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

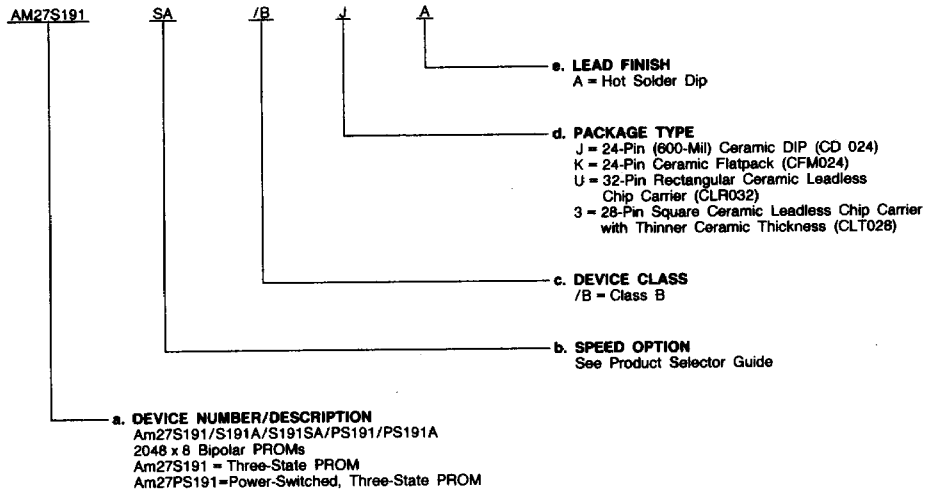
MILITARY ORDERING INFORMATION

(Am27S191/27PS191)

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

- a. Device Number
- b. Speed Option (if applicable)
- c. Device Class
- d. Package Type
- e. Lead Finish



| Valid Combinations | |
|--------------------|---------------------------|
| AM27S191 | /BJA, /BKA, /BUA, /B3A |
| AM27S191A | |
| AM27S191SA | |
| AM27PS191 | |
| AM27PS191A | |

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11.

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

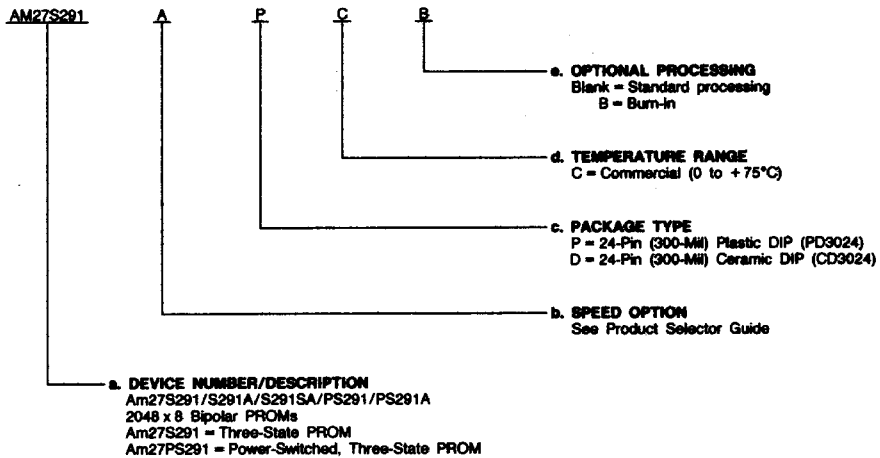
ORDERING INFORMATION

(Am27S291/27PS291)

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Speed Option (if applicable)
- c. Package Type
- d. Temperature Range
- e. Optional Processing



| Valid Combinations | |
|--------------------|------------------|
| AM27S291 | PC, PCB, DC, DCB |
| AM27S291A | |
| AM27S291SA | |
| AM27PS291 | |
| AM27PS291A | |

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

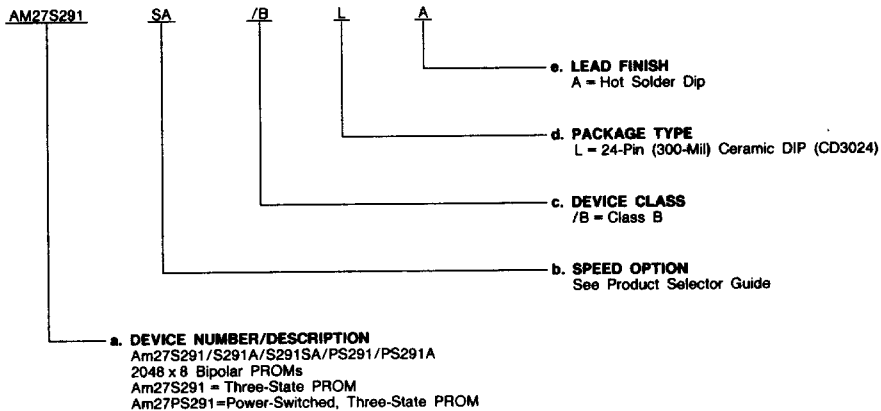
MILITARY ORDERING INFORMATION

(Am27S291/27PS291)

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

- a. Device Number
- b. Speed Option (if applicable)
- c. Device Class
- d. Package Type
- e. Lead Finish



| Valid Combinations | |
|--------------------|------|
| AM27S291 | /BLA |
| AM27S291A | |
| AM27S291SA | |
| AM27PS291 | |
| AM27PS291A | |

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11.

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

PIN DESCRIPTION

A₀ - A₁₀ Address Inputs (Input)

The 11-bit field presented at the address inputs selects one of 2048 memory locations to be read from.

Q₀ - Q₇ Data Output Port (Output)

The outputs whose state represents the data read from the selected memory locations.

\overline{G}_1, G_2, G_3 Output Enable (Input)

Provides direct control of the Q-output buffers. Outputs disabled forces all open-collector outputs to an "OFF" state

and all three-state outputs to a floating or high-impedance state.

$$\text{Enable} = \overline{G}_1 \cdot G_2 \cdot G_3$$

$$\begin{aligned}\text{Disable} &= \overline{G}_1 \cdot G_2 \cdot G_3 \\ &= G_1 + \overline{G}_2 + \overline{G}_3\end{aligned}$$

V_{CC} Device Power Supply Pin

The most positive of the logic power supply pins.

GND Device Power Supply Pin

The most negative of the logic power supply pins.

FUNCTIONAL DESCRIPTION

Notes on Power Switching

The Am27PS191 and Am27PS291 are power-switched devices. When the chip is selected, important internal currents increase from small idling or standby values to their larger selected values. This transition occurs very rapidly, meaning that access times from the powered-down state are only slightly slower than from the powered-up state. Deselected, I_{CC} is reduced to less than half its full operating amount. Due to this unique feature, there are special considerations which should be followed in order to optimize performance:

1. When the Am27PS191 and Am27PS291 are selected, a current surge is placed on the V_{CC} supply due to the power-up feature. In order to minimize the effects of this current transient, it is recommended that a 0.1μf ceramic capacitor be connected from pin 24 to pin 12 at each device. (See Figure 1.)
2. Address access time (TAVQV) can be optimized if a chip enable set-up time (TEVAV) of greater than 25ns is observed. Negative set-up times on chip enable (TEVAV < 0) should be avoided. (For typical and worse case characteristics, see Figures 2A and 2B.)

ABSOLUTE MAXIMUM RATINGS

| | |
|--|---------------------------------|
| Storage Temperature | -65 to +150°C |
| Ambient Temperature with Power Applied | -55 to +125°C |
| Supply Voltage | -0.5 V to +7.0 V |
| DC Voltage Applied to Outputs (Except During Programming) | -0.5 V to +V _{CC} Max. |
| DC Voltage Applied to Outputs During Programming | 21 V |
| Output Current into Outputs During Programming (Max. Duration of 1 sec) | 250 mA |
| DC Input Voltage | -0.5 V to +5.5 V |
| DC Input Current | -30 mA to +5 mA |

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

| | |
|---|--------------------|
| Commercial (C) Devices | |
| Ambient Temperature (T _A) | 0 to +75°C |
| Supply Voltage (V _{CC}) | +4.75 V to +5.25 V |
| Military (M) Devices* | |
| Case Temperature (T _C) | -55 to +125°C |
| Supply Voltage (V _{CC}) | +4.5 V to +5.5 V |

Operating ranges define those limits between which the functionality of the device is guaranteed.

*Military product 100% tested at T_C = +25°C, +125°C, and -55°C.

DC CHARACTERISTICS over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

| Parameter Symbol | Parameter Description | Test Conditions | Min. | Typ. | Max. | Unit |
|--------------------------|------------------------------|---|--|------|------------|------|
| V _{OH} (Note 1) | Output HIGH Voltage | V _{CC} = Min., I _{OH} = -2.0 mA V _{IN} = V _{IH} or V _{IL} | 2.4 | | | V |
| V _{OL} | Output LOW Voltage | V _{CC} = Min., I _{OL} = 16 mA V _{IN} = V _{IH} or V _{IL} | | | 0.50 | V |
| V _{IH} | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs (Note 3) | 2.0 | | | V |
| V _{IL} | Input LOW Level | Guaranteed input logical LOW voltage for all inputs (Note 3) | | | 0.8 | V |
| I _{IL} | Input LOW Current | V _{CC} = Max., V _{IN} = 0.45 V | | | -0.250 | mA |
| I _{IH} | Input HIGH Current | V _{CC} = Max., V _{IN} = V _{CC} | | | 40 | μA |
| I _{SC} | Output Short-Circuit Current | V _{CC} = Max., V _{OUT} = 0.0 V (Note 1) | COM'L -20 MIL -15 | | -90 -90 | mA |
| I _{CC} | Power Supply Current | All inputs = GND, V _{CC} = Max. | | | 185 | mA |
| V _I | Input Clamp Voltage | V _{CC} = Min., I _{IN} = -18 mA | | | -1.2 | V |
| I _{CEX} | Output Leakage Current | V _{CC} = Max., V _{G1} = 2.4 V | V _O = V _{CC} V _O = 0.4 V | | 40 -40 | μA |
| C _{IN} | Input Capacitance | V _{IN} = 2.0 V @ f = 1 MHz (Note 2) V _{CC} = 5 V, T _A = 25°C | | 4.0 | | pF |
| C _{OUT} | Output Capacitance | V _{OUT} = 2.0 V @ f = 1 MHz (Note 2) V _{CC} = 5 V, T _A = 25°C | | 8.0 | | pF |

- Notes: 1. Not more than one output should be shorted at a time. Duration of the short-circuit test should not be more than one second.
2. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted*)

| No. | Parameter Symbol | Parameter Description | Version | Am27S Version | | Am27PS Version | | Unit |
|-----|------------------|---|---------|---------------|------|----------------|------|------|
| | | | | COM'L | MIL | COM'L | MIL | |
| | | | | Max. | Max. | Max. | Max. | |
| 1 | TAVQV | Address Valid to Output Valid Access Time | SA | 25 | 30 | | | ns |
| | | | A | 35 | 50 | 50 | 65 | |
| | | | STD | 50 | 65 | 65 | 75 | |
| 2 | TGVQZ TEVQZ | Delay from Output Enable Valid to Output Hi-Z | SA | 18 | 20 | | | ns |
| | | | A | 25 | 30 | 25 | 30 | |
| | | | STD | 25 | 30 | 35 | 45 | |
| 3 | TGVQV TEVQV | Delay from Output Enable Valid to Output Valid | SA | 18 | 20 | | | ns |
| | | | A | 25 | 30 | 65 | 75 | |
| | | | STD | 25 | 30 | 80 | 90 | |
| 4 | TAVQV1 | Power-Switched Address Valid to Output Valid Access Time (Am27PS Versions only) | A | | | 65 | 75 | ns |
| | | | STD | | | 80 | 90 | |

See also Switching Test Circuits.

Notes: 1. Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V.

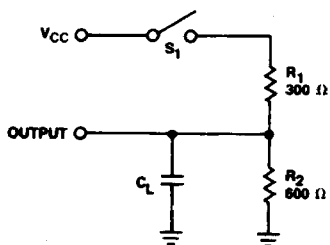
2. TGVQZ is measured at steady state HIGH output voltage -0.5 V and steady state LOW output voltage +0.5 V output levels.

3. TAVQV is tested with switch S_1 closed and $C_L = 50$ pF.

4. TGVQV is tested with $C_L = 50$ pF to the 1.5 V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. TGVQZ is tested with $C_L = 5$ pF. HIGH to high impedance tests are made with S_1 open to an output voltage of steady state HIGH -0.5 V with S_1 open; LOW-to-HIGH impedance tests are made to the steady state LOW +0.5 V level with S_1 closed.

*Subgroups 7 and 8 apply to functional tests.






SWITCHING TEST CIRCUIT



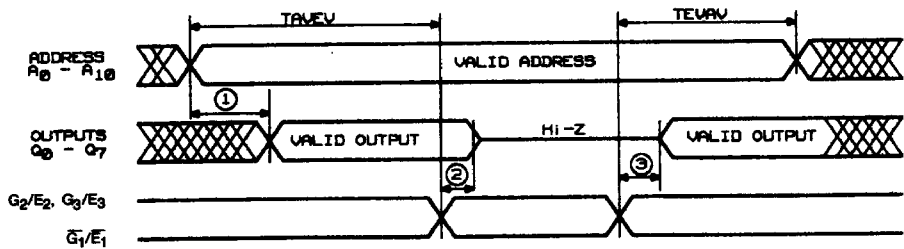
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SWITCHING WAVEFORMS

KEY TO SWITCHING WAVEFORMS

| WAVEFORM | INPUTS | OUTPUTS |
|---|----------------------------------|---|
|  | MUST BE STEADY | WILL BE STEADY |
|  | MAY CHANGE FROM H TO L | WILL BE CHANGING FROM H TO L |
|  | MAY CHANGE FROM L TO H | WILL BE CHANGING FROM L TO H |
|  | DON'T CARE; ANY CHANGE PERMITTED | CHANGING; STATE UNKNOWN |
|  | DOES NOT APPLY | CENTER LINE IS HIGH IMPEDANCE "OFF" STATE |

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