PCB **SN54ALS165, SN74ALS165**
PARALLEL-LOAD 8-BIT REGISTERS

- **Complementary Outputs**
- **Direct Overriding Load (Data) Inputs**
- **Gated Clock Inputs**
- **Parallel-to-Serial Data Conversion**
- **Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**
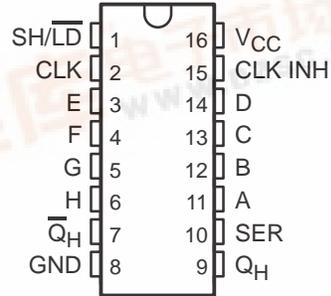
SN54ALS165 . . . J PACKAGE
SN74ALS165 . . . D OR N PACKAGE
(TOP VIEW)

```
SH/LD [ 1      16 ] V_CC
  CLK [ 2      15 ] CLK INH
    E [ 3      14 ] D
    F [ 4      13 ] C
    G [ 5      12 ] B
    H [ 6      11 ] A
   Q̄_H [ 7     10 ] SER
  GND [ 8       9 ] Q_H
```

SN54ALS165 . . . FK PACKAGE
(TOP VIEW)

```
         CLK  SH/LD  NC  V_CC  CLK INH
          3    2     1   20    19
    E [ 4                       18 ] D
    F [ 5                       17 ] C
   NC [ 6                       16 ] NC
    G [ 7                       15 ] B
    H [ 8                       14 ] A
          9    10    11   12    13
         |Q̄_H  GND   NC   Q_H   SER
```

NC – No internal connection

description

The 'ALS165 are parallel-load 8-bit serial shift registers that, when clocked, shift the data toward serial (Q_H and $\overline{Q}_H$) outputs. Parallel-in access to each stage is provided by eight individual direct data (A–H) inputs that are enabled by a low level at the shift/load (SH/$\overline{LD}$) input. The 'ALS165 have a clock-inhibit function and complemented serial outputs.
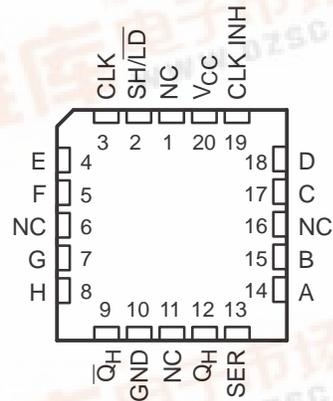
Clocking is accomplished by a low-to-high transition of the clock (CLK) input while SH/$\overline{LD}$ is held high and the clock inhibit (CLK INH) input is held low. The functions of CLK and CLK INH are interchangeable. Since a low CLK and a low-to-high transition of CLK INH also accomplishes clocking, CLK INH should be changed to the high level only while CLK is high. Parallel loading is inhibited when SH/$\overline{LD}$ is held high. The parallel inputs to the register are enabled while SH/$\overline{LD}$ is low independently of the levels of the CLK, CLK INH, or serial (SER) inputs.

The SN54ALS165 is characterized for operation over the full military temperature range of $-55°C$ to $125°C$. The SN74ALS165 is characterized for operation from $0°C$ to $70°C$.

FUNCTION TABLE

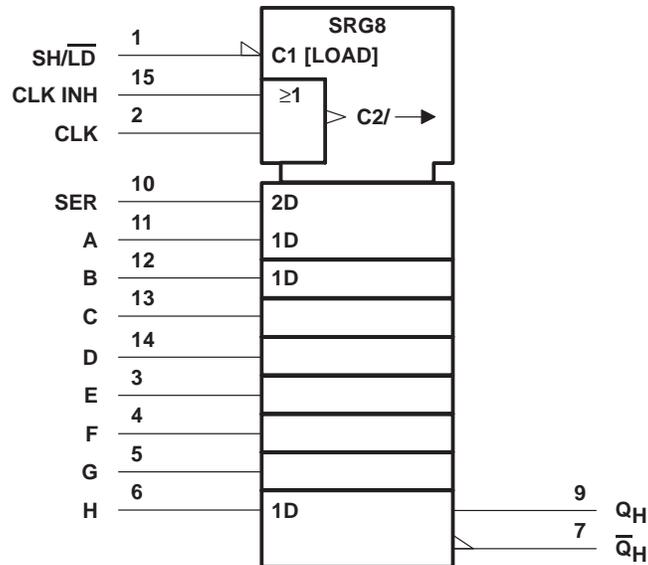| INPUTS			FUNCTION
SH/$\overline{LD}$	CLK	CLK INH	
L	X	X	Parallel load
H	H	X	No change
H	X	H	No change
H	L	↑	Shift[†]
H	↑	L	Shift[†]

[†] Shift = content of each internal register shifts toward serial outputs. Data at SER is shifted into first register.

TEXAS INSTRUMENTS

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SN54ALS165, SN74ALS165
PARALLEL-LOAD 8-BIT REGISTERS

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.
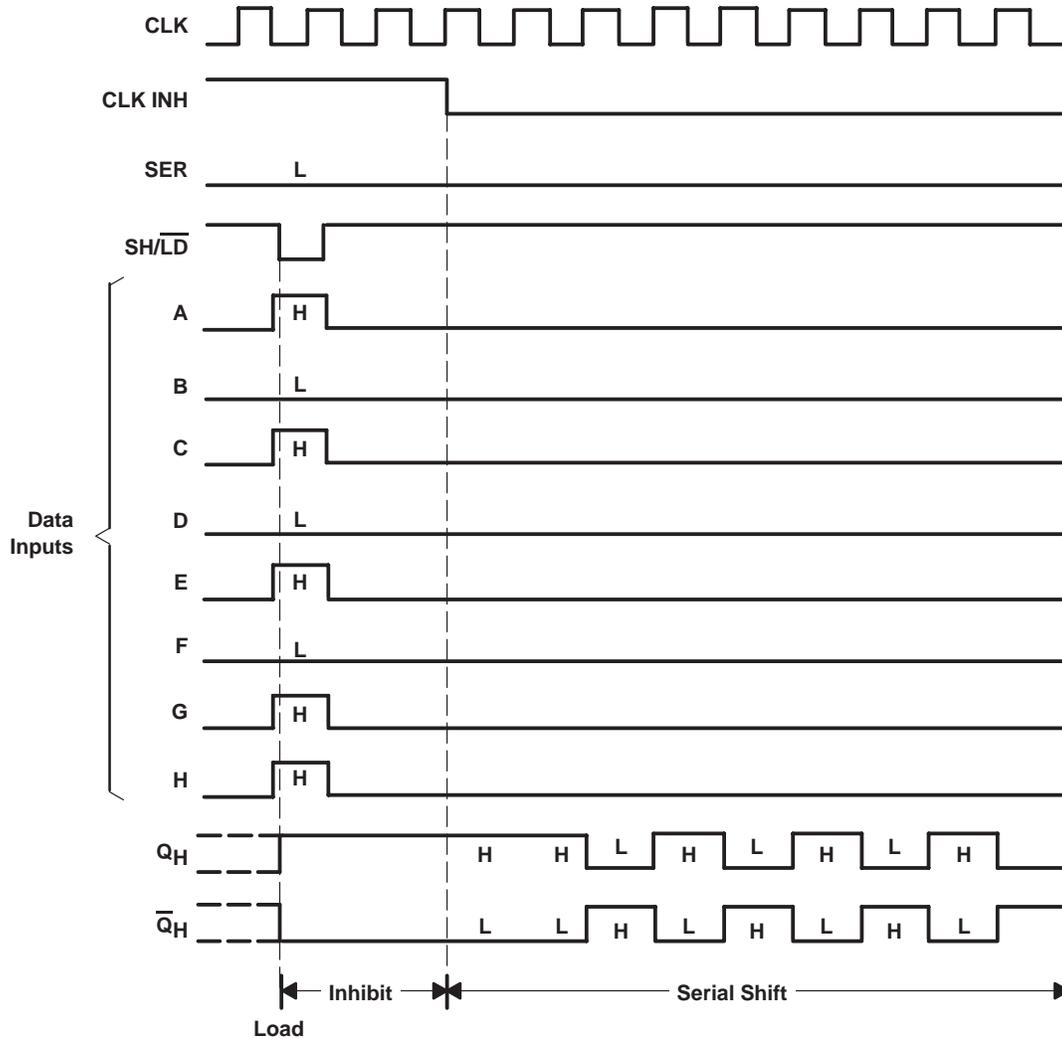
logic diagram (positive logic)
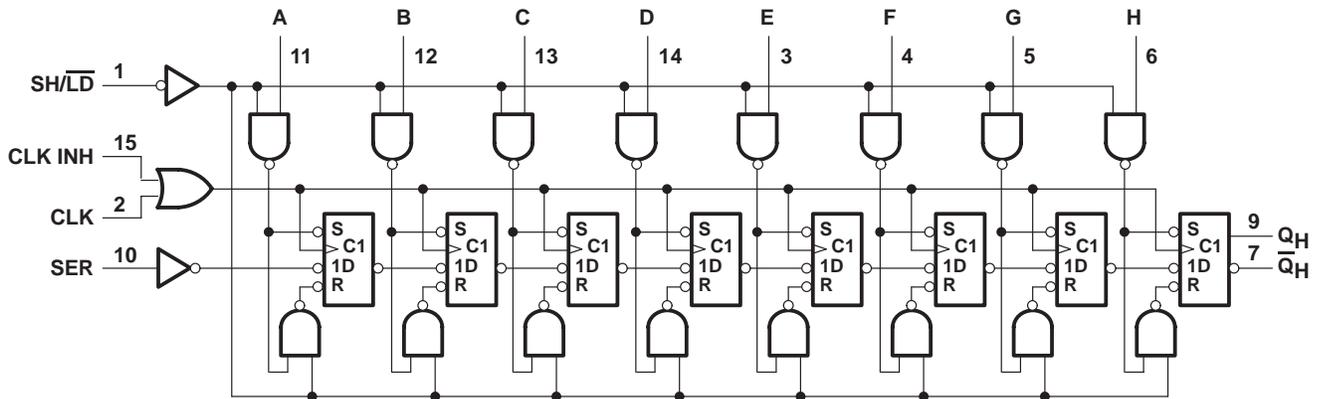
Pin numbers shown are for the D, J, and N packages.

typical shift, load, and inhibit sequences

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} .... 7 V

Input voltage, V_I .... 7 V

Operating free-air temperature range, T_A: SN54ALS165 .... −55°C to 125°C

SN74ALS165 .... 0°C to 70°C

Storage temperature range .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

SN54ALS165, SN74ALS165
PARALLEL-LOAD 8-BIT REGISTERS

recommended operating conditions

			SN54ALS165			SN74ALS165			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		35	0		45	MHz
$t_{w(CLK)}$	Pulse duration, CLK (see Figure 1)	CLK high	14			11			ns
		CLK low	14			11			
$t_{w(load)}$	Pulse duration, SH/$\overline{LD}$ low	CLK low	15			12			ns
t_{su1}	Setup time, clock enable (see Figure 1)		15			11			ns
t_{su2}	Setup time, parallel input (see Figure 1)		11			10			ns
t_{su3}	Setup time, serial input (see Figure 2)		11			10			ns
t_{su4}	Setup time, shift (see Figure 2)		15			10			ns
t_h	Hold time at any input		4			4			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS165			SN74ALS165			UNIT
			MIN	TYP[†]	MAX	MIN	TYP[†]	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} −2			V_{CC} −2			V
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O[‡]	V_{CC} = 5.5 V,	V_O = 2.25 V	−20		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V,	See Note 1		12	24		12	24	mA

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.
[‡] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: With the outputs open, CLK INH and CLK at 4.5 V, and a clock pulse applied to SH/$\overline{LD}$, I_{CC} is measured first with the parallel inputs at 4.5 V, then with the parallel inputs grounded.

switching characteristics (see Figures 1, 2, and 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX†				UNIT
			SN54ALS165		SN74ALS165		
			MIN	MAX	MIN	MAX	
f_{max}			35		45		MHz
t_{PLH}	SH/$\overline{LD}$	Any	4	23	4	20	ns
t_{PHL}			4	23	4	22	
t_{PLH}	CLK	Any	3	14	3	13	ns
t_{PHL}			3	15	3	14	
t_{PLH}	H	Q_H	3	14	3	13	ns
t_{PHL}			3	18	3	16	
t_{PLH}	H	Q_H	2	17	2	15	ns
t_{PHL}			3	17	3	16	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
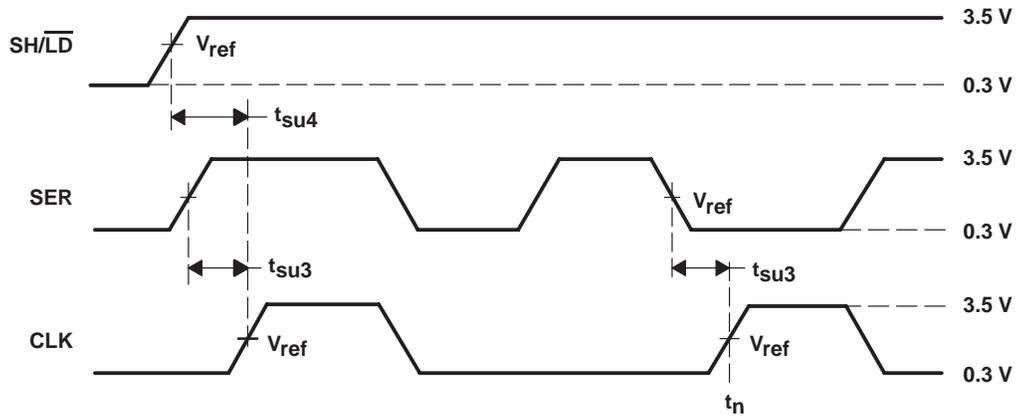
PARAMETER MEASUREMENT INFORMATION
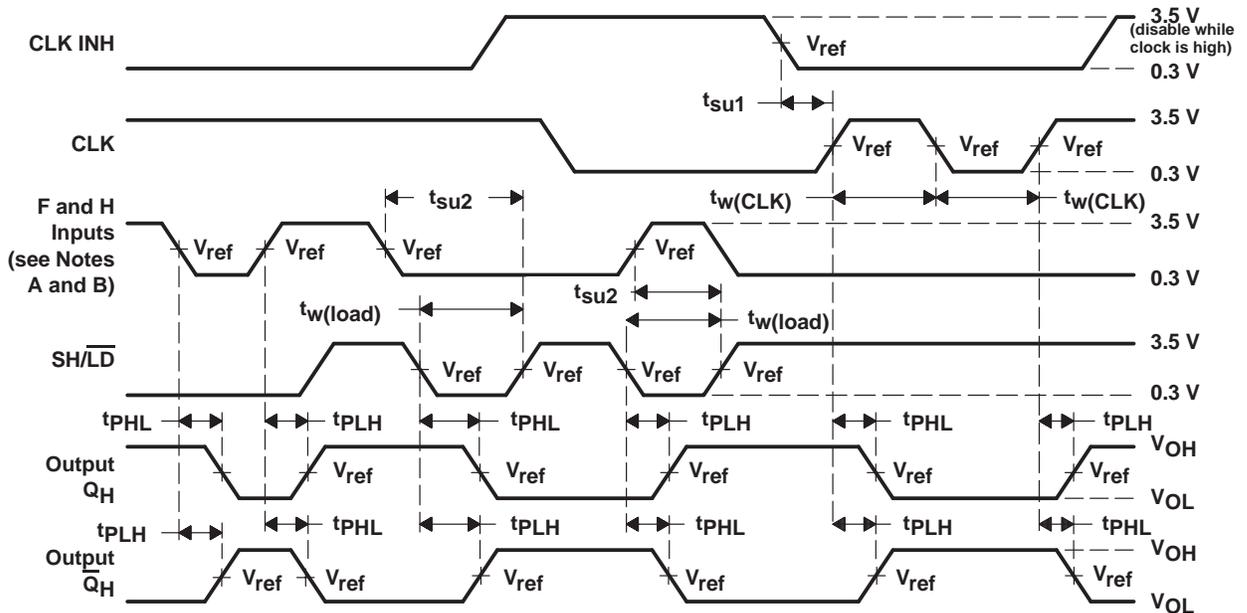
NOTES: A. The remaining six data inputs and SER are low.
B. Prior to test, high-level data is loaded into the H input.
C. The input pulse generators have the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $t_r = t_f = 2$ ns.
D. V_{ref} = 1.3 V

Figure 1. Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

NOTES: A. The eight data inputs and CLK INH are low. Results are monitored at Q_H at t_{n+7}.
   B. The input pulse generators have the following characteristics: PRR $\leq$ 1 MHz, duty cycle = 50%, $t_r = t_f = 2$ ns.
   C. $V_{ref} = 1.3$ V

Figure 2. Voltage Waveforms
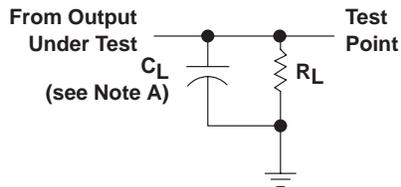
NOTE A: C_L includes probe and jig capacitance.

Figure 3. Load Circuit for Switching Tests

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SN74ALS165D	ACTIVE	SOIC	D	16	40	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74ALS165DR	ACTIVE	SOIC	D	16	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74ALS165N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74ALS165N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SNJ54ALS165J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SNJ54ALS165W	OBSOLETE	CFP	W	16		TBD	Call TI	Call TI

[1] The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
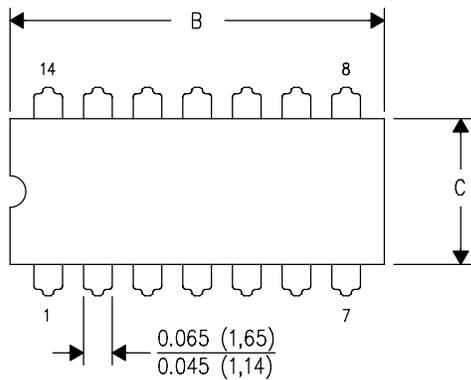
14 LEADS SHOWN

DIM PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

C

1   7

$\frac{0.065\ (1,65)}{0.045\ (1,14)}$

0.005 (0,13) MIN

$\frac{0.060\ (1,52)}{0.015\ (0,38)}$

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

$\frac{0.026\ (0,66)}{0.014\ (0,36)}$

0.100 (2,54)

A

0°-15°

$\frac{0.014\ (0,36)}{0.008\ (0,20)}$
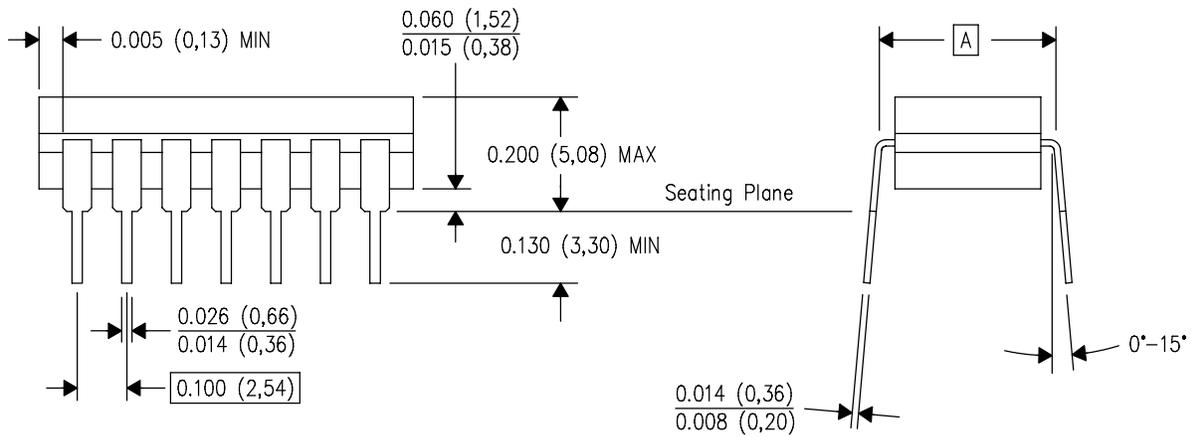
4040083/F 03/03

NOTES: A.   All linear dimensions are in inches (millimeters).
B.   This drawing is subject to change without notice.
C.   This package is hermetically sealed with a ceramic lid using glass frit.
D.   Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E.   Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R−GDFP−F16)

CERAMIC DUAL FLATPACK

Base and Seating Plane

$\dfrac{0.285\ (7,24)}{0.245\ (6,22)}$

$\dfrac{0.045\ (1,14)}{0.026\ (0,66)}$

$\dfrac{0.080\ (2,03)}{0.055\ (1,40)}$

$\dfrac{0.006\ (0,15)}{0.004\ (0,10)}$

0.305 (7,75) MAX

$\dfrac{0.019\ (0,48)}{0.015\ (0,38)}$

1   16

$\dfrac{0.430\ (10,92)}{0.370\ (9,40)}$

0.050 (1,27)

0.005 (0,13) MIN
4 Places

8   9

$\dfrac{0.360\ (9,14)}{0.250\ (6,35)}$

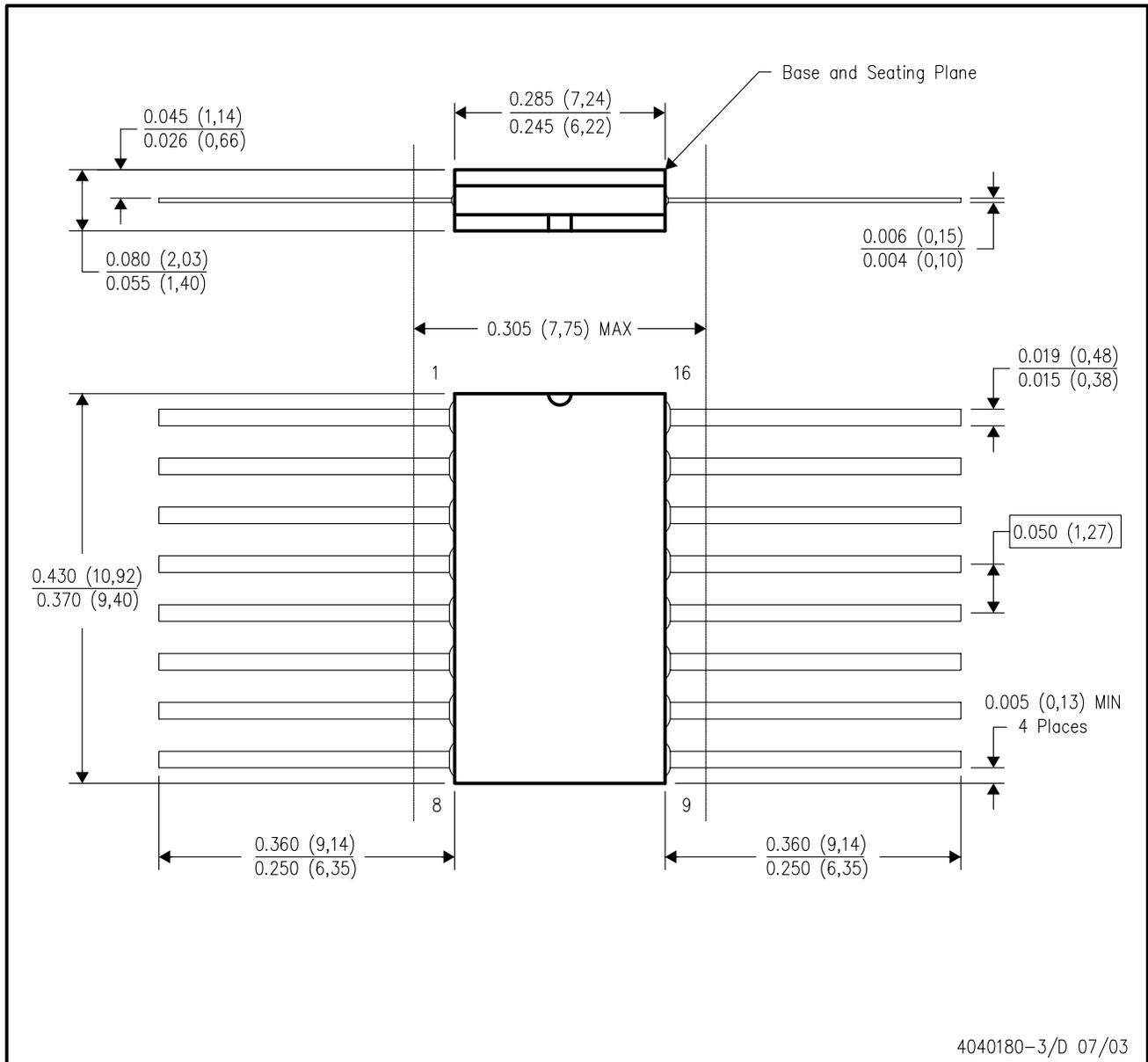$\dfrac{0.360\ (9,14)}{0.250\ (6,35)}$

4040180−3/D 07/03

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   This package can be hermetically sealed with a ceramic lid using glass frit.
         D.   Index point is provided on cap for terminal identification only.
         E.   Falls within MIL STD 1835 GDFP1−F16 and JEDEC MO−092AC

N (R−PDIP−T**)   PLASTIC DUAL−IN−LINE PACKAGE
16 PINS SHOWN
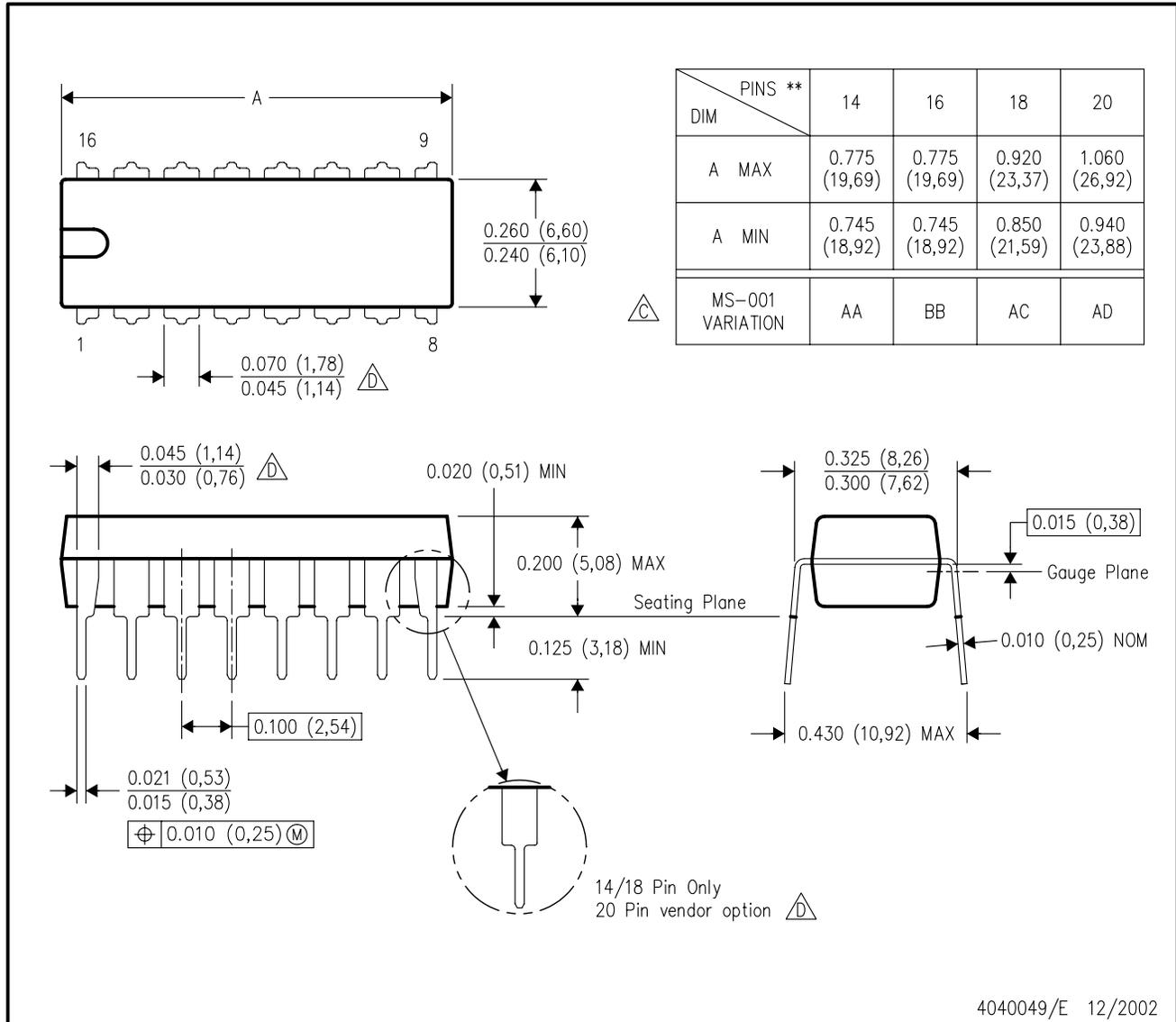
DIM ⟍ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
△C MS−001 VARIATION	AA	BB	AC	AD

0.260 (6,60)
0.240 (6,10)

0.070 (1,78)
0.045 (1,14) △D

0.045 (1,14)
0.030 (0,76) △D

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option △D

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

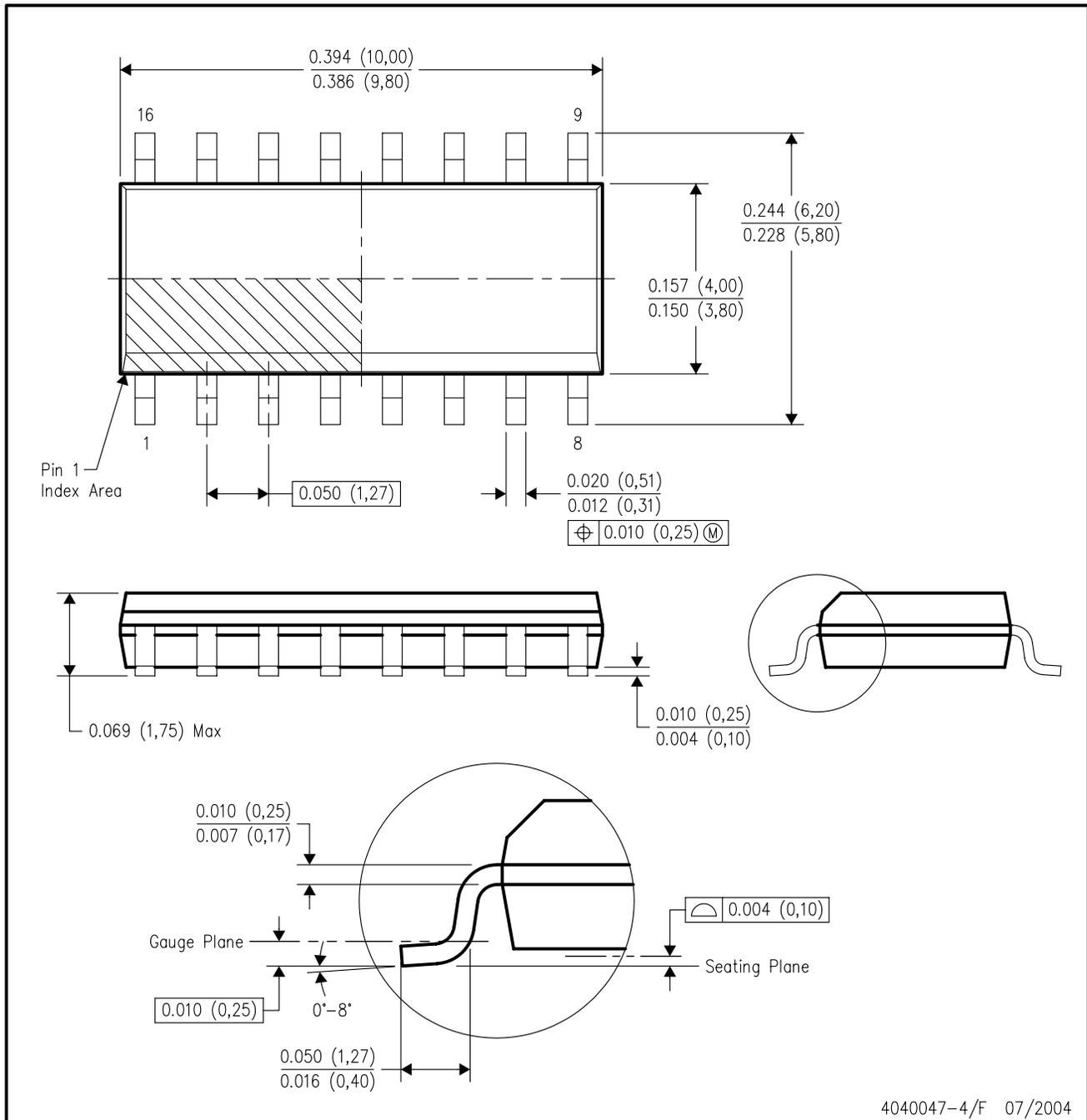0.430 (10,92) MAX

4040049/E 12/2002

NOTES: A.   All linear dimensions are in inches (millimeters).
          B.   This drawing is subject to change without notice.
       △C   Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
       △D   The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R−PDSO−G16) PLASTIC SMALL−OUTLINE PACKAGE

0.394 (10,00)
0.386 (9,80)

16

9

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)

1

8

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.007 (0,17)

Gauge Plane

0.004 (0,10)

Seating Plane

0.010 (0,25)

0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−4/F 07/2004

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS−012 variation AC.

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