



100BASE-X Fiber Physical Layer With 5-bit Interface

GENERAL DESCRIPTION

The ML6695 implements the physical layer of the Fast Ethernet 100BASE-X standard for fiber media. The device provides the 5-bit (or symbol) interface for interface to upper-layer silicon. The ML6695 integrates the data quantizer and the LED driver, allowing the use of low cost optical PMD components.

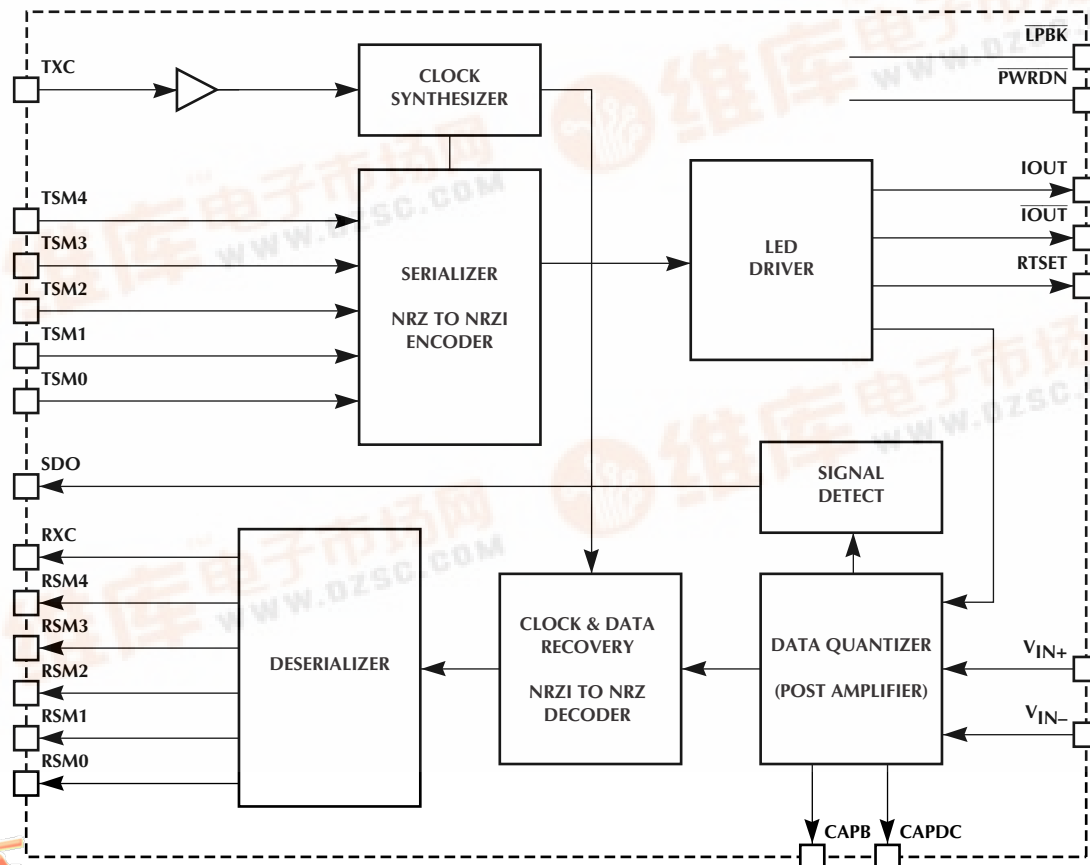
The ML6695 includes 125MHz clock recovery/clock generation, an LED driver, and a data quantizer (post amplifier). The device also offers a power down mode which results in total power consumption of less than 20mA.

The ML6695 is suitable for the current 100BASE-FX IEEE 803.2u standard defined using 1300nm optics, as well as for the *proposed* 100BASE-SX standard defined using lower cost 820nm optics.

FEATURES

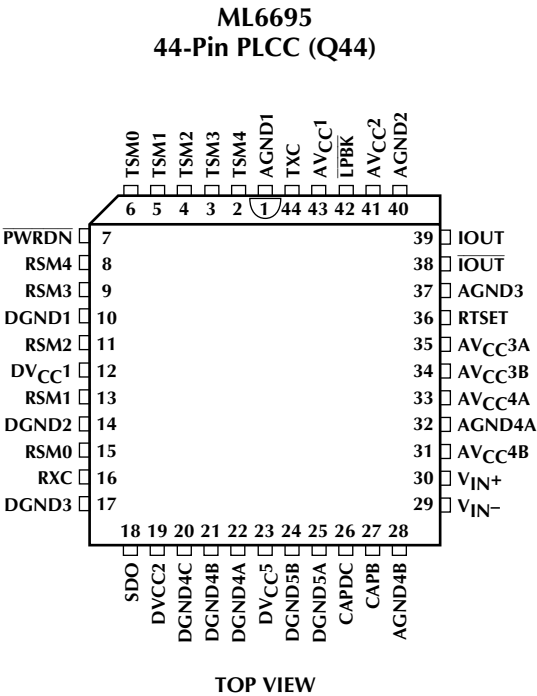
- 100BASE-FX physical layer with 5-bit interface
- Optimal 100BASE-SX solution (draft standard)
- Integrated data quantizer (post-amplifier)
- Integrated LED driver
- 125MHz clock generation and recovery
- Power-down mode

BLOCK DIAGRAM



ML6695

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	FUNCTION	PIN	NAME	FUNCTION
1	AGND1	Analog ground	5	TSM1	Transmit data TTL inputs. TSM 0-4 inputs accept TX data symbols from the MII. Data appearing at TSM 0-4 are clocked into the ML6695 on the rising edge of TXCLK .
2	TSM4	Transmit data TTL inputs. TSM 0-4 inputs accept TX data symbols from the MII. Data appearing at TSM 0-4 are clocked into the ML6695 on the rising edge of TXCLK .	6	TSM0	Transmit data TTL inputs. TSM 0-4 inputs accept TX data symbols from the MII. Data appearing at TSM 0-4 are clocked into the ML6695 on the rising edge of TXC.
3	TSM3	Transmit data TTL inputs. TSM 0-4 inputs accept TX data symbols from the MII. Data appearing at TSM 0-4 are clocked into the ML6695 on the rising edge of TXC.	7	PWRDN	Powerdown TTL input. Driving this pin low, or floating the pin, powers the ML6695 down to a low-current, inoperative state. Driving PWRDN high enables the ML6695.
4	TSM2	Transmit data TTL inputs. TSM 0-4 inputs accept TX data symbols from the MII. Data appearing at TSM 0-4 are clocked into the ML6695 on the rising edge of TXC.	8	RSM4	Receive data TTL outputs. RSM 0-4 output may be sampled synchronously with RXC's rising edge.

PIN DESCRIPTION (Continued)

PIN	NAME	FUNCTION	PIN	NAME	FUNCTION
9	RSM3	Receive data TTL outputs. RSM 0-4 output may be sampled synchronously with RXC's rising edge.	26	CAPDC	Data quantizer offset-correction loop, offset-storage capacitor input pin. The capacitor tied between this pin and AV _{CC} stores the amplified data quantizer offset voltage and also sets the dominant pole in the offset-correction loop. A 0.1μF surface mount is recommended.
10	DGND1	Digital ground			
11	RSM2	Receive data TTL outputs. RSM 0-4 output may be sampled synchronously with RXC's rising edge.	27	CAPB	Data quantizer input bias bypass capacitor input. The capacitor tied between this pin and AV _{CC} filters the quantizer's internal input bias reference. A 0.1μF surface-mount capacitor is recommended.
12	DV _{CC} 1	Digital positive power supply			
13	RSM1	Receive data TTL outputs. RSM 0-4 output may be sampled synchronously with RXC's rising edge.	28	AGND4B	Analog ground
14	DGND2	Digital ground	29	V _{IN} -	Receive quantizer input. This differential input pair receives 100BASE-FX NRZI signals from the network opto-coupler.
15	RSM0	Receive data TTL outputs. RSM 0-4 output may be sampled synchronously with RXC's rising edge.	30	V _{IN} +	Receive quantizer input. This differential input pair receives 100BASE-FX NRZI signals from the network opto-coupler.
16	RXC	Recovered receive symbol clock TTL output. This 25MHz clock is phase-aligned with the internal 125MHz bit clock recovered from the signal received at V _{IN} +/- . Receive data are clocked out at RSM 0-4 on the falling edges of this clock.	31	AV _{CC} 4B	Analog positive power supply
			32	AGND4A	Analog ground
			33	AV _{CC} 4A	Analog positive power supply
17	DGND3	Digital ground	34	AV _{CC} 3B	Analog positive power supply
18	SDO	Signal Detect TTL output. This output goes high when the signal at V _{IN} +/- exceeds the preset amplitude threshold.	35	AV _{CC} 3A	Analog positive power supply
			36	RTSET	Transmit level bias resistor. For 100BASE-FX, an external 2.32kΩ, 1% resistor connected between RTSET and AGND3 sets a precision constant bias current that gives a nominal output "on" current of 75mA at I _{OUT} .
19	DV _{CC} 2	Digital positive power supply			
20	DGND4C	Digital ground	37	AGND3	Analog ground
21	DGND4B	Digital ground			
22	DGND4	Digital ground	38	I _{OUT}	Transmit LED output. This pin connects through an external 15Ω resistor to AV _{CC} when the part is used to drive a network LED.
23	DV _{CC} 5	Digital positive power supply			
24	DGND5B	Digital ground			
25	DGND5A	Digital ground			

ML6695

PIN DESCRIPTION (Continued)

PIN	NAME	FUNCTION	PIN	NAME	FUNCTION
39	IOUT	Transmit LED output. This open-collector current output drives NRZI waveforms into an LED. Output current can be set externally by choosing RTSET value.	43	AV _{CC1}	Analog positive power supply
40	AGND2	Analog ground	44	TXC	Transmit clock TTL input. This 25MHz clock is phase-aligned with the internal 125MHz TX bit clock. Data appearing at Tsm<4:0> are clocked into the ML6695 on the rising edge of this clock.
41	AV _{CC2}	Analog positive power supply			
42	$\overline{\text{LPBK}}$	Loopback TTL input pin. Tying this pin to ground places the part in loopback mode; data at TSM0 0-4 are serialized, then sent to the quantizer, followed by the receive PLL for clock recovery, and finally to the RSM<4:07> outputs. Floating this pin or tying it to V _{CC} places the part in its normal mode of operation.			

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

V _{CC} Supply Voltage Range	–0.3V to 6V
Input Voltage Range	
Digital Inputs	–0.3V to V _{CC}
VIN+, VIN–, TXC, CAPDC, CAPB	–0.3V to V _{CC}
Output Current	
I _{OUT} , I _{OUT}	90mA
All Other Outputs	10mA

Junction Temperature	0°C to 125°C
Storage Temperature	–65°C to 150°C
Lead Temperature (Soldering, 10 sec)	260°C
Thermal Resistance (θ _{JA})	
PLCC	53°C/W

OPERATING CONDITIONS

Temperature Range	0°C to 70°C
V _{CC} Supply Voltage	5V ±5%
All V _{CC} supply pins <i>must</i> be within 0.1V of each other.	
All GND pins <i>must</i> be within 0.1V of each other.	

DC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{CC} = 5V ±5%, T_A = Operating Temperature Range (Note 1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
TTL INPUTS (TSM<4:0>, LPBK, TXC, PWRDN)						
V _{IL}	Input Low Voltage	I _{IL} = –400μA	–0.3		0.8	V
V _{IH}	Input High Voltage	I _{IH} = 100μA	2.0		V _{CC} +0.3	V
I _{IL}	Input Low Current	V _{IN} = 0.4V	–200			μA
I _{IH}	Input High Current	V _{IN} = 2.4V			100	μA
TTL OUTPUTS (RSM<4:0>, RXC, SDO)						
V _{OL}	Output Low Voltage	I _{OL} = 4mA			0.4	V
V _{OH}	Output High Voltage	I _{OH} = –4mA	2.4			
RECEIVER						
V _{ICM}	V _{IN} +/- input common-mode voltage	V _{CC} = 5V		2.5		V
V _{ID}	V _{IN} +/- differential input voltage range		3.5		1700	mV _{P-P}
R _{IDR}	V _{IN} +/- differential input resistance		500		1k	Ω
V _{SDA}	Signal detect assertion threshold	peak-to-peak non-idle signal level at V _{IN} +/- for SDO assertion	8		12	mV _{P-P}
A _{HYST}	Input hysteresis		1.5		2	dB
I _{RT}	RTSET input current	RTSET = 2.32kΩ ±1%	486	540	594	μA
TRANSMITTER						
I _{LEDH}	I _{OUT} high output current (Note 2)	RTSET = 2.32kΩ ±1%	67.5	75	82.5	mA
I _{LEDL}	I _{OUT} /I _{OUT} low output current	RTSET = 2.32kΩ ±1%			0.1	mA
POWER SUPPLY CURRENT						
I _{CC}	Supply Current, 100BASE-FX operation, transmitting	Current into all V _{CC} pins, V _{CC} = 5.25V		200	295	mA
I _{PD}	Supply Current, Powerdown Mode				20	mA

ML6695

AC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $V_{CC} = 5V \pm 5\%$, T_A = Operating Temperature Range (Note 1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
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TRANSMITTER (NOTE 8)

$t_{TR/F}$	I_{OUT} rise/fall time	Note 3			2	ns
t_{TDC}	I_{OUT} output duty cycle distortion	Note 3	-0.5		0.5	ns

SIGNAL DETECT

t_{AS}	SDO assert time (SDO low to high)	$V_{IN} > 8mV_{p-p}$			100	μs
t_{ANS}	SDO deassert time (SDO high to low)	$V_{IN} < 8mV_{p-p}$	350			μs

DATA INTERFACE

X_{NTOL}	TX input clock frequency tolerance	25MHz frequency	-50		50	ppm
t_{TPWH}	TXC pulse width HIGH		14		ns	
t_{TPWL}	TXC pulse width LOW		14		ns	
t_{RPWH}	RXC pulse width HIGH		14		ns	
t_{RPWL}	RXC pulse width LOW		14		ns	
t_{TPS}	Setup time, TSM 0-4 data valid to TXC rising edge (1.4V point)		13			ns
t_{TPH}	Hold time, TSM 0-4 data valid after TXC rising edge (1.4V point)		3			ns
t_{RCS}	Time that RSM0-4 data are valid before RXC falling edge (1.4V point)		10			ns
t_{RCH}	Time that RSM0-4 data are valid after RXC falling edge (1.4V point)		10			ns
t_{RPCR}	RXC 10%-90% rise time				6	ns
t_{RPCF}	RXC 90%-10% fall time				6	ns

Note 1. Limits are guaranteed by 100% testing, sampling, or correlation with worst case test conditions.

Note 2. Output current amplitude is $I_{OUT} = 207V/RTSET$.

Note 3. Using the test load shown in Figure 1, transmitting "H" symbols.

FUNCTIONAL DESCRIPTION

TRANSMIT SECTION

The ML6695 transmit section accepts parallel NRZ data nibbles, creates a serial NRZI data stream using the internal 125MHz clock multiplier, and provides an open-collector output IOOUT to directly drive an LED. IOOUT must be connected to V_{CC} through a 15Ω resistor. The internal clock multiplier accepts an external 25MHz clock input.

The LED driver at IOOUT is a current mode switch which develops the output light by sinking current through the network LED into IOOUT. RTSET'S value determines the output current:

$$RTSET = \left(\frac{1.25V}{IOOUT} \right) \times 140\Omega \quad (1)$$

where IOOUT is the desired output current.

RECEIVE SECTION

The ML6695 receive section includes a fiber optic quantizer and a 125MHz receive clock recovery circuit. The quantizer is a wide-bandwidth limiting amplifier with

DC offset correction. The quantizer output drives a data comparator with a controlled slicing threshold. The comparator provides a large-amplitude receive signal. The clock recovery circuit extracts 125MHz receive clock from the large-amplitude signal, and provides the clock for the parallel data output registers. Received NRZ data nibbles appear at the RSM outputs synchronously with RXC falling edges. Received signals exceeding the preset signal detect amplitude threshold for more than 5μs cause the SDO output to go high. Received signals that fall below the preset threshold for more than 5μs cause SDO to go low.

OTHER MODES

The ML6695 will enter a power down mode when the PWRDN pin is tied low. In this state the ML6695 powers down to a low-current (less than 20mA), inoperative state. Driving it high enables normal operation of the ML6695.

Loopback mode is entered when the $\overline{LPBK}$ is tied to ground. In this mode, the data at TSM0-4 are serialized, then sent to the quantizer, followed by the receive PLL for clock recovery, and finally to the RSM0-4 outputs. Tying LPBK to V_{CC} places the ML6695 in its normal mode of operation.

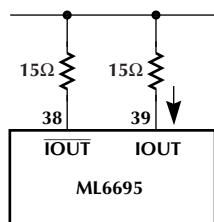
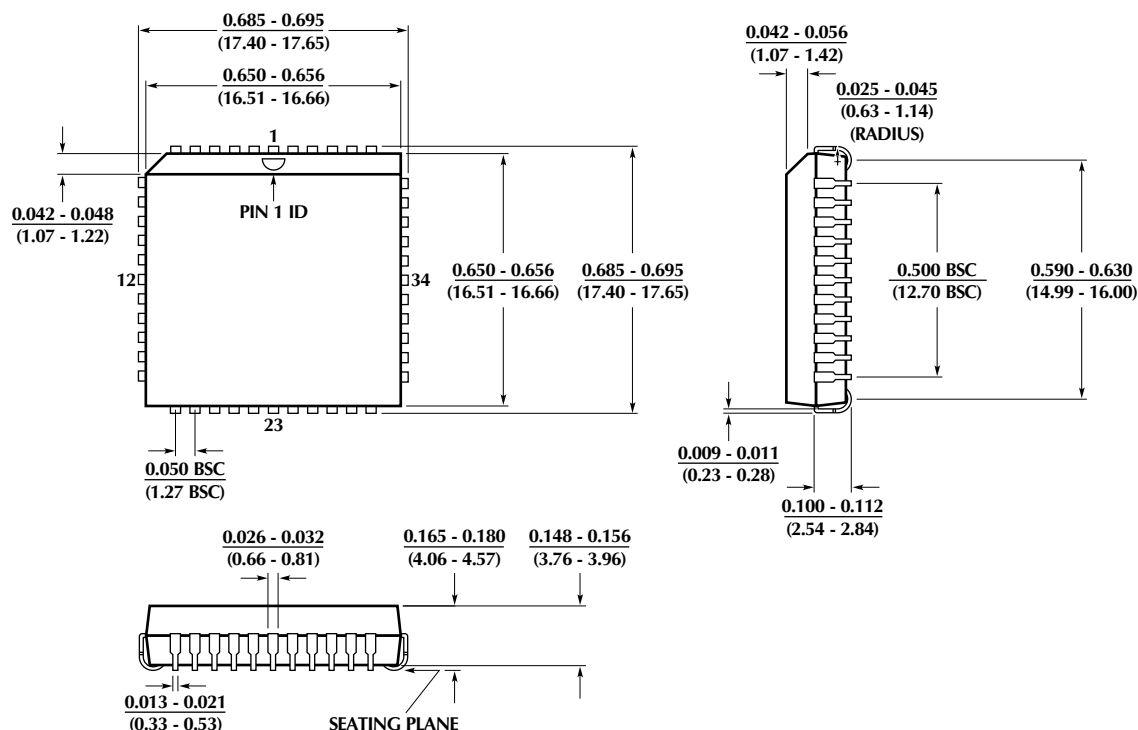


Figure 1. Test Load

ML6695

PHYSICAL DIMENSIONS inches (millimeters)

Package: Q44
44-Pin PLCC



ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML6695CQ	0°C to 70°C	44-Pin PLCC (Q44)

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Products described herein may be covered by one or more of the following U.S. patents: 4,897,611; 4,964,026; 5,027,116; 5,281,862; 5,283,483; 5,418,502; 5,508,570; 5,510,727; 5,523,940; 5,546,017; 5,559,470; 5,565,761; 5,592,128; 5,594,376; 5,652,479; 5,661,427; 5,663,874; 5,672,959; 5,689,167; 5,714,897; 5,717,798; 5,742,151; 5,747,977; 5,754,012; 5,757,174; 5,767,653; 5,777,514; 5,793,168; 5,798,635; 5,804,950; 5,808,455; 5,811,999; 5,818,207; 5,818,669; 5,825,165; 5,825,223; 5,838,723; 5,844,378; 5,844,941. Japan: 2,598,946; 2,619,299; 2,704,176; 2,821,714. Other patents are pending.

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