CY7C1352F

4-Mbit (256Kx18) Pipelined SRAM with NoBL™ Architecture

Features

- Pin compatible and functionally equivalent to ZBT™ devices
- Internally self-timed output buffer control to eliminate the need to use OE
- Byte Write capability
- 256K x 18 common I/O architecture
- Single 3.3V power supply
- 2.5V / 3.3V I/O Operation
- Fast clock-to-output times
  - — 2.6 ns (for 250-MHz device)
  - — 2.6 ns (for 225-MHz device)
  - — 2.8 ns (for 200-MHz device)
  - — 3.5 ns (for 166-MHz device)
  - — 4.0 ns (for 133-MHz device)
  - — 4.5 ns (for 100-MHz device)
- Clock Enable (CEN) pin to suspend operation
- Synchronous self-timed writes
- Asynchronous output enable (OE)
- JEDEC-standard 100 TQFP package
- Burst Capability—linear or interleaved burst order
- “ZZ” Sleep Mode Option and Stop Clock option

Functional Description[1]

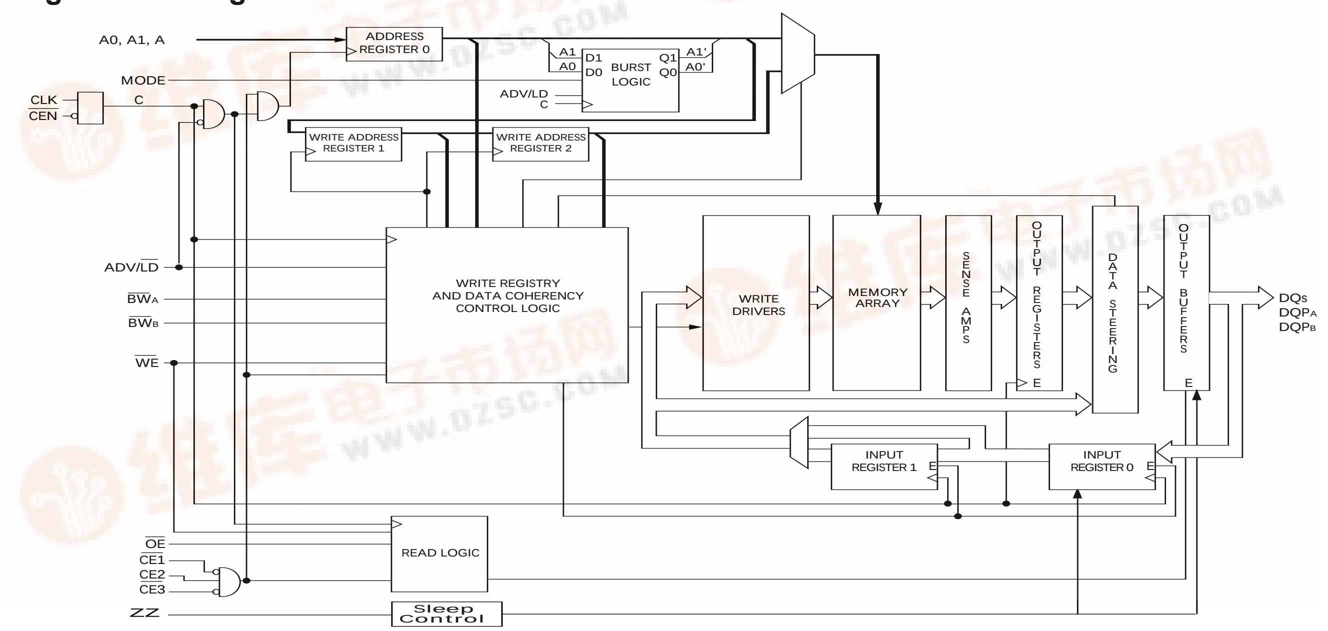
The CY7C1352F is a 3.3V, 256K x 18 synchronous-pipelined Burst SRAM designed specifically to support unlimited true back-to-back Read/Write operations without the insertion of wait states. The CY7C1352F is equipped with the advanced No Bus Latency™ (NoBL™) logic required to enable consecutive Read/Write operations with data being transferred on every clock cycle. This feature dramatically improves the throughput of the SRAM, especially in systems that require frequent Write/Read transitions.

All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock. The clock input is qualified by the Clock Enable (CEN) signal, which, when deasserted, suspends operation and extends the previous clock cycle. Maximum access delay from the clock rise is 2.8 ns (200-MHz device)

Write operations are controlled by the two Byte Write Select ($BW_{[A:B]}$) and a Write Enable (WE) input. All writes are conducted with on-chip synchronous self-timed write circuitry.

Three synchronous Chip Enables (CE_1, CE_2, CE_3) and an asynchronous Output Enable (OE) provide for easy bank selection and output three-state control. In order to avoid bus contention, the output drivers are synchronously three-stated during the data portion of a write sequence.

Logic Block Diagram



Note:
1. For best practices recommendations, please refer to the Cypress application note *System Design Guidelines* on www.cypress.com.

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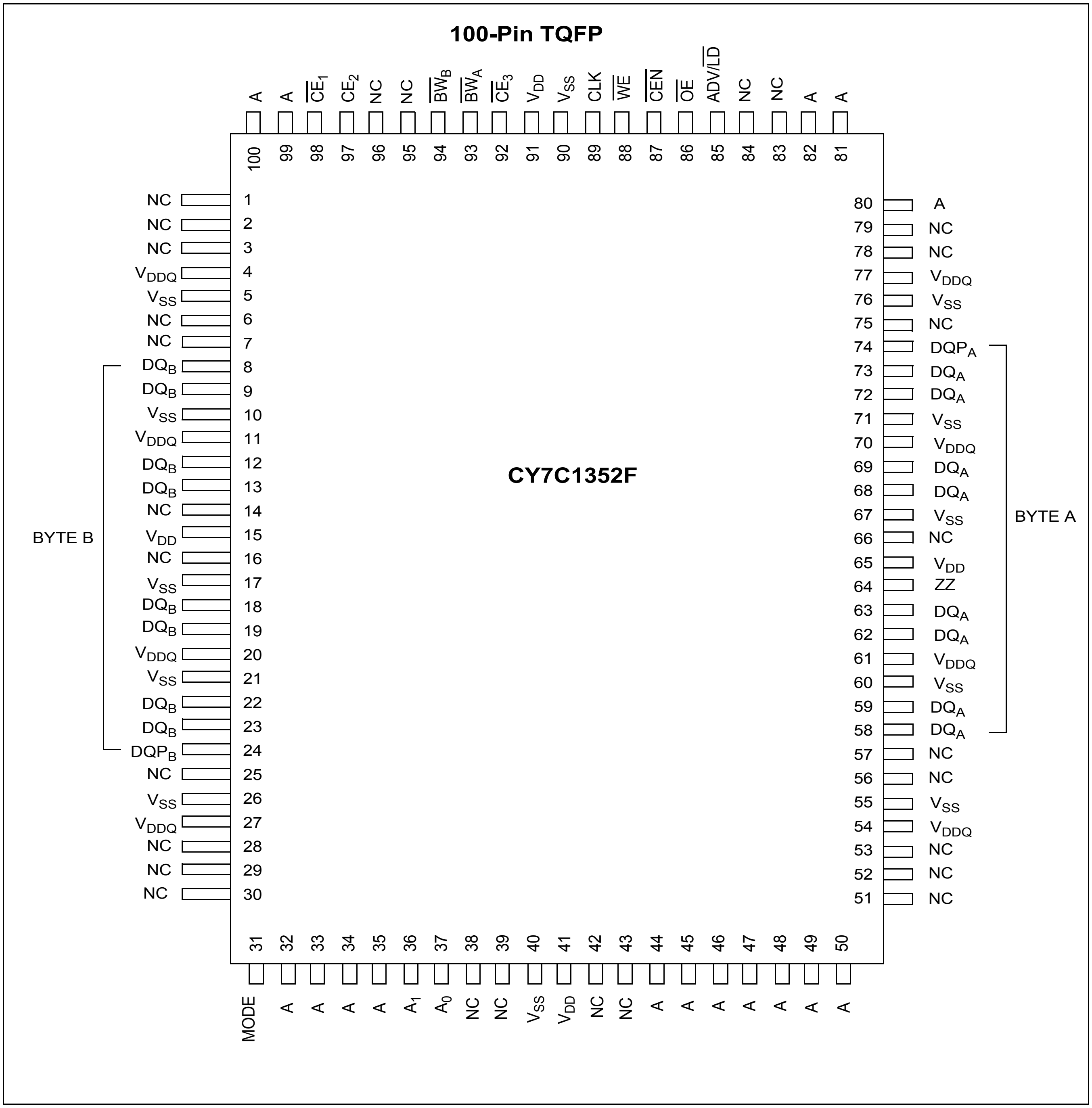
Selection Guide

	250 MHz	225 MHz	200 MHz	166 MHz	133 MHz	100 MHz	Unit
Maximum Access Time	2.6	2.6	2.8	3.5	4.0	4.5	ns
Maximum Operating Current	325	290	265	240	225	205	mA
Maximum CMOS Standby Current	40	40	40	40	40	40	mA

Shaded area contains advance information. Please contact your local Cypress sales representative for availability of these parts.

Pin Configuration



Pin Definitions

Name	TQFP	I/O	Description
A0, A1, A	37,36,32, 33,34,35, 44,45,46, 47,48,49, 50,80,81, 82,99,100	Input-Synchronous	**Address Inputs used to select one of the 256K address locations**. Sampled at the rising edge of the CLK. $A_{[1:0]}$ are fed to the two-bit burst counter.
$\overline{BW}_{[A:B]}$	93,94	Input-Synchronous	**Byte Write Inputs, active LOW**. Qualified with $\overline{WE}$ to conduct writes to the SRAM. Sampled on the rising edge of CLK.
$\overline{WE}$	88	Input-Synchronous	**Write Enable Input, active LOW**. Sampled on the rising edge of CLK if $\overline{CEN}$ is active LOW. This signal must be asserted LOW to initiate a write sequence.
ADV/$\overline{LD}$	85	Input-Synchronous	**Advance/Load Input**. Used to advance the on-chip address counter or load a new address. When HIGH (and $\overline{CEN}$ is asserted LOW) the internal burst counter is advanced. When LOW, a new address can be loaded into the device for an access. After being deselected, ADV/$\overline{LD}$ should be driven LOW in order to load a new address.
CLK	89	Input-Clock	**Clock Input**. Used to capture all synchronous inputs to the device. CLK is qualified with $\overline{CEN}$. CLK is only recognized if $\overline{CEN}$ is active LOW.
$\overline{CE}_1$	98	Input-Synchronous	**Chip Enable 1 Input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with CE_2 and $\overline{CE}_3$ to select/deselect the device.
CE_2	97	Input-Synchronous	**Chip Enable 2 Input, active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_3$ to select/deselect the device.
$\overline{CE}_3$	92	Input-Synchronous	**Chip Enable 3 Input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and CE_2 to select/deselect the device.
$\overline{OE}$	86	Input-Asynchronous	**Output Enable, asynchronous input, active LOW**. Combined with the synchronous logic block inside the device to control the direction of the I/O pins. When LOW, the DQ pins are allowed to behave as outputs. When deasserted HIGH, DQ pins are three-stated, and act as input data pins. $\overline{OE}$ is masked during the data portion of a write sequence, during the first clock when emerging from a deselected state, when the device has been deselected.
$\overline{CEN}$	87	Input-Synchronous	**Clock Enable Input, active LOW**. When asserted LOW the Clock signal is recognized by the SRAM. When deasserted HIGH the Clock signal is masked. Since deasserting $\overline{CEN}$ does not deselect the device, $\overline{CEN}$ can be used to extend the previous cycle when required.
ZZ	64	Input-Asynchronous	ZZ “sleep” Input. This active HIGH input places the device in a non-time-critical “sleep” condition with data integrity preserved. For normal operation, this pin has to be LOW or left floating. ZZ pin has an internal pull-down.
DQs	58,59,62, 63,68,69, 72,73, 8,9,12,13, 18,19,22, 23	I/O-Synchronous	**Bidirectional Data I/O Lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the address during the clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$ and the internal control logic. When $\overline{OE}$ is asserted LOW, the pins can behave as outputs. When HIGH, DQ_s and $DQP_{[A:B]}$ are placed in a three-state condition. The outputs are automatically three-stated during the data portion of a write sequence, during the first clock when emerging from a deselected state, and when the device is deselected, regardless of the state of $\overline{OE}$.
$DQP_{[A:B]}$	74,24	I/O-Synchronous	**Bidirectional Data Parity I/O Lines**. Functionally, these signals are identical to DQ_s. During write sequences, $DQP_{[A:B]}$ is controlled by $\overline{BW}_{[A:B]}$ correspondingly.
MODE	31	Input Strap pin	Mode Input. Selects the burst order of the device. When tied to Gnd selects linear burst sequence. When tied to V_{DD} or left floating selects interleaved burst sequence.
V_{DD}	15,41,65, 91	Power Supply	**Power supply inputs to the core of the device**.
V_{DDQ}	4,11,20,27,54,61,70, 77	I/O Power Supply	**Power supply for the I/O circuitry**.

Pin Definitions (continued)

Name	TQFP	I/O	Description
V_{SS}	5,10,17,21,26,40,55, 60,67,71, 76,90	Ground	**Ground for the device**.
NC	1,2,3,6,7, 14,16,25, 28,29,30, 38,39,42, 43,51,52, 53,56,57, 66,75,78, 79,83,84, 95,96		**No Connects**. Not internally connected to the die.

Functional Overview

The CY7C1352F is a synchronous-pipelined Burst SRAM designed specifically to eliminate wait states during Write/Read transitions. All synchronous inputs pass through input registers controlled by the rising edge of the clock. The clock signal is qualified with the Clock Enable input signal ($\overline{CEN}$). If $\overline{CEN}$ is HIGH, the clock signal is not recognized and all internal states are maintained. All synchronous operations are qualified with $\overline{CEN}$. All data outputs pass through output registers controlled by the rising edge of the clock. Maximum access delay from the clock rise (t_{CO}) is 2.8 ns (200-MHz device).

Accesses can be initiated by asserting all three Chip Enables ($\overline{CE}_1$, CE_2, $\overline{CE}_3$) active at the rising edge of the clock. If Clock Enable ($\overline{CEN}$) is active LOW and ADV/$\overline{LD}$ is asserted LOW, the address presented to the device will be latched. The access can either be a read or write operation, depending on the status of the Write Enable ($\overline{WE}$). $\overline{BW}_{[A:B]}$ can be used to conduct byte write operations.

Write operations are qualified by the Write Enable ($\overline{WE}$). All writes are simplified with on-chip synchronous self-timed write circuitry.

Three synchronous Chip Enables ($\overline{CE}_1$, CE_2, $\overline{CE}_3$) and an asynchronous Output Enable ($\overline{OE}$) simplify depth expansion. All operations (Reads, Writes, and Deselects) are pipelined. ADV/$\overline{LD}$ should be driven LOW once the device has been deselected in order to load a new address for the next operation.

Single Read Accesses

A read access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CEN}$ is asserted LOW, (2) $\overline{CE}_1$, CE_2, and $\overline{CE}_3$ are ALL asserted active, (3) the Write Enable input signal $\overline{WE}$ is deasserted HIGH, and (4) ADV/$\overline{LD}$ is asserted LOW. The address presented to the address inputs is latched into the Address Register and presented to the memory core and control logic. The control logic determines that a read access is in progress and allows the requested data to propagate to the input of the output register. At the rising edge of the next clock the requested data is allowed to propagate through the output register and onto the data bus, provided $\overline{OE}$ is active LOW. After the first clock of the read access the output buffers are controlled by $\overline{OE}$ and the internal control logic. $\overline{OE}$ must be driven LOW in order for the device to drive out the requested data. During the second clock, a subsequent operation (Read/Write/Deselect) can be initiated. Deselecting the device is also pipelined. Therefore, when the SRAM is deselected at clock rise by one of the chip enable signals, its output will three-state following the next clock rise.

Burst Read Accesses

The CY7C1352F has an on-chip burst counter that allows the user the ability to supply a single address and conduct up to four Reads without reasserting the address inputs. ADV/$\overline{LD}$ must be driven LOW in order to load a new address into the SRAM, as described in the Single Read Access section above. The sequence of the burst counter is determined by the MODE input signal. A LOW input on MODE selects a linear burst mode, a HIGH selects an interleaved burst sequence. Both burst counters use A0 and A1 in the burst sequence, and will wrap-around when incremented sufficiently. A HIGH input on ADV/$\overline{LD}$ will increment the internal burst counter regardless of the state of chip enables inputs or $\overline{WE}$. $\overline{WE}$ is latched at the beginning of a burst cycle. Therefore, the type of access (Read or Write) is maintained throughout the burst sequence.

Single Write Accesses

Write accesses are initiated when the following conditions are satisfied at clock rise: (1) $\overline{CEN}$ is asserted LOW, (2) $\overline{CE}_1$, CE_2, and $\overline{CE}_3$ are ALL asserted active, and (3) the write signal $\overline{WE}$ is asserted LOW. The address presented to the address inputs is loaded into the Address Register. The write signals are latched into the Control Logic block.

On the subsequent clock rise the data lines are automatically three-stated regardless of the state of the $\overline{OE}$ input signal. This allows the external logic to present the data on DQs and $DQP_{[A:B]}$. In addition, the address for the subsequent access (Read/Write/Deselect) is latched into the Address Register (provided the appropriate control signals are asserted).

On the next clock rise the data presented to DQs and $DQP_{[A:B]}$ (or a subset for byte write operations, see Write Cycle Description table for details) inputs is latched into the device and the write is complete.

The data written during the Write operation is controlled by $\overline{BW}_{[A:B]}$ signals. The CY7C1352F provides byte write capability that is described in the Write Cycle Description table. Asserting the Write Enable input ($\overline{WE}$) with the selected Byte Write Select ($\overline{BW}_{[A:B]}$) input will selectively write to only the desired bytes. Bytes not selected during a byte write operation will remain unaltered. A synchronous self-timed write mechanism has been provided to simplify the write operations. Byte write capability has been included in order to greatly simplify Read/Modify/Write sequences, which can be reduced to simple byte write operations.

Because the CY7C1352F is a common I/O device, data should not be driven into the device while the outputs are active. The Output Enable ($\overline{OE}$) can be deasserted HIGH before presenting data to the DQs and $DQP_{[A:B]}$ inputs. Doing so will three-state the output drivers. As a safety precaution, DQs and $DQP_{[A:B]}$ are automatically three-stated during the data portion of a write cycle, regardless of the state of $\overline{OE}$.

Burst Write Accesses

The CY7C1352F has an on-chip burst counter that allows the user the ability to supply a single address and conduct up to four Write operations without reasserting the address inputs. ADV/$\overline{LD}$ must be driven LOW in order to load the initial address, as described in the Single Write Access section above. When ADV/$\overline{LD}$ is driven HIGH on the subsequent clock rise, the chip enables ($\overline{CE}_1$, CE_2, and $\overline{CE}_3$) and $\overline{WE}$ inputs are ignored and the burst counter is incremented. The correct $\overline{BW}_{[A:B]}$ inputs must be driven in each cycle of the burst write in order to write the correct bytes of data.

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation "sleep" mode. Two clock cycles are required to enter into or exit from this "sleep" mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the "sleep" mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the "sleep" mode. $\overline{CE}_1$, CE_2, and $\overline{CE}_3$, must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

Interleaved Burst Address Table (MODE = Floating or V_{DD})

First Address A1, A0	Second Address A1, A0	Third Address A1, A0	Fourth Address A1, A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Address Table (MODE = GND)

First Address A1, A0	Second Address A1, A0	Third Address A1, A0	Fourth Address A1, A0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

Truth Table [2, 3, 4, 5, 6, 7, 8]

Operation	Address Used	$\overline{CE}$	ZZ	ADV/$\overline{LD}$	$\overline{WE}$	$\overline{BW}_x$	$\overline{OE}$	$\overline{CEN}$	CLK	DQ
Deselect Cycle	None	H	L	L	X	X	X	L	L-H	three-state
Continue Deselect Cycle	None	X	L	H	X	X	X	L	L-H	three-state
Read Cycle (Begin Burst)	External	L	L	L	H	X	L	L	L-H	Data Out (Q)
Read Cycle (Continue Burst)	Next	X	L	H	X	X	L	L	L-H	Data Out (Q)
NOP/Dummy Read (Begin Burst)	External	L	L	L	H	X	H	L	L-H	three-state
Dummy Read (Continue Burst)	Next	X	L	H	X	X	H	L	L-H	three-state
Write Cycle (Begin Burst)	External	L	L	L	L	L	X	L	L-H	Data In (D)
Write Cycle (Continue Burst)	Next	X	L	H	X	L	X	L	L-H	Data In (D)
NOP/WRITE ABORT (Begin Burst)	None	L	L	L	L	H	X	L	L-H	three-state

Notes:
2. X="Don't Care." H= Logic HIGH, L =Logic LOW. $\overline{CE}$ stands for ALL Chip Enables active. $\overline{BW}_X$ = 0 signifies at least one Byte Write Select is active, $\overline{BW}_X$ = Valid signifies that the desired byte write selects are asserted, see Write Cycle Description table for details.
3. Write is defined by $\overline{BW}_{[A:B]}$, and $\overline{WE}$. See Write Cycle Descriptions table.
4. When a write cycle is detected, all I/Os are three-stated, even during byte writes.
5. The DQ and DQP pins are controlled by the current cycle and the $\overline{OE}$ signal. $\overline{OE}$ is asynchronous and is not sampled with the clock.
6. $\overline{CEN}$ = H, inserts wait states.
7. Device will power-up deselected and the I/Os in a three-state condition, regardless of $\overline{OE}$.
8. $\overline{OE}$ is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle DQs and $DQP_{[A:B]}$ = Three-state when $\overline{OE}$ is inactive or when the device is deselected, and DQs and $DQP_{[A:B]}$ = data when $\overline{OE}$ is active.

Truth Table [2, 3, 4, 5, 6, 7, 8] (continued)

Operation	Address Used	$\overline{CE}$	ZZ	ADV/$\overline{LD}$	$\overline{WE}$	$\overline{BW}_x$	$\overline{OE}$	$\overline{CEN}$	CLK	DQ
WRITE ABORT (Continue Burst)	Next	X	L	H	X	H	X	L	L-H	three-state
IGNORE CLOCK EDGE (Stall)	Current	X	L	X	X	X	X	H	L-H	–
SNOOZE MODE	None	X	H	X	X	X	X	X	X	three-state

Truth Table for Read/Write [2, 3]

Function	$\overline{WE}$	$\overline{BW}_B$	$\overline{BW}_A$
Read	H	X	X
Write – No bytes written	L	H	H
Write Byte A – (DQ_A and DQP_A)	L	H	L
Write Byte B – (DQ_B and DQP_B)	L	L	H
Write All Bytes	L	L	L

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min.	Max.	Unit
I_{DDZZ}	Snooze mode standby current	$ZZ \geq V_{DD} - 0.2V$		40	mA
t_{ZZS}	Device operation to ZZ	$ZZ \geq V_{DD} - 0.2V$		$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	$ZZ \leq 0.2V$	$2t_{CYC}$		ns
t_{ZZI}	ZZ active to snooze current	This parameter is sampled		$2t_{CYC}$	ns
t_{RZZI}	ZZ inactive to exit snooze current	This parameter is sampled	0		ns

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... –65°C to +150°C

Ambient Temperature with Power Applied... –55°C to +125°C

Supply Voltage on V_{DD} Relative to GND.........–0.5V to +4.6V

DC Voltage Applied to Outputs in three-state ....–0.5V to V_{DDQ} + 0.5V

DC Input Voltage .... –0.5V to V_{DD} + 0.5V

Current into Outputs (LOW)... 20 mA

Static Discharge Voltage.. > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current.. > 200 mA

Operating Range

Range	Ambient Temperature (T_A)	V_{DD}	V_{DDQ}
Com'l	0°C to +70°C	3.3V – 5%/+10%	2.5V –5% to V_{DD}
Ind'l	–40°C to +85°C		

Electrical Characteristics Over the Operating Range[9, 10]

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{DD}	Power Supply Voltage			3.135	3.6	V
V_{DDQ}	I/O Supply Voltage			2.375	V_{DD}	V
V_{OH}	Output HIGH Voltage	V_{DDQ} = 3.3V, V_{DD} = Min., I_{OH} = –4.0 mA		2.4		V
		V_{DDQ} = 2.5V, V_{DD} = Min., I_{OH} = –2.0 mA		2.0		V
V_{OL}	Output LOW Voltage	V_{DDQ} = 3.3V, V_{DD} = Min., I_{OL} = 8.0 mA			0.4	V
		V_{DDQ} = 2.5V, V_{DD} = Min., I_{OL} = 2.0 mA			0.4	V
V_{IH}	Input HIGH Voltage[9]	V_{DDQ} = 3.3V		2.0	V_{DD} + 0.3V	V
		V_{DDQ} = 2.5V		1.7	V_{DD} + 0.3V	V
V_{IL}	Input LOW Voltage[9]	V_{DDQ} = 3.3V		–0.3	0.8	V
		V_{DDQ} = 2.5V		–0.3	0.7	V
I_X	Input Load Current except ZZ and MODE	GND ≤ V_I ≤ V_{DDQ}		–5	5	µA
	Input Current of MODE	Input = V_{SS}		–30		µA
		Input = V_{DD}			5	µA
	Input Current of ZZ	Input = V_{SS}		–5		µA
		Input = V_{DD}			30	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ $V_{DDQ,}$ Output Disabled		–5	5	µA
I_{DD}	V_{DD} Operating Supply Current	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{CYC}$	4-ns cycle, 250 MHz		325	mA
			4.4-ns cycle, 225 MHz		290	mA
			5-ns cycle, 200 MHz		265	mA
			6-ns cycle, 166 MHz		240	mA
			7.5-ns cycle, 133 MHz		225	mA
			10-ns cycle, 100MHz		205	mA

Electrical Characteristics Over the Operating Range[9, 10] (continued)

Parameter	Description	Test Conditions		Min.	Max.	Unit
I_{SB1}	Automatic CE Power-Down Current—TTL Inputs	V_{DD} = Max, Device Deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ f = f_{MAX} = $1/t_{CYC}$	4-ns cycle, 250 MHz		120	mA
			4.4-ns cycle, 225 MHz		115	mA
			5-ns cycle, 200 MHz		110	mA
			6-ns cycle, 166 MHz		100	mA
			7.5-ns cycle, 133 MHz		90	mA
			10-ns cycle, 100 MHz		80	mA
I_{SB2}	Automatic CE Power-down Current—CMOS Inputs	V_{DD} = Max, Device Deselected, $V_{IN} \leq 0.3V$ or $V_{IN} \geq V_{DDQ} - 0.3V$, f = 0	All speeds		40	mA
I_{SB3}	Automatic CE Power-down Current—CMOS Inputs	V_{DD} = Max, Device Deselected, or $V_{IN} \leq 0.3V$ or $V_{IN} \geq V_{DDQ} - 0.3V$ f = f_{MAX} = $1/t_{CYC}$	4-ns cycle, 250 MHz		105	mA
			4.4-ns cycle, 225 MHz		100	mA
			5-ns cycle, 200 MHz		95	mA
			6-ns cycle, 166 MHz		85	mA
			7.5-ns cycle, 133 MHz		75	mA
			10-ns cycle, 100 MHz		65	mA
I_{SB4}	Automatic CE Power-down Current—TTL Inputs	V_{DD} = Max, Device Deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = 0	All speeds		45	mA

Shaded areas contain advance information.

Thermal Resistance[11]

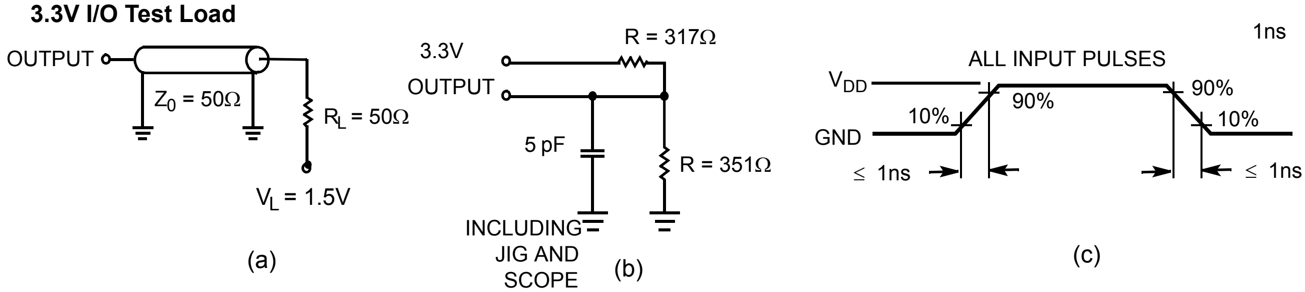
Parameter	Description	Test Conditions	TQFP Package	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	41.83	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		9.99	°C/W

Capacitance[11]

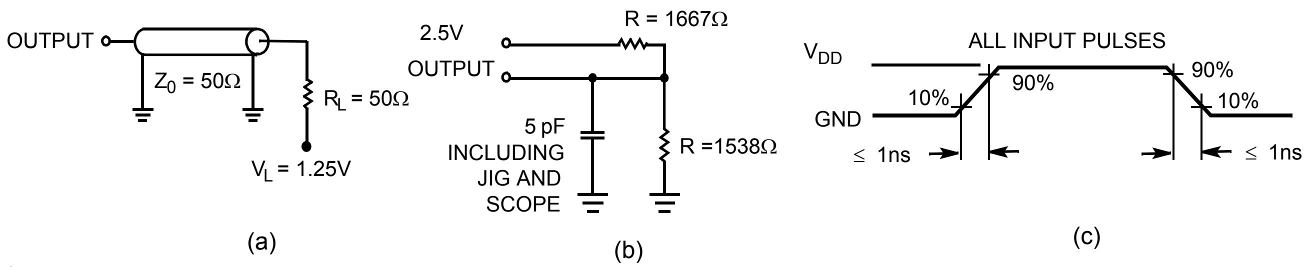
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V, V_{DDQ} = 3.3V	5	pF
C_{CLK}	Clock Input Capacitance		5	pF
$C_{I/O}$	Input/Output Capacitance		5	pF

AC Test Loads and Waveforms

3.3V I/O Test Load



2.5V I/O Test Load



Notes:

9. Overshoot: $V_{IH}(AC) < V_{DD}$ +1.5V (Pulse width less than $t_{CYC}/2$), undershoot: $V_{IL}(AC) > -2V$ (Pulse width less than $t_{CYC}/2$).
10. $T_{Power\text{-}up}$: Assumes a linear ramp from 0V to V_{DD} (min.) within 200ms. During this time $V_{IH} < V_{DD}$ and $V_{DDQ} < V_{DD}$.
11. Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics Over the Operating Range[12, 13, 14, 15, 16, 17]

Parameter	Description	250 MHz		225 MHz		200 MHz		166 MHz		133 MHz		100 MHz		Unit
		Min.	Max	Min.	Max	Min.	Max	Min.	Max	Min.	Max	Min.	Max	
t_{POWER}	V_{DD} (typical) to the first Access[12]	1		1		1		1		1		1		ms
Clock														
t_{CYC}	Clock Cycle Time	4.0		4.4		5.0		6.0		7.5		10		ns
t_{CH}	Clock HIGH	1.7		2.0		2.0		2.5		3.0		3.5		ns
t_{CL}	Clock LOW	1.7		2.0		2.0		2.5		3.0		3.5		ns
Output Times														
t_{CO}	Data Output Valid After CLK Rise		2.6		2.6		2.8		3.5		4.0		4.5	ns
t_{DOH}	Data Output Hold After CLK Rise	1.0		1.0		1.0		2.0		2.0		2.0		ns
t_{CLZ}	Clock to Low-Z[13, 14, 15]	0		0		0		0		0		0		ns
t_{CHZ}	Clock to High-Z[13, 14, 15]		2.6		2.6		2.8		3.5		4.0		4.5	ns
t_{OEV}	$\overline{OE}$ LOW to Output Valid		2.6		2.6		2.8		3.5		4.0		4.5	ns
t_{OELZ}	$\overline{OE}$ LOW to Output Low-Z[13, 14, 15]	0		0		0		0		0		0		ns
t_{OEHZ}	$\overline{OE}$ HIGH to Output High-Z[13, 14, 15]		2.6		2.6		2.8		3.5		4.0		4.5	ns
Set-up Times														
t_{AS}	Address Set-up Before CLK Rise	0.8		1.2		1.2		1.5		1.5		1.5		ns

Shaded areas contain advance information.

Notes:

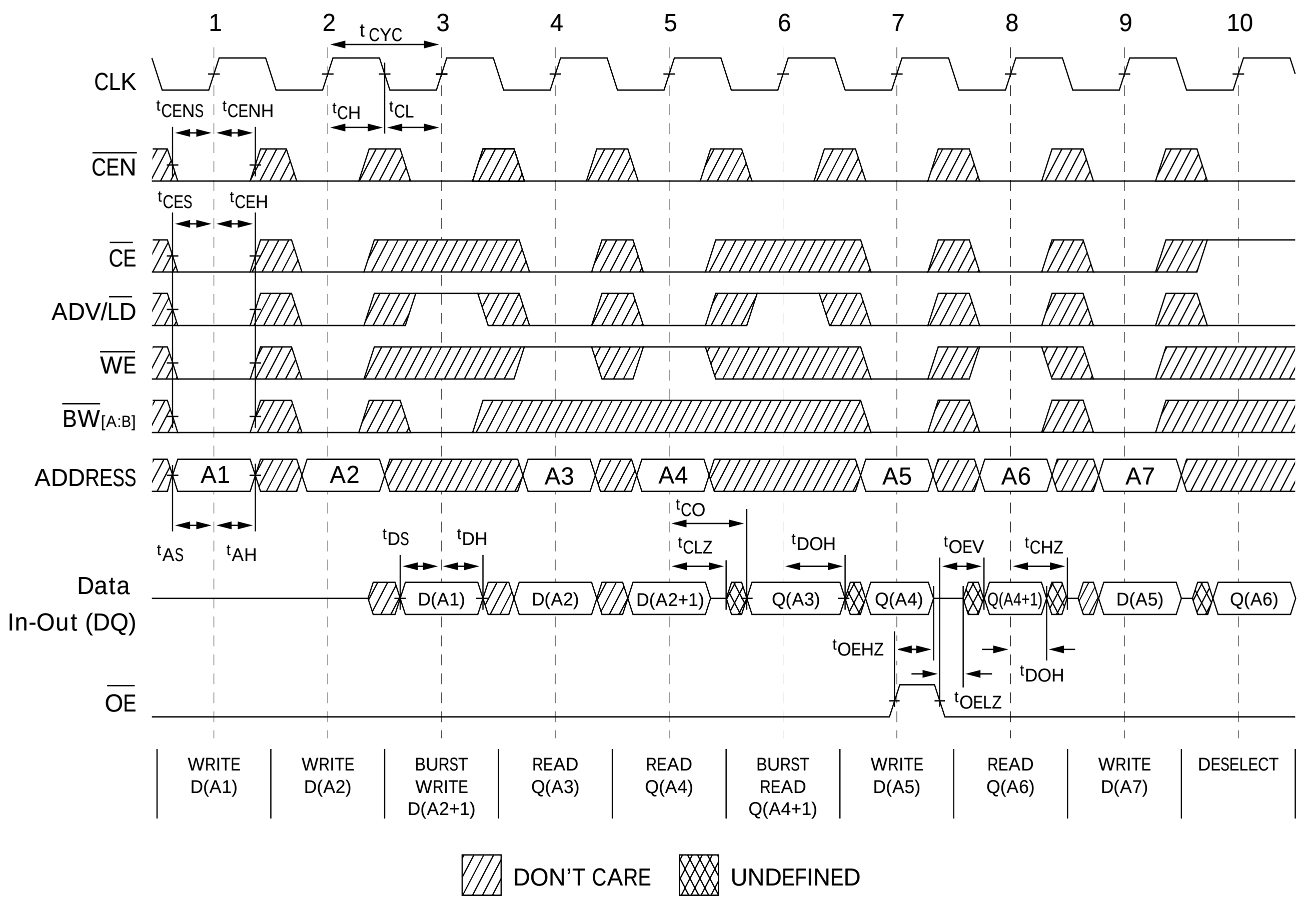
12. This part has a voltage regulator internally; tpower is the time that the power needs to be supplied above V_{DD} minimum initially before a read or write operation can be initiated.
13. t_{CHZ}, t_{CLZ}, t_{OELZ}, and t_{OEHZ} are specified with AC test conditions shown in part (b) of AC Test Loads. Transition is measured ± 200 mV from steady-state voltage.
14. At any given voltage and temperature, t_{OEHZ} is less than t_{OELZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve Three-state prior to Low-Z under the same system conditions.
15. This parameter is sampled and not 100% tested.
16. Timing reference level is 1.5V when V_{DDQ} = 3.3V and is 1.25V when V_{DDQ} = 2.5V.
17. Test conditions shown in (a) of AC Test Loads unless otherwise noted.

Switching Characteristics Over the Operating Range[12, 13, 14, 15, 16, 17] (continued)

Parameter	Description	250 MHz		225 MHz		200 MHz		166 MHz		133 MHz		100 MHz		Unit
		Min.	Max	Min.	Max	Min.	Max	Min.	Max	Min.	Max	Min.	Max	
t_{ALS}	ADV/$\overline{LD}$ Set-up Before CLK Rise	0.8		1.2		1.2		1.5		1.5		1.5		ns
t_{WES}	$\overline{GW}$, $\overline{BW}_{[A:B]}$ Set-Up Before CLK Rise	0.8		1.2		1.2		1.5		1.5		1.5		ns
t_{CENS}	$\overline{CEN}$ Set-up Before CLK Rise	0.8		1.2		1.2		1.5		1.5		1.5		ns
t_{DS}	Data Input Set-up Before CLK Rise	0.8		1.2		1.2		1.5		1.5		1.5		ns
t_{CES}	Chip Enable Set-Up Before CLK Rise	0.8		1.2		1.2		1.5		1.5		1.5		ns
Hold Times														
t_{AH}	Address Hold After CLK Rise	0.4		0.5		0.5		0.5		0.5		0.5		ns
t_{ALH}	ADV/$\overline{LD}$ Hold after CLK Rise	0.4		0.5		0.5		0.5		0.5		0.5		ns
t_{WEH}	$\overline{GW}$, $\overline{BW}_{[A:B]}$ Hold After CLK Rise	0.4		0.5		0.5		0.5		0.5		0.5		ns
t_{CENH}	$\overline{CEN}$ Hold After CLK Rise	0.4		0.5		0.5		0.5		0.5		0.5		ns
t_{DH}	Data Input Hold After CLK Rise	0.4		0.5		0.5		0.5		0.5		0.5		ns
t_{CEH}	Chip Enable Hold After CLK Rise	0.4		0.5		0.5		0.5		0.5		0.5		ns

Switching Waveforms

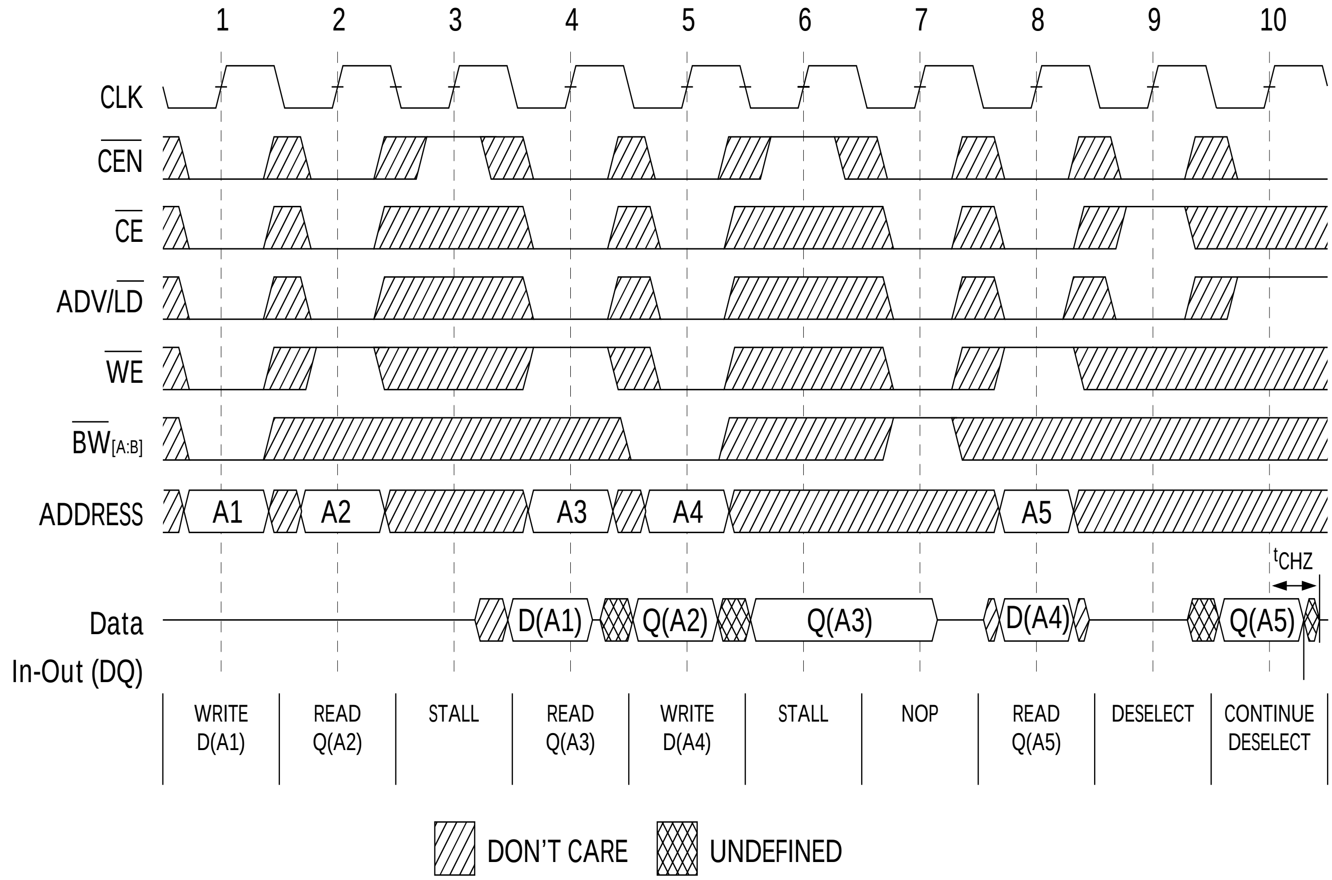
Read/Write Timing[18, 19, 20]



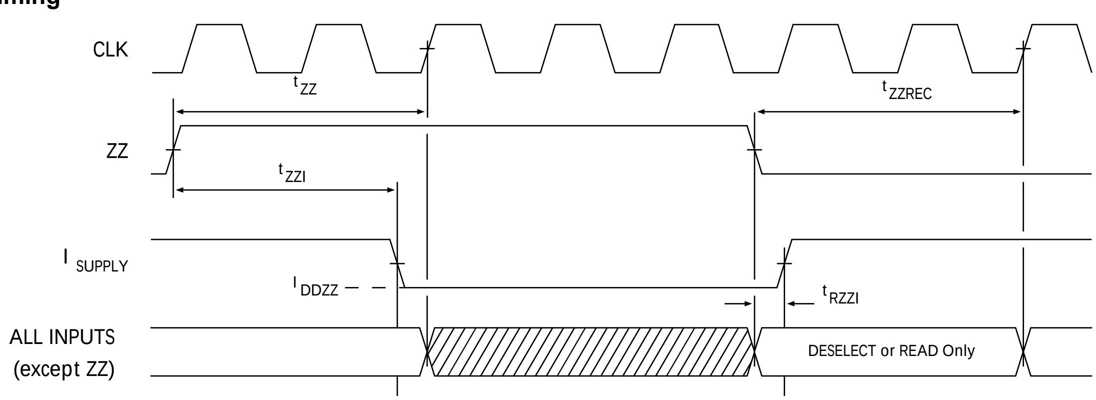
Note:
18. For this waveform $\overline{ZZ}$ is tied low.
19. When $\overline{CE}$ is LOW: $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH: $\overline{CE}_1$ is HIGH or CE_2 is LOW or $\overline{CE}_3$ is HIGH.
20. Order of the Burst sequence is determined by the status of the MODE (0= Linear, 1= Interleaved). Burst operations are optional.

Switching Waveforms (continued)

NOP, STALL, and DESELECT Cycles[18, 19, 21]



ZZ Mode Timing[22, 23]



Notes:

21. The IGNORE CLOCK EDGE or STALL cycle (Clock 3) illustrated $\overline{CEN}$ being used to create a pause. A write is not performed during this cycle.
22. Device must be deselected when entering ZZ mode. See cycle description table for all possible signal conditions to deselect the device.
23. DQs are in high-Z when exiting ZZ sleep mode.

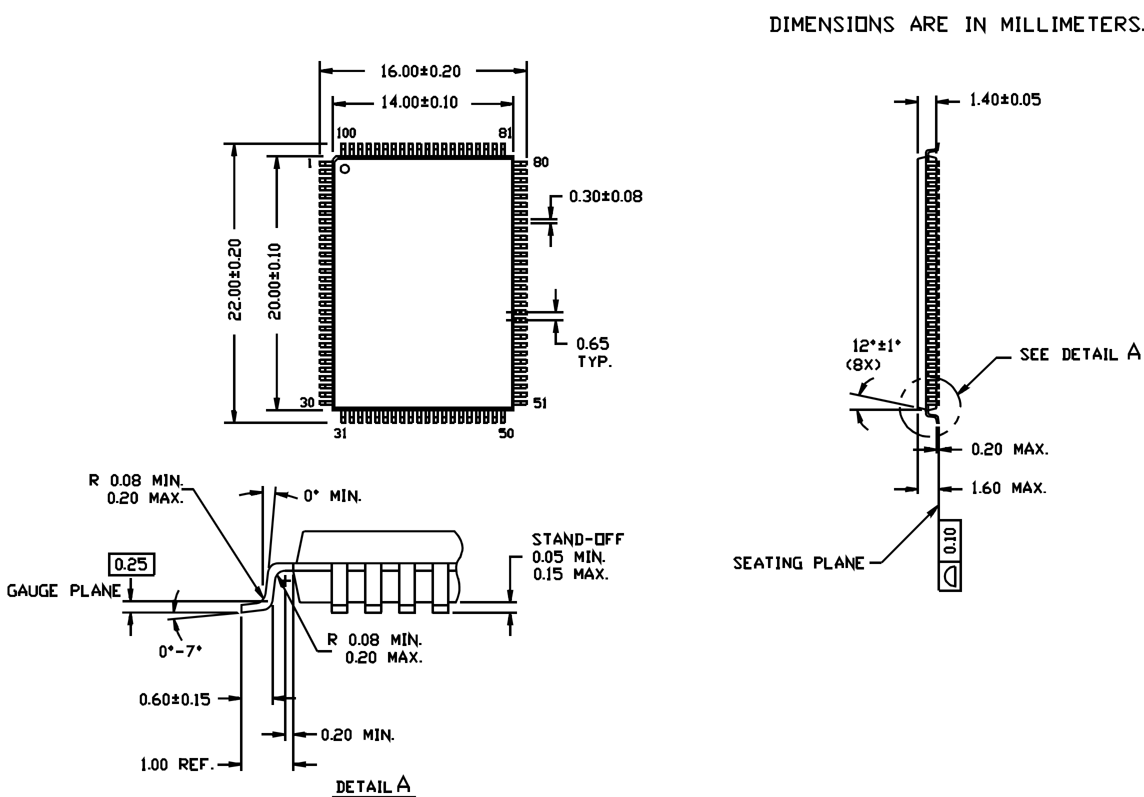
Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
250	CY7C1352F-250AC	A101	100-Lead Thin Quad Flat Pack(14 x 20 x 1.4mm)	Commercial
	CY7C1352F-250AI	A101	100-Lead Thin Quad Flat Pack(14 x 20 x 1.4mm)	Industrial
225	CY7C1352F-225AC	A101	100-Lead Thin Quad Flat Pack(14 x 20 x 1.4mm)	Commercial
	CY7C1352F-225AI	A101	100-Lead Thin Quad Flat Pack(14 x 20 x 1.4mm)	Industrial
200	CY7C1352F-200AC	A101	100-Lead Thin Quad Flat Pack(14 x 20 x 1.4mm)	Commercial
	CY7C1352F-200AI	A101	100-Lead Thin Quad Flat Pack(14 x 20 x 1.4mm)	Industrial
166	CY7C1352F-166AC	A101	100-Lead Thin Quad Flat Pack(14 x 20 x 1.4mm)	Commercial
	CY7C1352F-166AI	A101	100-Lead Thin Quad Flat Pack(14 x 20 x 1.4mm)	Industrial
133	CY7C1352F-133AC	A101	100-Lead Thin Quad Flat Pack(14 x 20 x 1.4mm)	Commercial
	CY7C1352F-133AI	A101	100-Lead Thin Quad Flat Pack(14 x 20 x 1.4mm)	Industrial
100	CY7C1352F-100AC	A101	100-Lead Thin Quad Flat Pack(14 x 20 x 1.4mm)	Commercial
	CY7C1352F-100AI	A101	100-Lead Thin Quad Flat Pack(14 x 20 x 1.4mm)	Industrial

Shaded areas contain advance information. Please contact your local cypress sales representative to order parts that are not listed in the ordering information table.

Package Diagram

100-Pin Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm) A101



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Document History Page

Document Title: CY7C1352F 4-Mbit (256Kx18) Pipelined SRAM with NoBL™ Architecture Document #: 38-05211 Rev. *C				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	119826	12/16/02	HGK	New Data Sheet
*A	123116	01/18/03	RBI	Added power-up requirements to AC test loads and waveforms information
*B	200662	See ECN	SWI	Final Data Sheet
*C	225487	See ECN	VBL	Update Ordering Info section: unshade active part numbers.