19-1433; Rev 1; 3/99

MAXIM

2.5Gbps, +3.3V Combined Transimpedance/Limiting Amplifier

General Description

The MAX3866 combined transimpedance preamplifier and limiting postamplifier is intended for application in SDH/SONET systems operating at 2.488Gbps. It operates from a single +3.3V or +5V supply and provides a differential output signal. The differential outputs are each 50Ω reverse terminated (100Ω differential termination) for low-noise and high-speed signal performance.

The small-signal bandwidth and noise performance is specified for a source capacitance of 0.5pF. When the MAX3866 is used with the PIN photodetector, sensitivities better than -22dBm can be achieved. The MAX3866 is equipped with a programmable TTL loss-of-power (LOP) output.

Applications

SDH/SONET Transmission Systems

PIN/Preamplifier Receivers

2.488Gbps ATM Receivers

Regenerators for SDH/SONET

Features

- **Input Sensitivities Better than -22dBm (7.8µAp-p)**
- **Overdrive Capability Better than +1.4dBm (2.5mAp-p)**
- **Single +3.3V or +5V Supply**
- **165mW Power Dissipation (at 3.3V)**
- **1.8GHz Analog Input Bandwidth**
- **Programmable Loss-of-Power Indicator**
- **100Ω Differential Output**

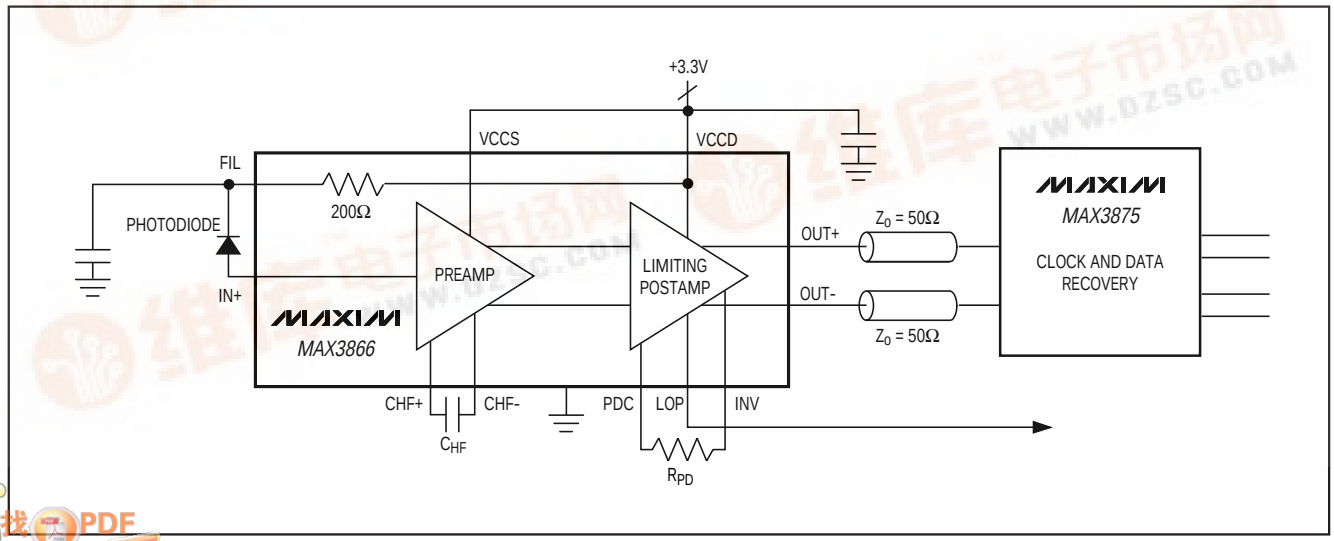
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX3866E/D	(see Note)	Dice

Note: *Dice are designed to operate over a -40°C to +120°C junction temperature (T_J) range, but are tested and guaranteed at T_A = +25°C.*

Pad Configuration appears at end of data sheet.

Typical Application Circuit



2.5Gbps, +3.3V Combined Transimpedance/Limiting Amplifier

ABSOLUTE MAXIMUM RATINGS

VCCD Voltage .....-0.5V to +7.0V
VCCS Voltage .....0 ≤ VCCS ≤ VCCD and if VCCD ≥ 3.13V then 3.13V ≤ VCCS ≤ VCCD
CHF+, CHF-, FIL, INV, LOP Voltage .....-0.5V to (VCCD + 0.5V)
IN-, IN+ Voltage.....-0.5V to +1.0V
CPD+, CPD- Voltage .....(VCCD - 1.6V) to (VCCD + 0.5V)
OUT+, OUT- Voltage .....(VCCD - 1.1V) to (VCCD + 0.5V)
IN Current.....0 to 3mA
PDC Current.....-1mA to 0
Operating Junction Temperature Range (T_j).....-55°C to +125°C
Storage Temperature Range .....-60°C to +160°C
Processing Temperature (Die).....+400°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(VCCD = VCCS = +3.3V ±5% or VCCD = +5.0V ±10%, VCCS = open, T_j = -40°C to +120°C, unless otherwise noted. Typical values are at +3.3V and T_j = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{VCC}			50	73	mA
Input Bias Voltage	V_{IN}			0.84	0.95	V
Differential Output Impedance	Z_{OUT}		90	105	120	Ω
LOP Output High Voltage	V_{OH}	Load = 4.7kΩ to V_{CCD} (Note 7)	V_{CCD} - 0.1		V_{CCD}	V
LOP Output Low Voltage	V_{OL}	Load = 4.7kΩ to V_{CCD} (Note 7)			0.4	V
Differential Output Voltage Swing	V_{OD}	R_L = 100Ω (differential), I_{IN} ≥ 7µAp-p	100	145		mVp-p
Output Common-Mode Voltage	V_{CM}	R_L = 100Ω (differential)		V_{CCD} - 0.12		V

AC ELECTRICAL CHARACTERISTICS

(VCCD = VCCS = +3.3V ±5% or VCCD = +5.0V ±10%, VCCS = open, T_j = -40°C to +120°C, unless otherwise noted. Typical values are at +3.3V and T_j = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Small-Signal Bandwidth	BW			1.8		GHz
Input Sensitivity	I_{IN}	2.5Gbps, 2^{23} - 1 PRBS, BER ≤ 10^{-10}, C_{IN} = 0.5pF, T_j = +120°C		7.8	(Note 3)	µAp-p
Input-Referred RMS Noise	N_{IN}	C_{IN} = 0.5pF, T_j = +120°C		433	566	nA
Low-Frequency Cutoff	f_L				100	kHz
Power-Supply Rejection Ratio	PSRR	f ≤ 2MHz, 100mVp-p	25	30		dB
LOP Hysteresis		Electrical (Note 4), low LOP assert, R_{PD} = 510Ω	3			dB
LOP Assert Level		R_{PD} = 510Ω	0.9			µA
LOP Deassert Level		R_{PD} = 510Ω			8.0	µA
Output Edge Speed	t_r, t_f	20% to 80% (Note 5)		50	70	ps
Pulse-Width Distortion	PWD	(Notes 5, 6)		21	80	ps

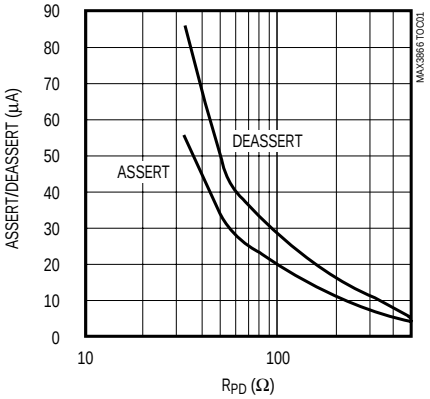
Note 1: C_{IN} = total capacitance on IN.
Note 2: AC parameters are guaranteed by design and characterization.
Note 3: See *Typical Operating Characteristics* for worst-case distribution.
Note 4: Hysteresis = 20 log ($V_{DEASSERT}$ / V_{ASSERT}).
Note 5: I_{IN} = 2.5mA.
Note 6: PWD = $|[(2 \cdot \text{Pulse Width}) - \text{Period}]| / 2$.
Note 7: External load not required for normal operation.

2.5Gbps, +3.3V Combined Transimpedance/Limiting Amplifier

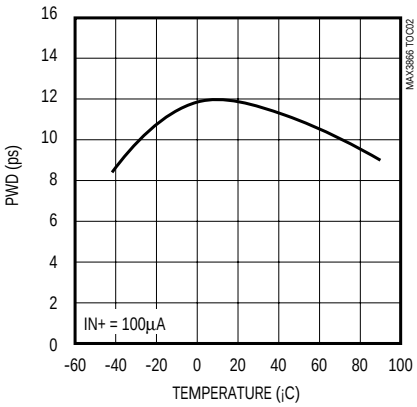
Typical Operating Characteristics

(V_{CCD} = V_{CCS} = +3.3V, T_A = +25°C, unless otherwise noted.)

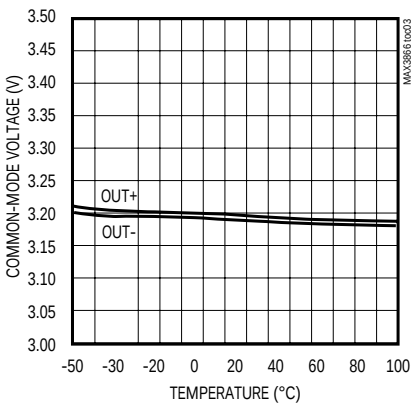
LOP ASSERT/DEASSERT vs. R_{PD}



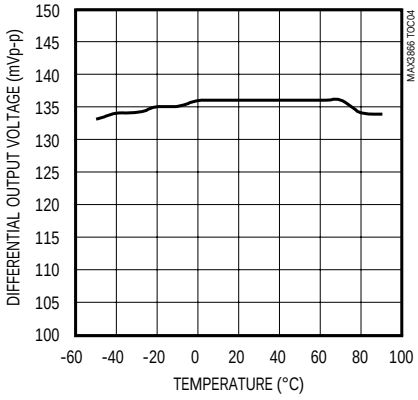
PULSE-WIDTH DISTORTION vs. TEMPERATURE



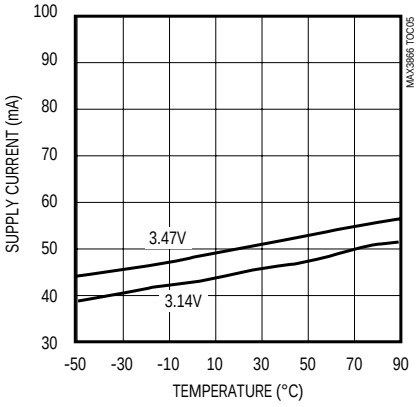
OUTPUT COMMON-MODE VOLTAGE vs. TEMPERATURE



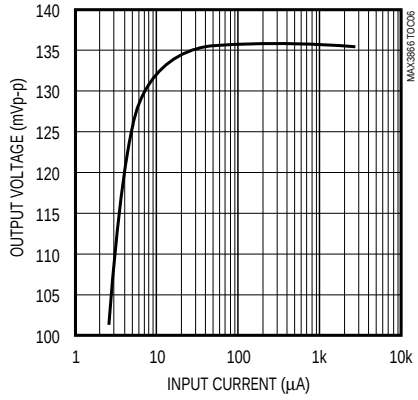
DIFFERENTIAL OUTPUT VOLTAGE vs. TEMPERATURE



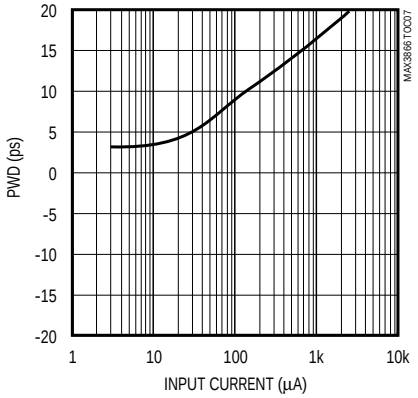
SUPPLY CURRENT vs. TEMPERATURE



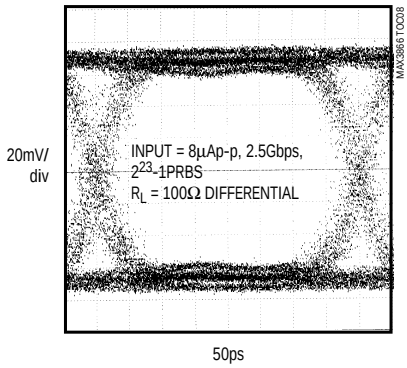
OUTPUT VOLTAGE vs. INPUT CURRENT



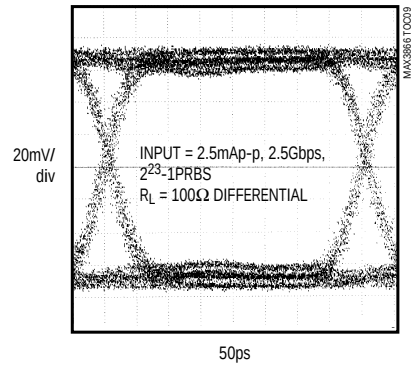
PULSE-WIDTH DISTORTION vs. INPUT CURRENT



ELECTRICAL EYE DIAGRAM



ELECTRICAL EYE DIAGRAM

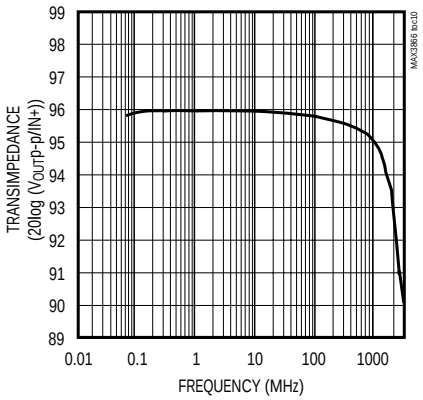


2.5Gbps, +3.3V Combined Transimpedance/Limiting Amplifier

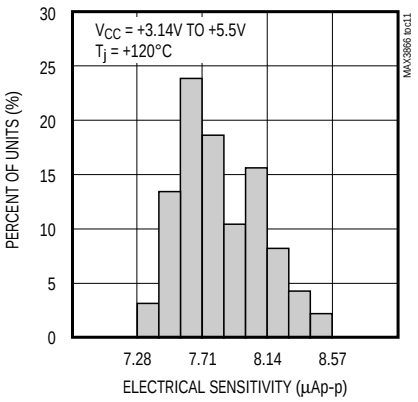
Typical Operating Characteristics (continued)

(V_{CCD} = V_{CCS} = +3.3V, T_A = +25°C, unless otherwise noted.)

SMALL-SIGNAL IMPEDANCE vs. FREQUENCY



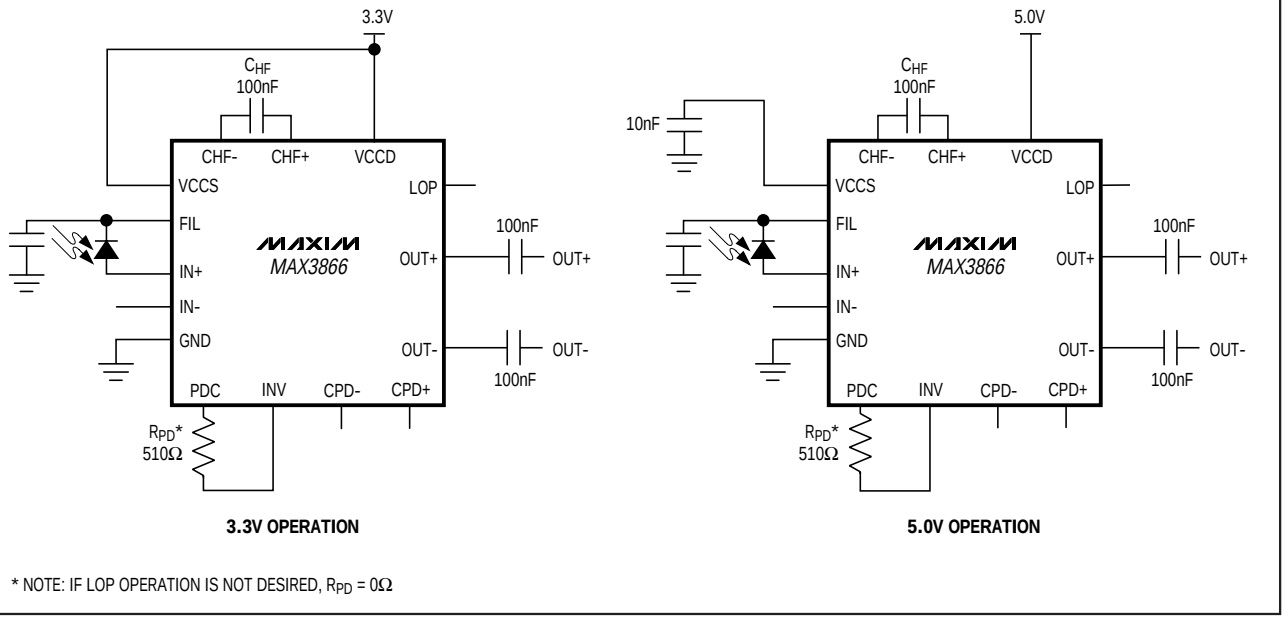
DISTRIBUTION OF ELECTRICAL SENSITIVITY (WORST CASE)



Pad Description

PAD NAME	FUNCTION
VCCS	Positive Supply Voltage of Input Stage. Apply +3.3V if VCCD = +3.3V. If VCCD > +3.47V, disconnect from supply and decouple to GND.
CHF+	External Filter Capacitor. A capacitor connected between CHF+ and CHF- is used for setting the low-frequency cutoff.
CHF-	External Filter Capacitor. A capacitor connected between CHF+ and CHF- is used for setting the low-frequency cutoff.
FIL	On-Chip Resistor for Filtering Photodiode Supply Voltage (connected to VCCD on chip)
GND	Electrical Ground
IN+	Signal Input
IN-	No Connect
PDC	The voltage at this node programs the gain of the power detector. Connect a resistor between PDC and INV to adjust the LOP threshold.
INV	Used for programming the gain of the power detector. Connect a resistor between PDC and INV to adjust the LOP threshold.
CPD-	Filter Node for Power Detector. A capacitor connected between CPD+ and CPD- will provide additional filtering to the rectifier output within the power detector.
CPD+	Filter Node for Power Detector. A capacitor connected between CPD+ and CPD- will provide additional filtering to the rectifier output within the power detector.
OUT-	Inverted Data-Signal Output
OUT+	Noninverted Data-Signal Output
LOP	TTL Output, Loss-of-Power, active high
VCCD	Power-Supply Voltage

Typical Operating Circuits



Circuit Description

Data Path

The combined preamplifier and limiting postamplifier (Figure 1) accepts an input current from a photodiode attached to the input pad IN+. The transimpedance input amplifier stage converts the input current to an output voltage with a typical transimpedance of 1.4kΩ.

The second stage of the data path is an active highpass filter. This filter converts the single-ended input signal to a differential signal, eliminating the DC component and adding approximately 16dB of gain. The output of the highpass filter drives the power detector and limiting amplifier circuitry.

The limiting amplifier circuit is the third stage of the data signal path. It amplifies and limits the differential input signal. The output stage is a differential pair with internal 50Ω load resistors. The limited output voltage is typically 145mVp-p.

Power Detector

The power detect circuit consists of an adjustable-gain amplifier and combined rectifier with a lowpass filter. The adjustable-gain amplifier is controlled by an op amp. The gain is adjusted by means of an external resistor connected between the PDC and INV pins.

The output voltage of the adjustable gain amplifier drives the combined rectifier and lowpass filter circuitry. The resulting DC voltage is fed to a Schmitt trigger, which generates a high-level output signal if the DC input signal is below the LOP assert level, thus causing an LOP condition on the LOP output.

Design Procedure

Power Supply

The complete amplifier is supplied by a single supply voltage, V_{CCD}. For operation at 3.3V, the supply voltage is applied at both the VCCD and VCCS pins (see *Typical Operating Circuit*). For operation at 5.0V, the voltage is only applied at VCCD. In this case, VCCS is on-chip controlled to approximately 3.2V. In the 5.0V configuration, an external 10nF grounded capacitor is required at the VCCS pin.

External Filter Capacitor C_{HF}

The value of C_{HF} affects the maximum speed at which the compensation loop adjusts the input offset current. C_{HF} should be chosen between 10nF and 100nF. The loop should be as slow as possible to reduce pattern-dependent jitter. Maxim recommends a value of C_{HF} = 100nF.

2.5Gbps, +3.3V Combined Transimpedance/Limiting Amplifier

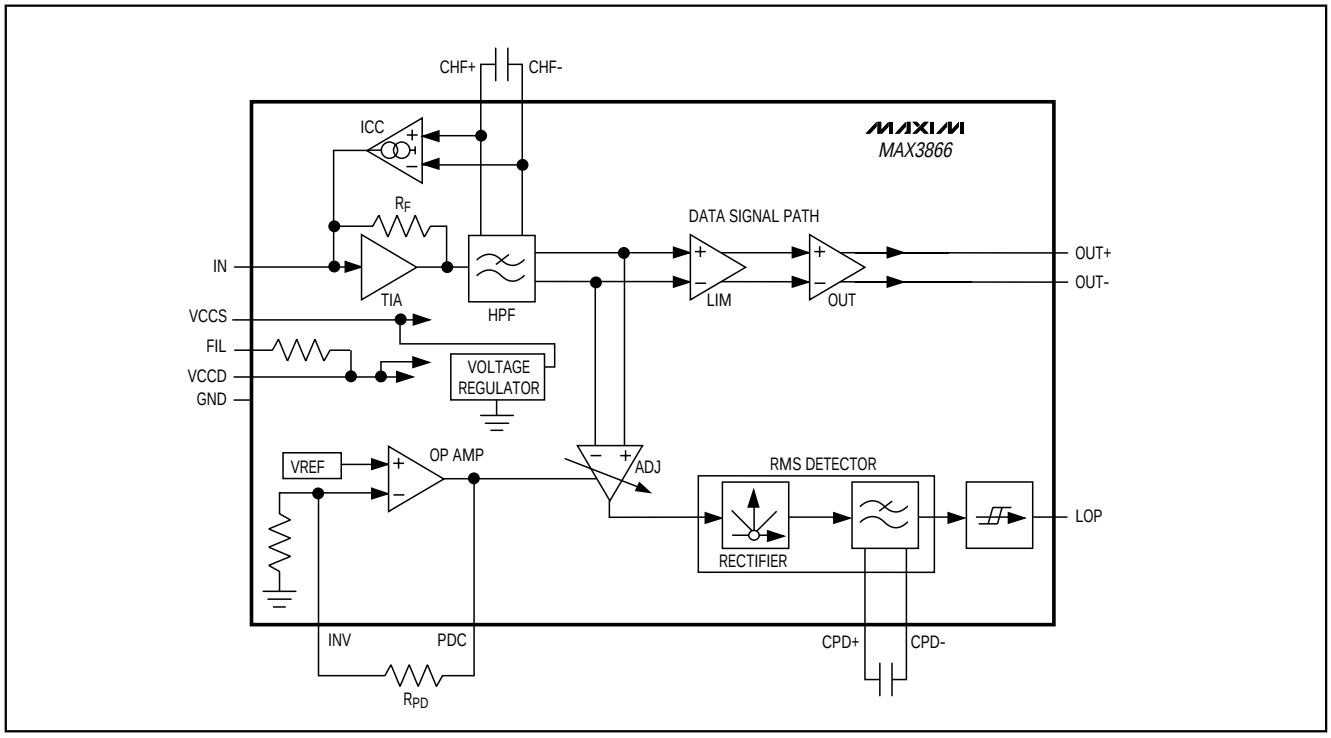


Figure 1. Functional Diagram of the Combined Preamplifier and Limiting Postamplifier

External Filter Capacitor CPD

The LF cutoff of the power detector can be reduced by adding external capacitance across the CPD pins. This capacitor is only needed when this circuit is operated at lower data rates and lower edge speeds. In this way, the remaining ripple of power detector output voltage is reduced.

Loss-of-Power Threshold

If the LOP function is desired, Maxim recommends R_{PD} = 510Ω. If the LOP function is not desired, R_{PD} = 0Ω (shorted). See Figure 2 for LOP definitions. If desired, the LOP threshold can be adjusted (see Assert/Deassert vs. R_{PD} in the *Typical Operating Characteristics.*

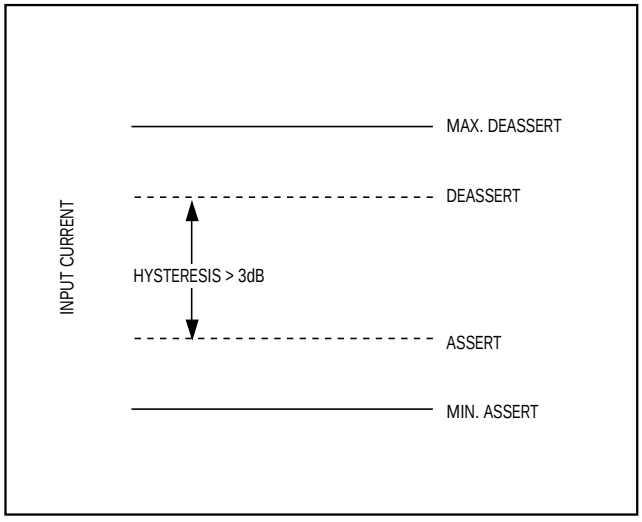


Figure 2. Loss-of-Power Definitions with R_{PD} = 510Ω

Internal Input/Output Schematics

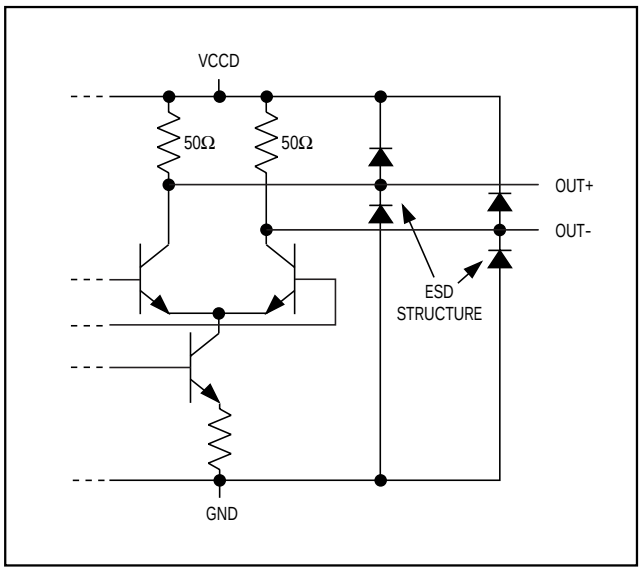


Figure 3. OUT Pads

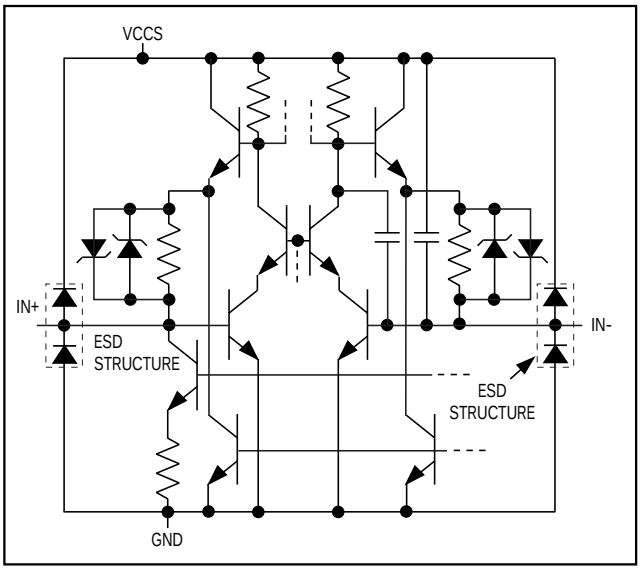


Figure 4. IN Pads

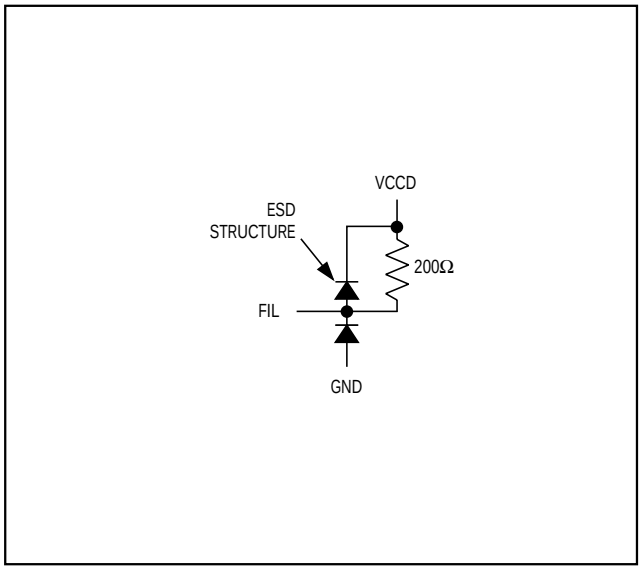


Figure 5. FIL Pads

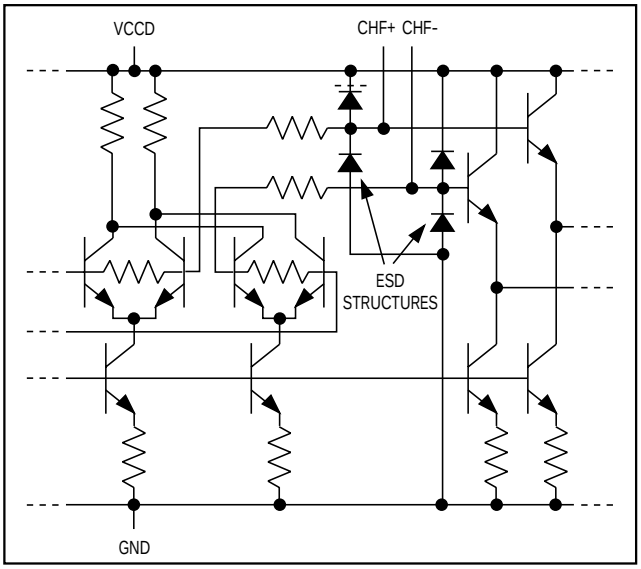


Figure 6. CHF Pads

Internal Input/Output Schematics (continued)

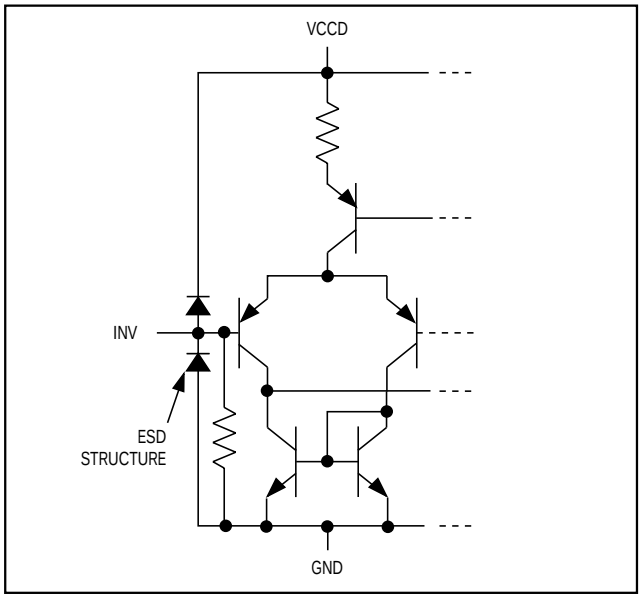


Figure 7. INV Pad

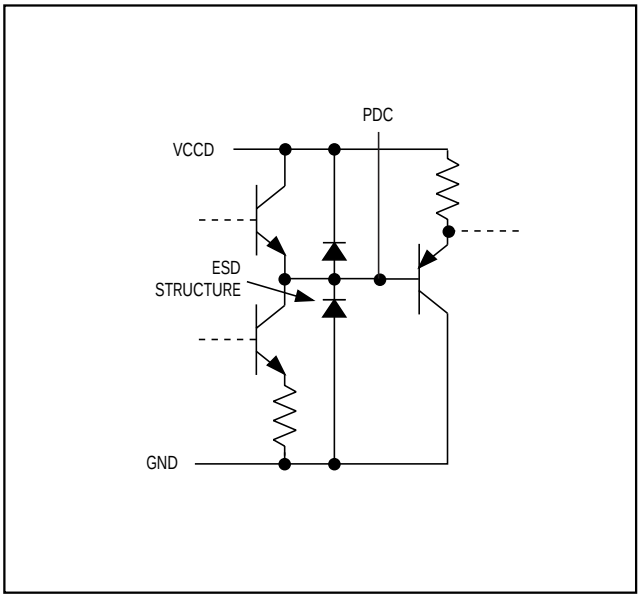


Figure 8. PDC Pad

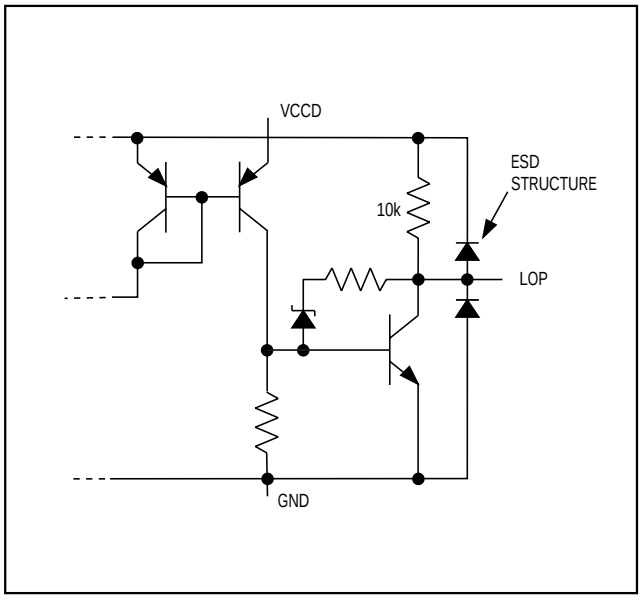


Figure 9. LOP Pad

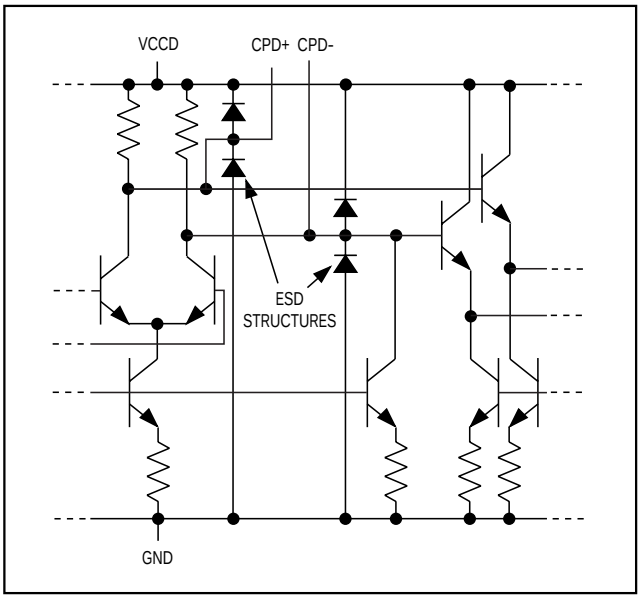


Figure 10. CPD Pad

Applications Information

Converting Average Optical Power to Signal Amplitude

Many of the MAX3866's specifications relate to input signal amplitude. When working with fiber optic receivers, the input is usually expressed in terms of average optical power and extinction ratio. The relations given in Table 1 are helpful for converting optical power to input signal when designing with the MAX3866.

In an optical receiver, the input current to the transimpedance amplifier can be found by multiplying the power relationships in Table 1 with the photodiode responsivity.

Wire Bonding

Make corrections to the die with gold wire only, using ball bonding techniques. Die pad size is 4mils (100µm) square and die thickness is 12mils (~300µm).

Layout Techniques

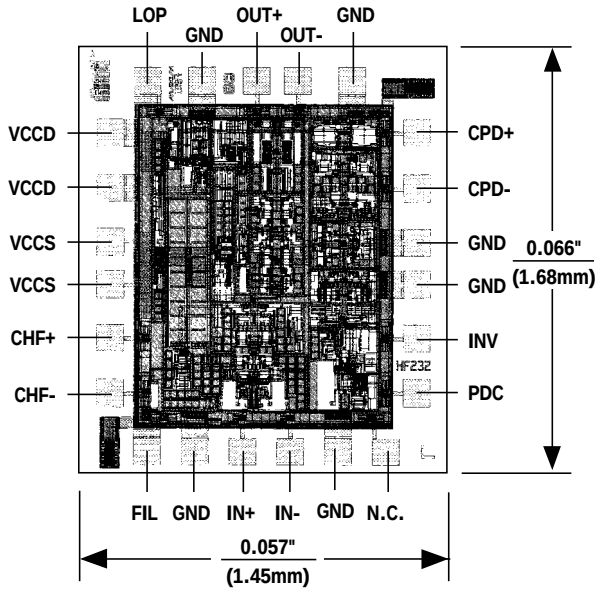
The MAX3866's performance can be greatly affected by circuit board layout and design. Use good high-frequency design techniques, including minimizing ground inductances and using fixed-impedance transmission lines on all data signals.

Table 1. Optical-Power Relations*

PARAMETER	SYMBOL	RELATION
Average Power	P_{AVE}	$P_{AVE} = (P0 + P1) / 2$
Extinction Ratio	r_e	$r_e = P1 / P0$
Optical Power of a "1"	P1	$P1 = 2P_{AVE}\frac{r_e}{r_e + 1}$
Optical Power of a "0"	P0	$P0 = 2P_{AVE} / (r_e + 1)$
Signal Amplitude	P_{IN}	$P_{IN} = P1 - P0 = 2P_{AVE}\frac{(r_e - 1)}{(r_e + 1)}$

**Assuming a 50% average input mark density.*

Pad Configuration



TRANSISTOR COUNT: 851

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