TDA7340G

AUDIO SIGNAL PROCESSOR

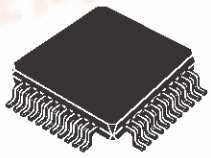
AUDIOPROCESSOR:
- MUTE, SOFT MUTE AND ZERO CROSSING MUTE
- ONE DIFFERENTIAL, TWO STEREO AND TWO MONO INPUTS
- DIFFERENTIAL PHONE INPUT
- VOLUME, BASS, TREBLE AND LOUDNESS CONTROL
- FOUR SPEAKER ATTENUATORS WITH INDEPENDENT ATTENUATION CONTROL

STEREODECODER:
- ROLL-OFF ADJUSTMENT
- ADJUSTMENT FREE INTEGRATED 456KHz VCO
- HIGH CUT CONTROL
- STEREO BLEND

NOISE BLANKER:
- INTEGRATED HIGH-PASS FILTER
- NOISE RECTIFIER OUTPUT FOR QUALITY DETECTION
- PROGRAMMABLE TRIGGER THRESHOLD
- DEVIATION AND FIELD STRENGTH DEPENDENT TRIGGER ADJUSTMENT

PAUSE DETECTOR:
- PROGRAMMABLE THRESHOLD

ALL FUNCTIONS PROGRAMMABLE VIA I^2C BUS



PQFP44

ORDERING NUMBER: TDA7340G

DESCRIPTION

The TDA7340G I^2C bus controlled audio signal processor contains all signal processing blocks of a high performance car radio, including audio-processor, stereodecoder, noise blanker, pause detector and different mute functions.
The use of BICMOS technology allows the implementation of several filter functions with switched capacitor techniques like fully integrated, adjustment free PLL Loop filter, pilot detector with integrator and pilot cancellation.

This minimizes the number of external components.

Due to a highly linear signal processing, using CMOS-switching techniques instead of standard bipolar multipliers, very low distortion and very low noise are obtained also in the stereodecoder part. The audioprocessor contains several new features like softmute, zero-crossing mute and pause detector.

Very low DC stepping is obtained by use of a BICMOS technology.

AUDIO PROCESSOR PART

FEATURES:

Input Multiplexer:

- DIFFERENTIAL CD STEREO INPUT
- CASSETTE STEREO INPUT
- FM STEREO INPUT FROM STEREODECODER
- AM INPUT:
  MONO OR STEREO MODE (PROGRAMMABLE)
- BEEP INPUT (ONLY IN AM MONO MODE)
- TELEPHONE DIFFERENTIAL MONO INPUT
- GAIN PROGRAMMABLE IN 3 x 3.75dB STEPS

Loudness:

- FULLY PROGRAMMABLE
- 15 x 1.25dB STEPS

Volume Control:

- 1.25dB COARSE ATTENUATOR
- 0.31dB FINE ATTENUATORS
- MAX GAIN 20dB
- MAX ATTENUATION 59.7dB (PLUS LOUDNESS)

Bass Control

- ±7 x 2dB STEPS
- 2nd ORDER SYMMETRICAL OR NON SYMMETRICAL CUT FREQUENCY RESPONSE

Treble Control

±7 x 2dB STEPS

Speaker Control

- 4 INDEPENDENT SPEAKER CONTROL IN 1.25dB STEPS
- CONTROL RANGE 37.5dB
- INDEPENDENT SPEAKER MUTE

Mute Functions

- DIRECT MUTE
- ZERO CROSSING MUTE WITH PROGRAMMABLE THRESHOLD
- SOFT MUTE WITH EXTERNAL DEFINED SLOPE
- SOFT MUTE VIA I^2C BUS OR EXTERNALLY CONTROLLED

Pause Detector

- PROGRAMMABLE THRESHOLD
- DELAY TIME DEFINED BY AN EXTERNAL CAPACITOR

STEREO DECODER PART

FEATURES:

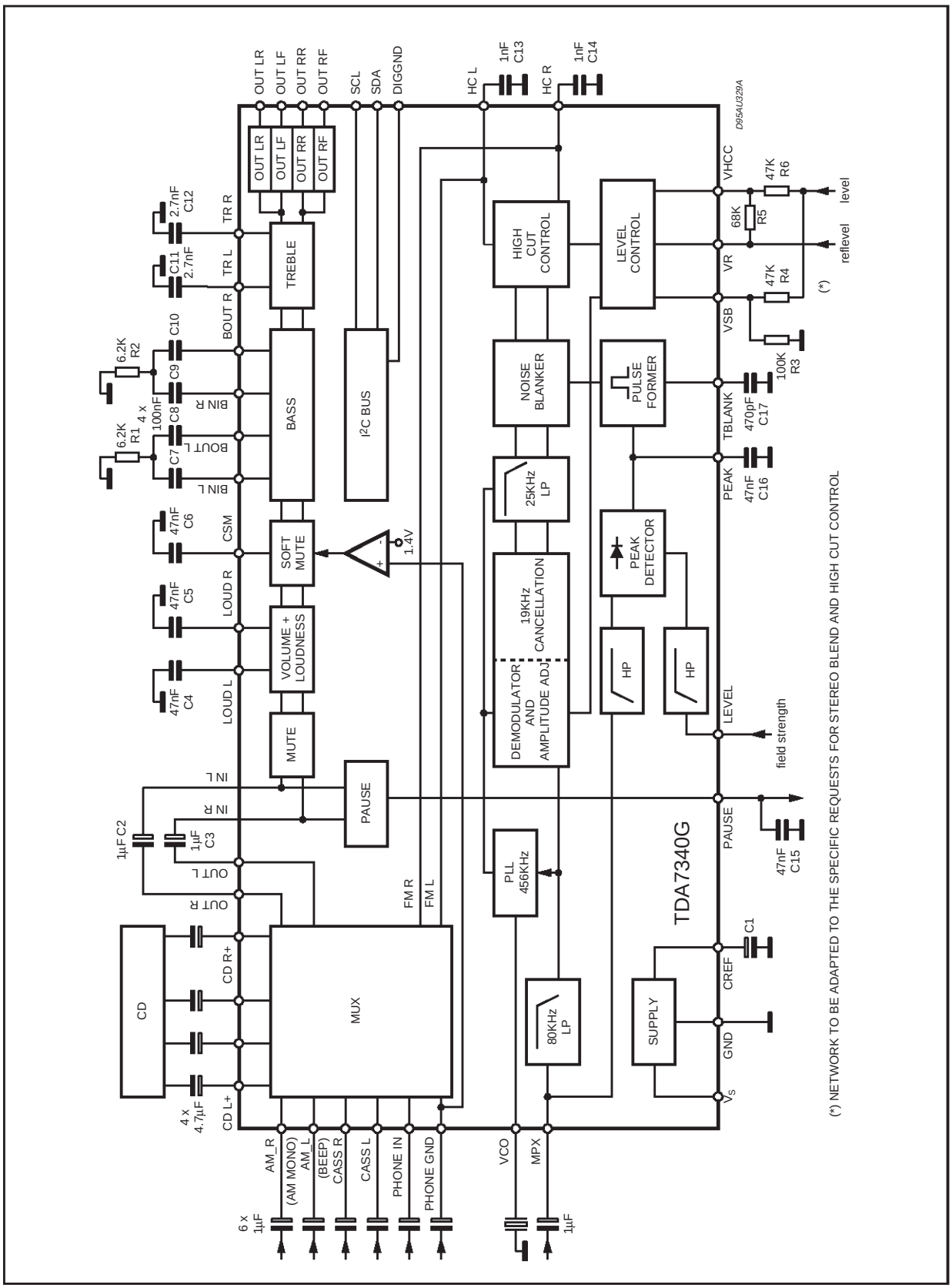
- INTERNALLY ADJUSTABLE ROLL-OFF COMPENSATION (I^2C BUS CONTROLLED)
- INTEGRATED PILOT CANCELLATION
- ON CHIP FILTER FOR PILOT DETECTOR AND PLL
- ADJUSTMENT FREE VOLTAGE CONTROLLED OSCILLATOR
- AUTOMATIC PILOT DEPENDENT MONO/STEREO SWITCHING
- VERY HIGH INTERMODULATION AND INTERFERENCE SUPPRESSION
- I^2C BUS CONTROLLED (STD OFF, FORCED MONO, STEREO)
- HIGH CUT CONTROL
- STEREO BLEND

NOISE BLANKER PART

FEATURES:

- INTERNAL 2nd ORDER HIGH-PASS FILTER
- NOISE RECTIFIER OUTPUT FOR SIGNAL QUALITY DETECTION
- PROGRAMMABLE TRIGGER THRESHOLD
- TRIGGER THRESHOLD DEPENDENT ON HIGH FREQUENCY NOISE
- BLANKING TIME PROGRAMMABLE BY EXTERNAL CAPACITOR
- VERY LOW OFFSET CURRENT DURING HOLD TIME DUE TO OPAMPS WITH MOS INPUTS
- LEVEL INPUT FOR ADDITIONAL SPIKE DETECTION ON FIELD STRENGTH WITH INTERNAL 1st ORDER + 20KHz HIGH PASS FILTER
- NOISE RECTIFIER OUTPUT FOR QUALITY DETECTION
- CIRCUITS FOR DEVIATION AND FIELD STRENGTH DEPENDENT TRIGGER ADJUSTMENT

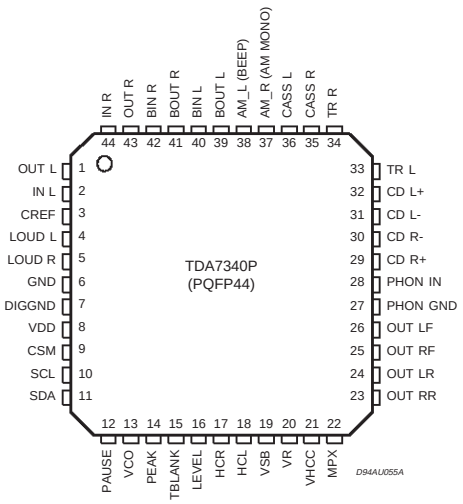
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Operating Supply Voltage	10.5	V
T_{amb}	Operating Temperature Range	-40 to 85	°C
T_{stg}	Storage Temperature Range	-55 to 150	°C

PIN CONNECTION



THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	max 85	°C/W

ELECTRICAL CHARACTERISTICS (V_S = 9V; T_{amb} = 25°C; R_L = 10KΩ; all gains = 0dB; f = 1KHz; C_{REF} = 22µF; unless otherwise specified, refer to the Test Circuit.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SUPPLY						
V_S	Supply Voltage		6	9	10	V
I_S	Supply Current	Stereo Decoder = ON	10	20	25	mA
		Stereo Decoder = OFF	5	12.5	20	mA
SVR	Ripple Rejection	Audioprocessor	70	90		dB
		Stereo Decoder + Audioprocessor		55		dB
INPUT SECTION						
R_I	Input Resistance		70	100	130	KΩ
V_{CL}	Clipping Level	d ≤ 0.3%	2.1	2.6		Vrms
S_I	Input Separation		80	100		dB
R_L	Output Load Resistance		2			KΩ
$G_{I\ MIN}$	Minimum Input Gain		-0.75	0	0.75	dB
$G_{I\ MAX}$	Max Input Gain		10.25	11.25	12.25	dB
G_{STEP}	Step Resolution		2.75	3.75	4.75	dB
e_{IN}	Input Noise	Single Ended Input		2.3		µV
V_{DC}	Dc Steps	Adjacent Gain Step		2	10	mV
		G_{MIN} to G_{MAX}		3		mV

ELECTRICAL CHARACTERISTICS (continued.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
DIFFERENTIAL CD STEREO INPUT						
R_I	Input Resistance	Input selector BIT D6 = 0 (0dB)	10	15	20	KΩ
		Input selector BIT D6 = 1(-6dB)	14	20	30	KΩ
CMRR	Common Mode Rejection Ratio	V_{CM} = 1V_{RMS} ; f = 1KHz	48	75		dB
		f = 10KHz	45	70		dB
d	Distortion	V_I = 1V_{RMS}		0.01	0.08	%
e_{IN}	Input Noise	20Hz to 20KHz; Flat; D6 = 0		5		μV
G_{DIFF}	Differential Gain	D6 = 0	-1	0	1	dB
		D6 = 1	-7	-6	-5	dB
DIFFERENTIAL TELEPHONE MONO INPUT						
R_I	Input Resistance		14	20	26	KΩ
CMRR	Common Mode Rejection Ratio	V_{CM} = 1V_{RMS} ; f = 1KHz	45	60		dB
d	Distortion	V_I = 1V_{RMS}		0.15	0.5	%
e_{IN}	Input Noise	20Hz to 3 KHz; Flat		10		μV
G_{DIFF}	Differential Gain		-4.75	-3.75	-2.75	dB
VOLUME CONTROL						
R_I	Input Resistance (INR, INL)		24	35	46	KΩ
C_{MAX}	Max Gain		18.75	20	21.25	dB
A_{MAX}	Max Attenuation		57.7	59.7	62.7	dB
A_{STEPC}	Step Resolution Coarse Attenuation		0.50	1.25	2.00	dB
A_{STEPF}	Step Resolution Fine Attenuation		0.11	0.31	0.51	dB
E_A	Attenuation Set Error	G = -20 to 20dB	-1.25	0	1.25	dB
		G = -20 to -59.7dB	3		2	dB
E_T	Tracking Error				2	dB
V_{DC}	DC Steps	Adjacent Attenuation Steps	-3	0.1	3	mV
		from 0dB to A_{MAX}		0.5	5	mV
LOUDNESS CONTROL (LOUDL, LOUDR)						
R_I	Internal Resistance		35	50	65	KΩ
A_{STEP}	Step Resolution		0.5	1.25	2.0	dB
A_{MAX}	Max Attenuation		17.5	18.75	20.0	dB
ZERO CROSSING MUTE						
V_{TH}	Zero Crossing Threshold (1)	WIN = 11		20		mV
		WIN = 10		40		mV
		WIN = 01		80		mV
		WIN = 00		160		mV
A_{MUTE}	Mute Attenuation		80	100		dB
V_{DC}	DC Step	0dB to Mute		0.3	3	mV
SOFT MUTE						
A_{MUTE}	Mute Attenuation		45	60		dB
t_D	Delay Time	C_{EXT} = 22nF; I = I_{MAX}	0.8	1.5	2.0	ms
		0 to -20dB; I = I_{MIN}	15	25	45	ms
SOFT MUTE AT PHONE-GND						
V_{il}	Input Low Voltage			1.4	1.6	V

(1) WIN represents the MUTE programming bit pair D6,D5 for the zero crossing window threshold

ELECTRICAL CHARACTERISTICS (continued.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
BASS CONTROL						
C_{RANGE}	Control Range		±11.5	±14	±16	dB
A_{STEP}	Step Resolution		1	2	3	dB
R_B	Internal Feedback Resistance		35	50	65	KΩ
TREBLE CONTROL						
C_{RANGE}	Control Range		±13	±14	±15	dB
A_{STEP}	Step Resolution		1	2	3	dB
SPEAKER ATTENUATORS						
C_{RANGE}	Control Range		35.0	37.5	40.0	dB
A_{STEP}	Step Resolution		0.5	1.25	2.0	dB
A_{MUTE}	Output Mute Attenuation	Data Word = 38.75dB	80	100		dB
E_A	Attenuation Set Error				1.50	dB
V_{DC}	DC Step	Adjacent Attenuation Steps		0.1	3	mV
AUDIO OUTPUTS						
V_{CLIP}	Clipping Level	d = 0.3%	2.1	2.6		V_{RMS}
R_L	Output Load Resistance		2			KΩ
R_{OUT}	Output Impedance			30	100	Ω
V_{DC}	DC Voltage Level		3.5	3.8	4.1	V
PAUSE DETECTOR						
V_{TH}	Zero Crossing Threshold (1)	WIN = 11		20		mV
		WIN = 10		40		mV
		WIN = 01		80		mV
		WIN = 00		160		mV
I_{DELAY}	Pull-up Current		15	25	35	µA
V_{THP}	Pause Threshold			3.0		V
GENERAL						
E_{NO}	Output Noise	BW = 20Hz to 20KHz, flat Output Muted All gains = 0dB		 2.5 5	 15	 µV µV
S/N	Signal to Noise Ratio	All gains 0dB; V_O = 1V_{RMS} ;		106		dB
d	Distortion	V_I = 1V_{RMS} ;		0.01	0.08	%
S_C	Channel Separation Left/Right		80	100		dB
E_T	Total Tracking Error	A_V = 0 to -20dB;		0	1	dB
		A_V = -20 to -60dB;		0	2	dB
$C_{REF\ (11)}$	External Reference Capacitor			10		µF
BUS INPUT						
V_{IL}	Input Low Voltage				1	V
V_{IH}	Input High Voltage		3			V
I_{IN}	Input Current	V_{IN} = 0.4V	-5		5	µA
V_O	Output Voltage SDA Acknowledge	I_O = 1.6mA		0.4	0.8	V

(1) WIN represent the MUTE programming bit palr D6,D5 for the zero crossing window threshold

STEREO DECODER PART

ELECTRICAL CHARACTERISTICS (V_S = 9V; modulation frequency: 1KHz; de-emphasis time: T = 50µs; nominal MPX input voltage: V_{MPX} = 0.5V_{RMS} (75KHz deviation); G_I = 3.5dB; T_{amb} = 27°C; unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{IN}	MPX Input Level			0.5	1.25	V_{RMS}
R_{IN}	Input Resistance		35	50	65	KΩ
G_{MIN}	Minimum Input Gain		2.5	3.5	4.5	dB
G_{MAX}	Maximum Input Gain		9.5	11	12.5	dB
G_{STEP}	Step Resolution		1.75	2.5	3.25	dB
SVRR	Supply Voltage Ripple Rejection	V_{RIPPLE} = 100mV; f = 1KHz	50	60		dB
V_O	DC Output Voltage (HCL, HCR)		4.2	4.5	4.8	V
α	Channel Separation	V_{SB} - V_R = 100m_{VDC}		50		dB
THD	Total Harmonic distortion			0.02	0.2	%
$\frac{S+N}{N}$	Signal plus noise to noise ratio	f = 20Hz to 16KHz; S = 2V_{RMS}		91		dB
CARRIER AND HARMONIC SUPPRESSION AT THE OUTPUT						
α19	Pilot Signal f = 19KHz		55	75		dB
α38	Subcarrier f = 38KHz			75		dB
α57	Subcarrier f = 57KHz			62		dB
α76	Subcarrier f = 76KHz			90		dB
INTERMODULATION (note 1)						
α2	f_{mod} = 10KHz; f_{spur} = 1KHz			65		dB
α3	f_{mod} = 13KHz; f_{spur} = 1KHz			75		dB
TRAFFIC RADIO (note 2)						
α57	Signal f = 57KHz			70		dB
SCA - SUBSIDIARY COMMUNICATIONS AUTHORIZATION (note 3)						
α67	Signal f = 67KHz			75		dB
ACI - ADJACENT CHANNEL INTERFERENCE (note4)						
α114	Signal f = 114KHz			95		dB
α190	Signal f = 190KHz			84		dB
MONO/ STEREO SWITCH						
V_{INTH}	Pilot Threshold Voltage	for stereo "ON" P_{th} = 1 P_{th} = 0	11 18	15 25	22 34	mV_{RMS} mV_{RMS}
V_{INTH}	Pilot Threshold Voltage	for stereo "OFF" P_{th} = 1 P_{th} = 0	6 13	12 19	18 25	mV_{RMS} mV_{RMS}
STEREO BLEND						
V_{SB-VR}	Control Voltage for Channel Separation	α = 6dB; V_R = 3.6V (note 5)	-0.31	-0.26	-0.23	V
V_{SB-VR}	Control Voltage for Channel Separation	α = 26dB;		-50		mV
HIGH CUT CONTROL						
τ_{deemp}	De-Emphasis Time Constant	C_{13}, C_{14} = 1nF; V_{HCC-VR} = 100mV		50		µs
R_{HCC}	High Cut Control Resistance	V_{HCC-VR} = 100mV		50		KΩ
R_{HCC}	High Cut Control Resistance	V_{HCC-VR} = -1.3V (note 6)	115	150	185	KΩ
VCO						
f_{OSC}	Oscillator Frequency				456	KHz
Δf/f	Capture and Holding Range				1	%

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
NOISE INTERFERENCE DETECTOR							
V_{TR}	Trigger Threshold 7) 8) (see pulse slope fig 3)	meas. with V_{RECT} = 1.2V	NTB = 10		100		mV_P
			NTB = 01		130		mV_P
			NTB = 10		160		mV_P
			NTB = 01		190		mV_P
		meas. with V_{RECT} = 1.4V	NTB = 00		150		mV_P
			NTB = 11		200		mV_P
			NTB = 10		250		mV_P
			NTB = 01		300		mV_P
V_{RECT}	Rectifier Voltage	V_{MPXIN} = 0mV		0.5	0.9	1.3	V
		V_{MPXIN} = 50mV;f = 200KHz			1.9		V
		V_{MPXIN} = 100mV; f = 200KHz		2.0	2.9	3.4	V
T_S	Suppression Pulse Duration	C_{BLANK} = 470pF			40		µs
I_{OS}	Input Offset Current During Suppression Time				10		pA
$V_{RECTDEV}$	Deviation Dependent Rectifier Voltage 9)	meas. with V_{MPX} =500mV (75KHz dev.)	OVD = 11(off)		0.9		V
			OVD = 10		1.3		V
			OVD = 01		2.3		V
			OVD = 00		3.2		V
V_{RECTFS}	Field strength Controlled Rectifier Voltage 10)	meas. with VMPX = 0mV, V_{SB} = V_R = -500 mV (Fully Mono)	FSC = 11(off)		0.9		V
			FSC = 10		1.2		V
			FSC = 01		1.8		V
			FSC = 00		2.2		V

NOTES TO THE CHARACTERISTICS

1) INTERMODULATION SUPPRESSION

$$\alpha 2 = \frac{V_O \text{ (signal) (at1KHz)}}{V_O \text{ (spurious) (at1KHZ)}} \text{ ; } f_s = (2 \times 10KHz) - 19KHz$$

$$\alpha 3 = \frac{V_O \text{ (signal) (at1KHz)}}{V_O \text{ (spurious) (at1KHZ)}} \text{ ; } f_s = (3 \times 13KHz) - 38KHz$$

measured with : 91% mono signal; 9% pilot signal; fm=10KHz or 13KHz

2) TRAFFIC RADIO (V.F.) suppression

$$\alpha 57 \text{ (V.W.F.)} = \frac{V_{O(signal)} \text{ (at1KHz)}}{V_O \text{ (spurious) (at1KHZ } \pm 23Hz)}$$

measured with : 91% stereo signal; 9% pilot signal; fm=1KHz; 5% subcarrier (f=57KHz, fm = 23Hz AM, m = 60%)

NOTES TO THE CHARACTERISTICS (continued)

3) SCA (SUBSIDIARY COMMUNICATIONS AUTHORIZATION)

$$\alpha 67 = \frac{V_{O(signal)}\ (at1KHz)}{V_O\ (spurious)\ (at9KHZ)}\ ;\ f_s = (2 \times 38KHz) - 67KHz$$

measured with : 81% mono signal; 9% pilot signal; fm=1KHz;
10% SCA - subcarrier (f_s = 67KHz, unmodulated)

4) ACI (ADJACENT CHANNEL INTERFERENCE)

$$\alpha 114 = \frac{V_O\ (signal)\ (at1KHz)}{V_O\ (spurious)\ (at4KHZ)}\ ;\ f_s = 110KHz - (3 \times 38KHz)$$

$$\alpha 190 = \frac{V_O\ (signal)\ (at1KHz)}{V_O\ (spurious)\ (at4KHZ)}\ ;\ f_s = 186KHz - (5 \times 38KHz)$$

measured with : 90% mono signal; 9% pilot signal; fm=1KHz; 1% spurious signal
(f_s = 110KHz or 186KHz, unmodulated)

5) Control range typ 11% of V_R (see figure 2)

6) Control range typ 30% of V_R (see figure 1)

7) All thresholds are measured by using a pulse with T_R = 2µs, T_{HIGH} = 2µs and T_F = 10µs.
The repetition rate must not increase the PEAK voltage.

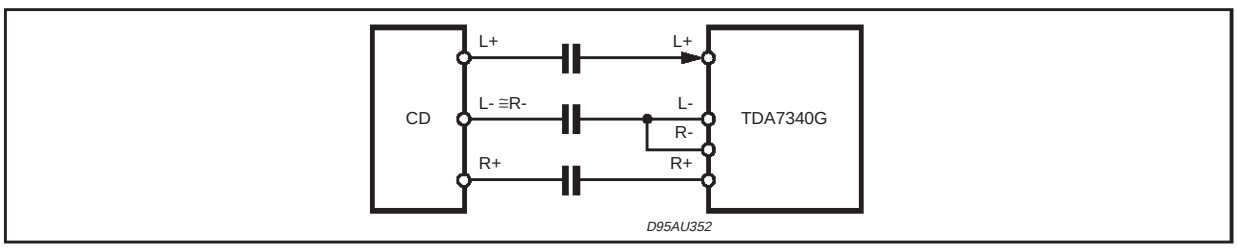
8) NBT represent the STDEC bit pair D_6, D_5 for the noise blanker trigger threshold
NAT represent the SPKR_LF bit pair D_7, D_5 for the noise controlled trigger threshold

9) OVD represent the SPKR_LR bit pair D_7, D_6 for the over deviation detector

10) FSC represent the SPKR_RF bit pair D_7, D_6 for the field strength control

11) The TDA7340G has a dedicated internal circuitry providing a soft power-on. The I2C bus data programmation must start after the reference DC level has reached the target Vs/2 value, otherwise a pop can be generated. The Cref pin and Out pins rise time at power on are riported in Figg.4, 5, 6 for Cref values of 4.7uF, 10uF, 22uF.

12) The CDL- and CDR- can be shortcircuited in applications providing 3 wires CD signal.



13)The AGND and DGND layout wires must be kept separated. A 50Ω resistor is recommend to be put as far as possible from the device.

Figure 1: High Cut Control

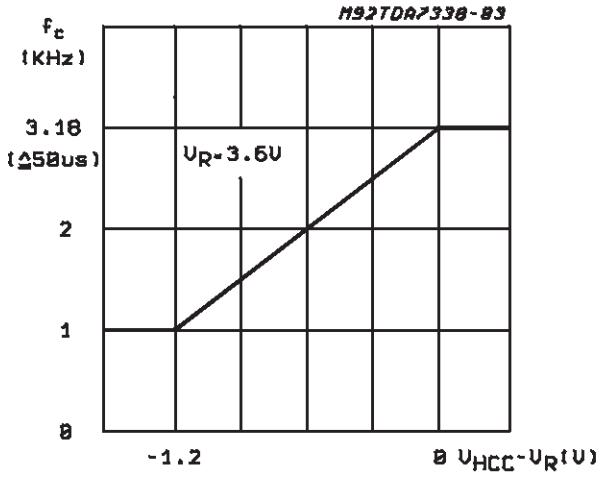


Figure 2: Stereo Blend

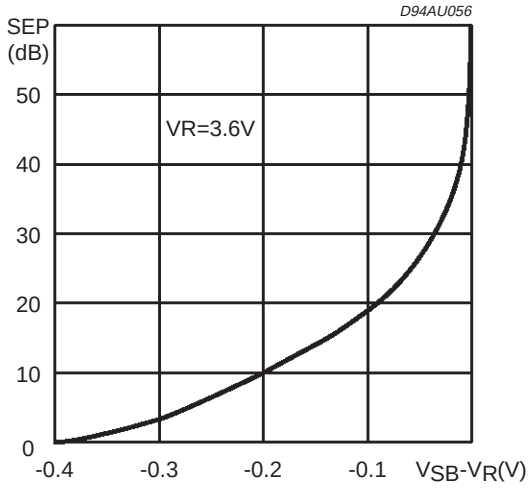
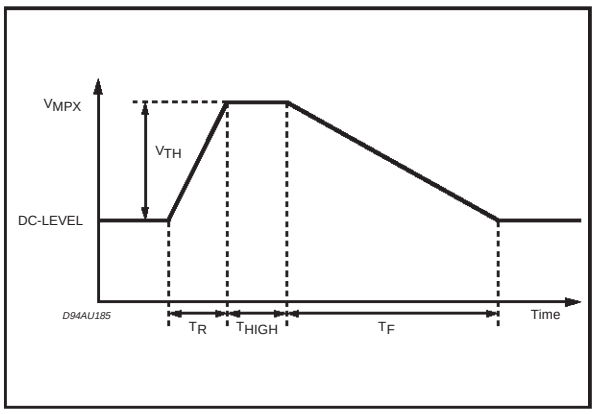


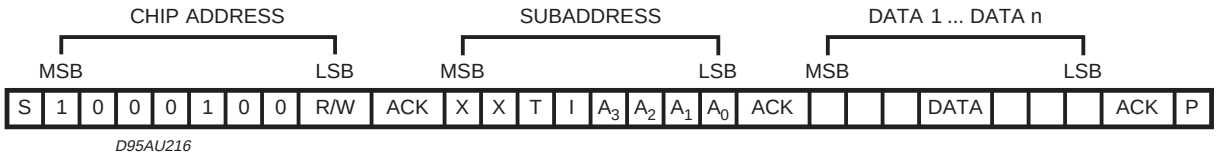
Figure 3



I²C BUS INTERFACE PROTOCOL

The interface protocol comprises:

- A start condition (s)
- A chip address byte, (the LSB bit determines read/write transmission).
- A subaddress byte
- A sequence of data (N-bytes + acknowledge)
- A stop condition (P)



ACK = Acknowledge

S = Start

P = Stop

I = Autoincrement

MAX CLOCK SPEED 500kbits/s

Autoincrement

If bit I in the subaddress byte is set to ”1”, the autoincrement of subaddress is enabled.

SUBADDRESS (RECEIVE MODE)

MSB							LSB	FUNCTION
X	X	T	I	A_3	A_2	A_1	A_0	
				0	0	0	0	Input Selector
				0	0	0	1	Loudness
				0	0	1	0	Volume
				0	0	1	1	Bass, Treble
				0	1	0	0	Speaker Attenuator LF
				0	1	0	1	Speaker Attenuator LR
				0	1	1	0	Speaker Attenuator RF
				0	1	1	1	Speaker Attenuator RR
				1	0	0	0	Mute
				1	0	0	1	Stereodecoder

T = Testmode I = Autoincrement X = Not Used

TRANSMITTED DATA (SEND MODE)

MSB							LSB
X	X	X	X	ST	SM	ZM	$\overline{P}$

P = Pause (low active)

ZM =Zero Crossing Muted (HIGH = active)

SM = Soft mute activated (HIGH = active)

ST = Stereo (HIGH = active)

X = Not used

The transmitted data is automatically updated after each 9th clock pulse.

Transmission can be repeated without new chipaddress.

DATA BYTE SPECIFICATION

X = not relevant; set to ”1”during testing

INPUT SELECTOR

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
0					0	0	0	Quasi Diff CD
1					0	0	0	Full Diff CD
					0	0	1	Stereo Decoder
					0	1	0	Cassette Stereo
		0			0	1	1	AM Mono
					1	0	0	Telephone Mono
		0			1	0	1	Beep Mono
		1			0	1	1	AM Stereo
					1	0	1	Not allowed
					1	1	0	Not allowed
					1	1	1	Not allowed
			0	0				11.25dB gain
			0	1				7.5dB Gain
			1	0				3.75dB Gain
			1	1				0 dB Gain
	0							0dB Differential input Gain (CD Input)
	1							-6dB Differential input Gain (CD Input)

For example to select quasi diff CD input with a gain of 7.5dB the Data Byte is: XXX01000

LOUDNESS

MSB							LSB	LOUDNESS
D7	D6	D5	D4	D3	D2	D1	D0	
X	X	X	0	0	0	0	0	0dB
X	X	X	0	0	0	0	1	-1.25dB
X	X	X	0	0	0	1	0	-2.5dB
X	X	X	0	0	0	1	1	-3.75dB
X	X	X	0	0	1	0	0	-5dB
X	X	X	0	0	1	0	1	-6.25dB
X	X	X	0	0	1	1	0	-7.5dB
X	X	X	0	0	1	1	1	-8.75dB
X	X	X	0	1	0	0	0	-10dB
X	X	X	0	1	0	0	1	-11.25dB
X	X	X	0	1	0	1	0	-12.5dB
X	X	X	0	1	0	1	1	-13.75dB
X	X	X	0	1	1	0	0	-15dB
X	X	X	0	1	1	0	1	-16.25dB
X	X	X	0	1	1	1	0	-17.5dB
X	X	X	0	1	1	1	1	-18.75dB
X	X	X	1	D_3	D_2	D_1	D_0	loudness OFF (1)

For example to select -17.5dB loudness the Data Byte is: XXX01110

Note (1):
If the loudness is switched OFF, the loudness stage is acting like a volume attenuator with flat frequency response. D0 to D3 determine the attenuation level

MUTE

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
							1	Soft Mute On
						0	1	Soft Mute with fast slope (I = I_{MAX})
						1	1	Soft Mute with slow slope (I = I_{MIN})
				1				Direct Mute
			0		1			Zero Crossing Mute ON
			0		0			ZC Mute OFF (delayed until next zero crossing)
			1					Zero Crossing Mute and Pause Detector Reset(*)
	0	0						160mV ZC Window Threshold (WIN = 00)
	0	1						80mV ZC Window Threshold (WIN = 01)
	1	0						40mV ZC Window Threshold (WIN = 10)
	1	1						20mV ZC Window Threshold (WIN = 11)
0								Nonsymmetrical Bass Cut
1								Symmetrical Bass Cut

An additional direct mute function is included in the Speaker Attenuators

(*) BIT D4 = 1disables the zero cross mute and pause detector, otherwise always active

SPEAKER ATTENUATORS

MSB							LSB	SPEAKER ATTENUATORS LF, LR, RF, RR
D7	D6	D5	D4	D3	D2	D1	D0	
								-1.25dB STEPS
					0	0	0	0dB
					0	0	1	-1.25dB
					0	1	0	-2.5dB
					0	1	1	-3.75dB
					1	0	0	-5dB
					1	0	1	-6.25dB
					1	1	0	-7.5dB
					1	1	1	-8.75dB
								10dB STEPS
			0	0				0dB
			0	1				-10dB
			1	0				-20dB
			1	1				-30dB
			1	1	1	1	1	Speaker Mute

For example an attenuationof 25dB on a selected output is given by: 11110100

Note:
If the speaker attenuator bytes the three MSBs are used for additional Noise blanker Roll off programming

STEREO DECODER

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
						0	0	11dB Input Gain
						0	1	8.5dB Input Gain
						1	0	6dB Input Gain
						1	1	3.5dB Input Gain
					0			Stereo Decoder Muted
				1				Stereo Decoder Off
			1					Forced Mono
	0	0						Noise Blanker Threshold 1 NBT 35mV
	0	1						Noise Blanker Threshold 2 NBT 45mV
	1	0						Noise Blanker Threshold 3 NBT 55mV
	1	1						Noise Blanker Threshold 4 NBT 65mV
0								Pilot Threshold High (P_{th} = 0)
1								Pilot Threshold Low (P_{th} = 1)

For example pilot threshold low, noise blanker threshold 3 (NTB = 10), Stereo decoder ON, 6dB input gain is given by: 11000010.

NOISE BLANKER: SPKR LF

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
								Noise Contrelled Trigger Adjustment (NAT) *) at V_{PEAK} = 1.5V
0	0							$V_{THNOISE}$ = 140mV
0	1							$V_{THNOISE}$ = 260mV
1	0							$V_{THNOISE}$ = 220mV
1	1							$V_{THNOISE}$ = 280mV
								Noise Blanker Trigger Threshold Fine Adjust
		0						The NBT Threshold is reduced by 5mV
		1						Threshold is as defined above (35, 45, 55, 65mV)

NOISE BLANKER: SPKR LR

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
								Over Deviation Detector (OVD) *) (V_{SB} = V_R = -1V, fully mono)
0	0							$V_{PEAKDEV}$ = 2.8V_{OP}
0	1							$V_{PEAKDEV}$ = 2.0V_{OP}
1	0							$V_{PEAKDEV}$ = 1.2V_{OP}
1	1							off
								Noise Blanker Input Mode *)
		0						Internal MPX trigger path is disabled and the LEVEL pin is directly connected to the trigger input (bypassing the high pass filter).
		1						Internal MPX trigger path and the LEVEL pin via the 120KHz high pass are connected (default)

NOISE BLANKER: SPKR RF

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
								Field Strength Control (FSC) *) (V_{SS} = V_R = -1V, fully mono)
0	0							V_{PEAKFS} = 2.4V
0	1							V_{PEAKFS} = 1.9V
1	0							V_{PEAKFS} = 1.4V
1	1							off
		0						Blend Mode on
		1						Blend Mode off

NOISE BLANKER: SPKR RR

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
								Roll Off Compensation
0	0	1						13.8%
0	1	0						15.6%
0	1	1						17.4%
1	0	0						19.2%
1	0	1						21%
1	1	0						22.8%
1	1	1						24.6%

*) See Noise blanker description

BASS/TREBLE

MSB						LSB		FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
								TREBLE STEPS
				0	0	0	0	-14dB
				0	0	0	1	-12dB
				0	0	1	0	-10dB
				0	0	1	1	-8dB
				0	1	0	0	-6dB
				0	1	0	1	-4dB
				0	1	1	0	-2dB
				0	1	1	1	0dB
				1	1	1	1	0dB
				1	1	1	0	2dB
				1	1	0	1	4dB
				1	1	0	0	6dB
				1	0	1	1	8dB
				1	0	1	0	10dB
				1	0	0	1	12dB
				1	0	0	0	14dB
								BASS STEPS
0	0	0	0					-14dB
0	0	0	1					-12dB
0	0	1	0					-10dB
0	0	1	1					-8dB
0	1	0	0					-6dB
0	1	0	1					-4dB
0	1	1	0					-2dB
0	1	1	1					0dB
1	1	1	1					0dB
1	1	1	0					2dB
1	1	0	1					4dB
1	1	0	0					6dB
1	0	1	1					8dB
1	0	1	0					10dB
1	0	0	1					12dB
1	0	0	0					14dB

For example12dB TREBLE and -8dB BASS give the following Data Byte : 00111001

VOLUME

MSB						LSB		FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
								0.31dB FINE ATTENUATION STEPS
						0	0	0
						0	1	-0.31dB
						1	0	-0.62dB
						1	1	-0.94dB
								1.25dB COARSE ATTENUATION STEPS
			0	0	0			0dB
			0	0	1			-1.25dB
			0	1	0			-2.5dB
			0	1	1			-3.75dB
			1	0	0			-5dB
			1	0	1			-6.25dB
			1	1	0			-7.5dB
			1	1	1			-8.75dB
								10dB GAIN ATTENUATION STEPS
0	0	0						20dB
0	0	1						10dB
0	1	0						0dB
0	1	1						-10dB
1	0	0						-20dB
1	0	1						-30dB
1	1	0						-40dB
1	1	1						-50dB

For example to select -47.81dB Volume the Data Byte is: 11011001

STATUS AFTER POWER ON RESET

VOLUME	-59.69dB
BASS, TREBLE	Treble = +2dB, Bass = 0dB, symmetrical
SPKRS LF, RF, LR, RR	-37.5dB
LOUDNESS	OFF, -17.5dB
INPUT	No input selected, GAIN = 0dB, DIFF CD GAIN = -06dB, FULLY DIFF MODE
STEREODEC	OFF, FORCED MONO, 6dB GAIN, PILOT THRESHOLD LOW, NOISE BLANKER =11
MUTE	DIRECTLY MUTED, SOFT OFF, ZEROCROSS RESET, WINDOW THRESHOLD =11
NOISE BLANKER	NTB = 11, NAT = 11, OVD = OFF, FSC OFF, BLEND MODE OFF, INTERNAL MPX PATH ENABLED

DESCRIPTION OF THE NOISE BLANKER

In the normal automotive environment the MPX signal is disturbed by ignition spikes, motors and high frequency switches etc.

The aim of the noise blanker part is to cancel the influence of the spikes produced by these components. Therefore the output of the stereodecoder is switched off for a time of 40µs (average spike duration).
In a first stage the spikes must be detected but to avoid a wrong triggering on high frequency noise a complex trigger control is implemented.

Behind the trigger stage a pulse former generates the 40µs ”blanking” pulse.
In the following section all of these circuits are described in their function and their programming, too (see fig.4).

1.1 Trigger Path

The incoming MPX signal is highpass-filtered, amplified and rectified (block RECT-PEAK).
The second order highpass-filter has a corner-frequency of 140KHz.

The rectifier signal, RECT, is used to generate by peak-rectification a signal called PEAK, which is available at the PEAK pin.

Also noise with a frequency >100KHz increases the PEAK voltage. The value of the PEAK voltage influences the trigger threshold voltage Vth (block ATC).

Both signals, RECT and PEAK+Vth are fed to a comparator (block PEAK-COMP) which outputs a sawtooth-shaped waveform at the TBLANK pin. A second comparator (block BLANK-COMP) forms the internal blanking duration of 40µs.

The noise blanker is supplied by his own biasing circuit (block BIAS-MONO).

1.2 Automatic Noise Controlled Threshold Control (ATC)

The are two independent possibilities for programming the trigger threshold:

a) the minimum threshold in 8 steps (bits D6, D5 of the STD-byte and bit D5 of the SPKR_LF byte)

b) and the noise adjusted threshold in 4 steps (bits D6, D5of the SPKR_LF byte, (see fig.5)

The minimum threshold is used in combination with a good MPX signal without any noise.

The sensitivity in this operation is high, depending only on the programmed "minimum trigger threshold", bits NTB of the noise blanker byte 1.

It is independent of the PEAK voltage.

If the MPX signal is noisy (low fieldstrength) the PEAK signal increases due to the higher noise, which is also rectified (see part 1.1).

With increasing of the PEAK voltage the trigger threshold voltage increases, too. This particular gain is programmable in 4 steps (see fig.2).

1.3 Automatic Threshold Control by the Stereoblend voltage (ATC-SB)

Besides the noise controlled threshold adjustment there is an additional possibility for influencing the trigger. It is controlled by the difference between Vsb and Vr, similar to the Stereoblend. The reason for implementing such a second control will be explained in the following:

The point where the MPX signal starts to become noisy is fixed by the RF part. Therefore also the starting point of the normal noise controlled trigger adjustment is fixed (fig.6).

But in some cases the behaviour of the noiseblanker can be improved by increasing the threshold even in a region of higher fieldstrength, for the MPX signal often shows distortion in this range.

Because of the overlap of this range and the range of the stereo/mono transition it can be controlled by Vsb and Vr.
This threshold increase is programmable in 3 steps or switched off (see fig.6).

1.4 Over Deviation Detector (MPX-RECT)

Sometimes when listening to stations with a higher deviation than 75KHz the noiseblanker triggers on the high frequency modulation.

To avoid this blanking, which causes noise in the output signal, the noiseblanker offers a deviation-dependent threshold adjustment.

By rectifying the MPX signal a further signal representing the actual deviation is obtained. It is used to increase the PEAK voltage.

Offset and gain of this circuit are programmable in 3 steps (the first step turns off the detector, see fig.7).

1.5 Blend Mode

Another possibility to avoid a disturbing triggering on modulation is to use the spikes on the fieldstrength signal (LEVEL pin).

But in the range of higher fieldstrength the signal saturates and no more spike detection is possible. For this reason the TDA7340G offers the "BLEND MODE". When "BLEND MODE" is activated a smooth transition between the LEVEL- and the MPX-signal is used to detect the spikes either on LEVEL or on MPX.

In the lower fieldstrength range mainly the LEVEL-signal is used whereas in the higher range mainly the MPX is used. This switching is controlled also by the normal Stereoblend signal to avoid additional pins.

With "BLEND MODE OFF" both signals are used to detect spikes in the whole fieldstrength range.

1.6 Input Mode

The NB of TDA7340G offers two input modes. The first one uses the internal trigger path and optional the LEVEL input. But the TDA7340G offers also an external trigger mode.

During this mode the internal MPX trigger path is disabled whereas the high pass at the LEVEL pin is bypassed.

By using an external highpass at the LEVEL-pin one can adjust the NB's behaviour to the desired one.

Figure 4: Block Diagram of the Noise Blanker

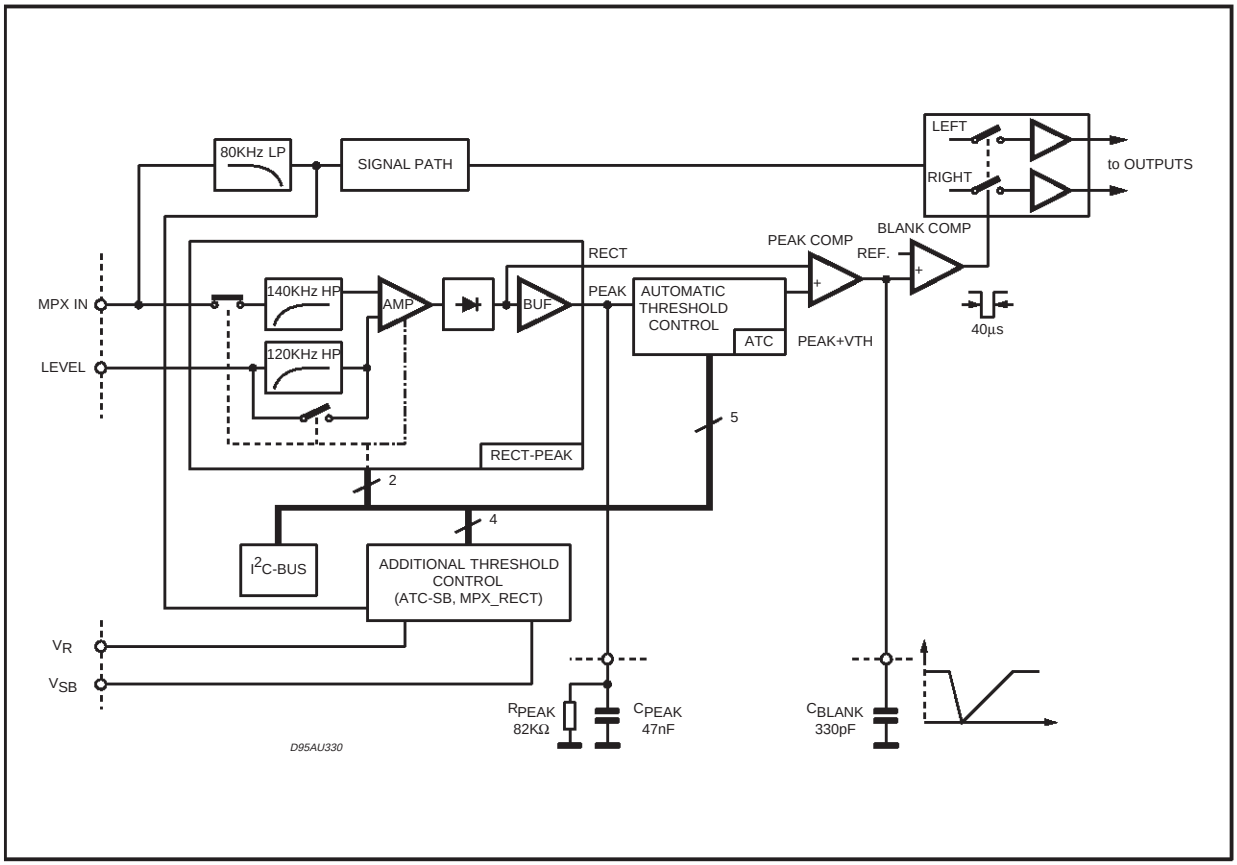


Figure 5: Trigger Threshold vs. V_{peak}

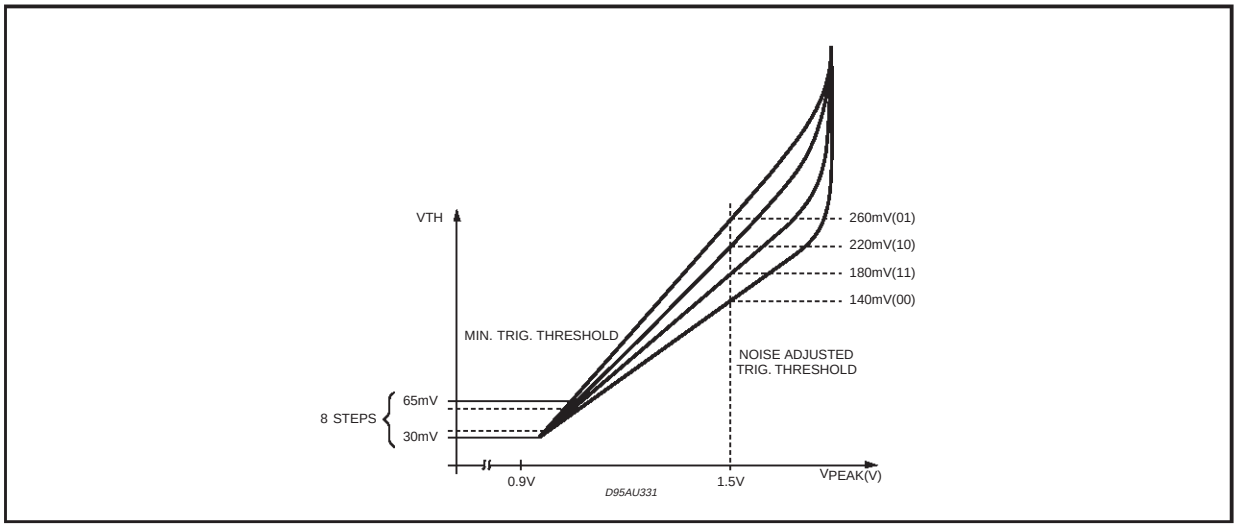


Figure 6: Behaviour of the Field Strength Controlled Threshold Adjustment

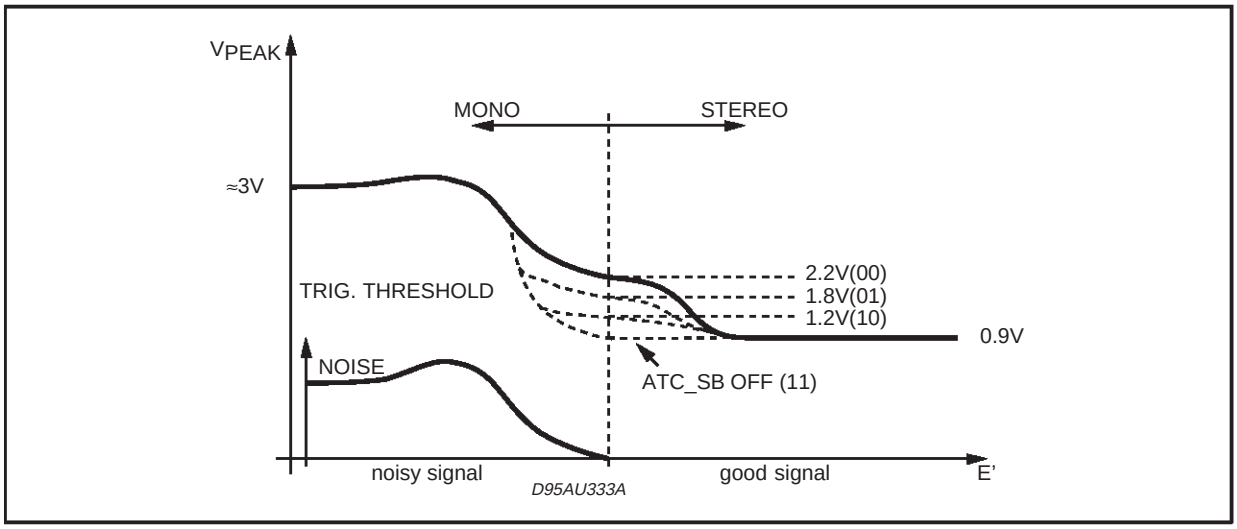
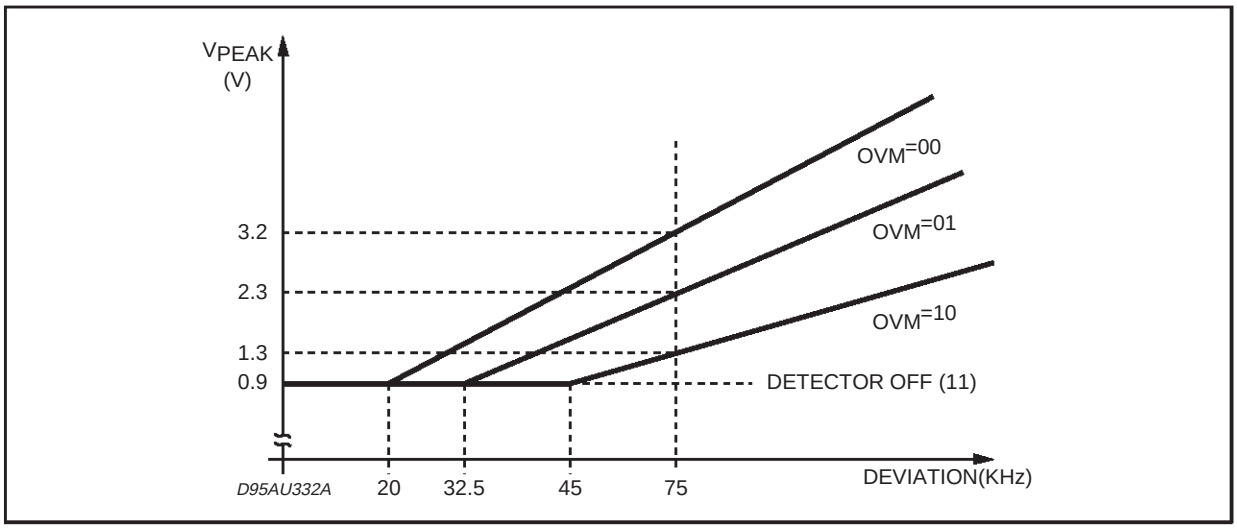


Figure 7: Behaviour of the Deviation Dependent Threshold Adiust (Over Deviation Detector)



MUTE & PAUSE FEATURES

The TDA7340G provides three types of mute, controlled via I2C bus (see pag.12, MUTE BYTE register).

SOFT MUTE

Bit **D0=1** → **Soft Mute ON**

Bit **D0=0** →**Soft Mute OFF**

It allows an automatic soft muting and unmuting of the signal.
The time constant is fixed by an external capacitor Csm inserted between pin Csm and ground.

Once fixed the external capacitor, two different slopes (time constant) are selectable by programmation of bit D1.

Bit **D1=1** → **fast slope (I=Imax)**

Bit **D1=0** → **slow slope (I=Imin)**

The soft mute generates a gradual signal decreasing avoiding big click noise of an immediate high attenuation, without necessity to program a sequence of decreasing volume levels. A response example is reported in Fig.12 (mute) and Fig.13 (unmute). The final attenuation obtained with soft mute ON is 60dB typical.
The used reference parameter is the delay time taken to reach 20dB attenuation (no matter what the signal level is).

Using a capacitor Csm=22nF this delay is:

d = 1. 8ms when selected Fast slope mode (bit D1=1)

d = 25 ms when selected Slow slope mode (bit D1=0)

In application, the soft mute ON programmation should be followed by programmation of DIRECT MUTE ON (see later) in order to achieve a final 100dB attenuation.

Beside the I2C bus programmation, the Soft Mute ON can be generated in a fast way by forcing a LOW level at pin phone GND, controlled by the µP through a transistor. This approach is recommended for fast RDS AF switching.

The Soft Mute status can be detected via I2C bus, reading the Transmitted Byte, bit SM (see data sheet pag.11).

read bit SM = 1 soft mute status ON

read bit SM = 0 soft mute status OFF

DIRECT MUTE

bit **D3 = 1** Direct mute ON
bit **D3 = 0** Direct nute OFF

The direct mute bit forces an internal immediate signal connection to ground.
It is located just before the Volume/Loudness stage, and gives a typical 100dB attenuation.

SPEAKERS MUTE

An additional direct mute function is included in the speakers attenuators stage.

The four output LF, RF, LR, RR can be separately muted by setting the speaker attenuator byte to the value 11111111 binary.

Typical attenuation level 100dB. This mute is useful for fader and balance functions. It should not be applied for system mute/unmute, because it can generate noise due to the offset of previous stages (bass / treble).

ZEROCROSSING MUTE

bit **D2=1 D4=0** zero crossing mute ON

bit **D2=0 D4=0** zero crossing mute OFF

The mute activation/deactivation is delayed until the signal waveform crosses the DC zero level (Vref level).

The detection works separately for the left and the right channels (see Figg. 14, 15). Four different windows threshold are software selectable by two dedicated bits.

bit **D6**	bit **D5**	**WINDOW**
0	**0**	Vref DC +/-160mV
0	**1**	Vref DC +/-80mV
1	**0**	Vref DC +/-40mV
1	**1**	Vref DC +/-20mV

The zero crossing mute activation/deactivation starts when the AC signal level falls inside the selected window (internal comparator).

The ZEROCROSS Mute (and Pause) detector is always active. It can be disabled, if the feature is not used, by forcing the bit **D4=1** Zero crossing and Pause detector reset.

In this way the internal comparator logic is stopped, eliminating its switching noise.

The zero cross mute status is detected reading the Transmitted Byte bit ZM.

bit **ZM = 1** zero cross mute status ON
bit **ZM = 0** zero cross mute status OFF

PAUSE FUNCTION

On chip is implemented a pause detector block.

It uses the same 4 windows threshold selectable for the zero crossing mute, bit D6,D5 byte MUTE (see above). The detector can be put in OFF by forcing bit **D4=1**, otherwise it is active.

The Pause detector info is available at PAUSE pin. A capacitor must be connected between PAUSE pin and Ground.

When the incoming signal is detected to be outside the selected window, the external capacitor is discharged. When the signal is inside the window, the capacitor is integrating up (see Figg.16 and 17).

The pause status can be detected in two ways:

a)by reading directly the Pause pin level.
The ON/OFF voltage threshold is 3.0V typical.
Pause OFF = level low (< 3.0V)
Pause ON = level high (; 3.0V)

b)by reading via I^2C bus the Transmitted Byte, bit P
P = 0 pause active.
P = 1 no pause detected.

The external capacitor value fixes the time constant.

The pull up current is 25uV typical
With input signal

Vin = 1Vrm --; Vdc pin pause = 15mV

Vin = 0Vrms --; Vdc pin pause = 5.62V

For example choosing Cpause = 100nF the charge up constant is about 22ms. Instead with Cpause = 15nF the charge up constant is about 360us.

The Pause detection is useful in applications like RDS, to perform noiseless tuning frequeny jumps avoiding to mute the signal.

NO SYMMETRICAL BASS CUT RESPONSE

bit **D7=0** No symmetrical

bit **D7=1** Symmetrical

The Bass stage has the option to generate an unsymmetrical response, for cut mode settings (bass level from -2db to - 14dB)

For example using a T-type band pass external

filter, the bass cut response becomes a low pass filter, while the response in bass boost condition is unchanged.

The feature is useful for human ear equalization in noisy enviroments like cars etc.

See examples in Fig. 18 (symmetrical response) and Fig. 19 (unsymmetrical response).

TRANSMITTED DATA (SEND MODE)

bit	**P = 0**	Pause active
bit	**P = 1**	No pause detected
bit	**ZM = 1**	Zero cross mute ON
bit	**ZM = 0**	Zero cross mute OFF
bit	**SM = 1**	Soft mute ON
bit	**SM = 0**	Soft mute OFF
bit	**ST = 1**	Stereo signal detected (input MPX)
bit	**ST = 0**	Mono signal detected (input MPX)

The TDA7340G allows the reading of four info bits.

The type (Stereo/Mono) of received broadcasting signal is easily checked and displayed by using the **ST** bit.

The **P** bit check is useful in tuning jumps without signal muting.

The **SM** soft mute status becomes active immediately, when bit D0 is set to 1 (soft mute ON, MUTE byte) and not when the signal level has reached the 60 dB final attenuation.

TDA7340G I^2C BUS PROTOCOL

The protocol is standard I^2C, using subaddress byte plus data bytes (see pagg.11 to 16).

The optional Autoincrement mode allows to refresh all the bytes registers with transmission of a single subaddress, reducing drastically the total transmission time.

Without autoincrement, subaddress bit **I = 0,** to refresh all the bytes registers (10), it is necessary to transmit 10 times the chip address, the subaddress and the data byte.

Working with a 100Kb/s clock speed the total time would be :

[(9*3+2)*10]bits*10us=2.9ms

Instead using autoincrement mode, subaddress bit **I=1,** the total time will be:

(9*12+2)*10us=1.1ms.

The autoincrement mode is useful also to refresh partially the data. For example to refresh the 4 speakers attenuators it is possible to program the subaddress Spkr LF (code XX010100), followed by the data byte of SPKR LF, LR, RF, RR in sequence.

Note:
that the autoincrement mode has a module 16 counter, whereas the total used register bytes are 10.

It is not correct to refresh all the 10 bytes starting from a subaddress different than XX010000.

For example using subaddress XX010010 (volume) the registers from Volume to Stereodecoder (see pag.11) are correctly updated but the next two transmitted bytes instead to refer to the wanted Input selector and Loudness are discharged. (the solution in this case is to send two separated pattern in autoinc mode, the first composed by address, subaddress XX010010, 8 data bytes, and the second composed by address, subaddress XX010000, 2 data bytes).

With autoincrement disabled, the protocol allows the transmission in sequence of N data bytes of a specific register, without necessity to resend each time the address and subaddress bytes.

This feature can be implemented, for example, if a gradual Volume change has to be performed (the MCU has not to send the STOP condition, keeping active the TDA7340G communication).

WARNING

The TDA7340G always needs to receive a STOP condition, before beginning a new START condition. The device doesn't recognize a START condition if a previously active communication was not ended by a STOP condition.

I^2C BUS READ MODE

The TDA7340G gives to the master a 1 byte "TRANSMITTED INFO" via I2C bus in read mode. The read mode is Master activated by sending the chip address with LSB set to 1, followed by acknowledge bit.

The TDA7340G recognizes the request. At the following master generated clocks bits, the TDA7340G issues the TRANSMITTED INFO byte on the SDA data bus line (MSB transmitted first).

At the nineth clock bit the MCU master can:

- acknowledge the reception, starting in this way the transmission of another byte from the TDA7340G.
- no acknowledge, stopping the read mode communication.

LOUDNESS STAGE

The previous STMicroelectronics audioprocessors were implementing a fixed loudness response, only ON/OFF sw programmable.

No possibility to change the loud boost rate at a certain volume level.

The TDA7340G implements a fully programmable loudness control in 15 steps of 1.25dB.

It allows a customized loudness response for each application.

The external network connected to the loudness pins LOUD_L and LOUD_R fixes the type of loudness response

1) Simple Capacitor
The loudness effect is only a boost of low frequencies. (see Fig.20)

2)Second order Loudness (boost of low and high frequencies).

3)Second order decreased type Loudness (lower boost of low and high frequencies).

4)Second order modified type Loudness (higher boost of low and high frequencies).

BASS FILTER

Several bass filter types can be implemented. Normally it is used the basic T-type Bandpass Filter. Starting from the filter component values (R1 internal and R2, C1, C2 external), the centre frequency Fc, the gain Av at max bass boost and the filter Q factor are computed as follows:

$$F_c = \frac{1}{2 \cdot \Pi \cdot \sqrt{(R1 \cdot R2 \cdot C1 \cdot C2)}}$$

$$A_v = \frac{R2 \cdot C2 + R2 \cdot C1 + R1 \cdot C1}{R2 \cdot C1 + R2 \cdot C2}$$

$$Q = \frac{\sqrt{(R1 \cdot R2 \cdot C1 \cdot C2)}}{R2 \cdot C1 + R2 \cdot C2}$$

Viceversa fixed Fc, Av, and R1 = 50KΩ (internal typ.+/-30%), the external component values are:

$$C1 = \frac{A_v - 1}{2 \cdot \Pi \cdot R1 \cdot Q}$$

$$C2 = \frac{Q \cdot Q \cdot C1}{A_v - 1 - Q \cdot Q}$$

$$R2 = \frac{A_v - 1 - Q \cdot Q}{2 \cdot \Pi \cdot C1 \cdot F_c \cdot (A_v - 1) \cdot Q}$$

TREBLE STAGE

The Treble stage is a simple high pass filter which time constant is fixed by internal resistor (50Kohm typ) and an external capacitor connected between pins TREB_R/TREB_L and Ground.

IN-OUT PINS

The multiplexer output is available at OUT_R and OUT_L pins for optional connection of external graphic equalizer (TDA7316/TDA7317), surround chip (TDA7346) etc.

The signal is fed in again at pins IN_L and IN-R.

In case of application without external devices the pins OUT_L/OUT_R and IN_L/IN_R cannot be short circuited, but must be decoupled via capacitor, necessary to avoid signal DC jumps, generating "Clicking" output noise.

The input impedance of the next volume stage is 35Kohm typical (minimum 24Kohm). A capacitor no lower than 1uF should be used.

INPUT SELECTOR

The multiplexer selector can choose one of the following inputs:

- a differential CD stereo input.
- an FM stereo input coming from the on chip-stereo decoder.
- a Cassette stereo input.
- a Telephone Differential mono input.
- an AM stereo input or alternatively (sw programmable) an AM mono + BEEP mono.

The signal fed to the input pins must be decoupled via series capacitors. The minimum allowed value depends on the correspondent input impedance.

For the CD diff input (Zi=10Kohm worst case) a Cin=4.7uF is recommended.

For the other inputs (70Kohm worst case, except PHONE 14Kohm worst case but speech audio band) a Cin=1uF is recommended.

Figure 8: Power on Time Constant vs Cref Capacitor C_{REF} =4.7µF

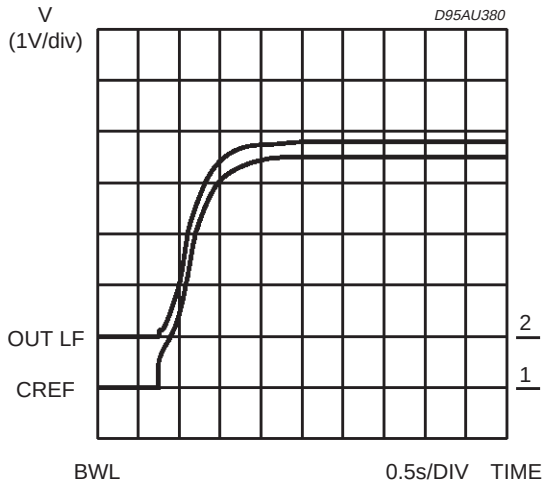


Figure 9: Power on Time Constant vs Cref Capacitor C_{REF} =10µF

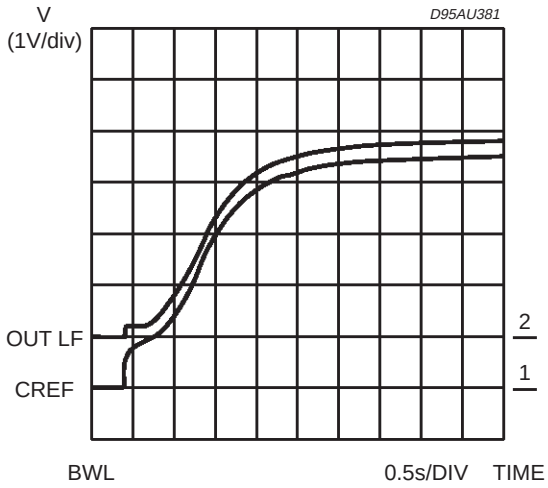


Figure 10: Power on Time Constant vs Cref Capacitor C_{REF} =22µF

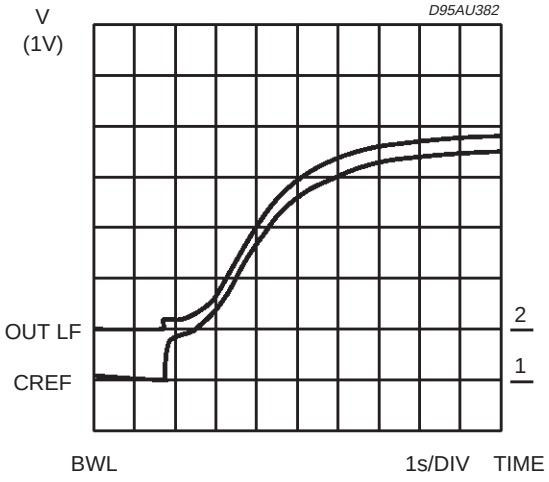


Figure 11: SVRR vs. Frequency

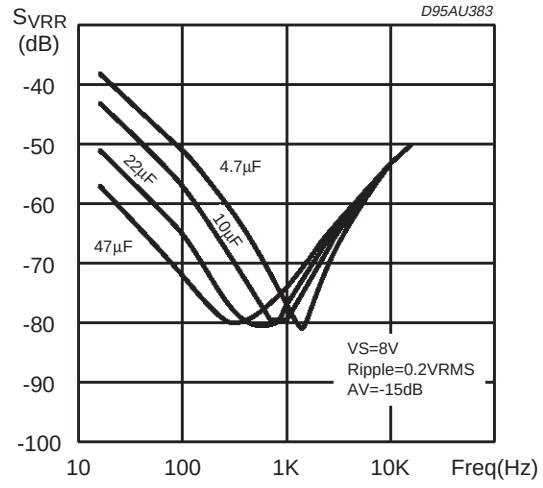


Figure 12: Soft Mute ON

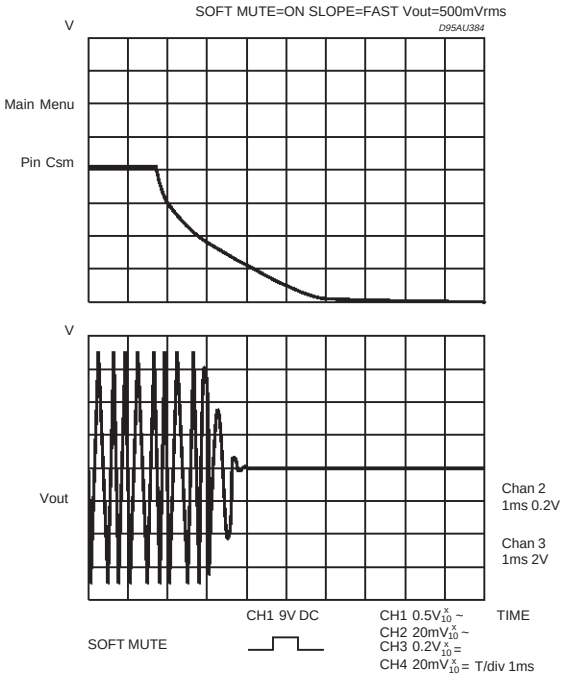


Figure 13: Soft Mute ON

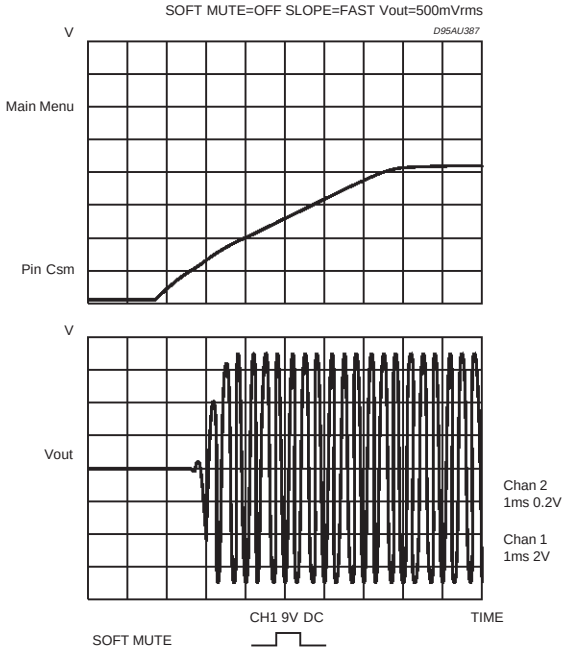


Figure 14: Zero Crossing Mute ON

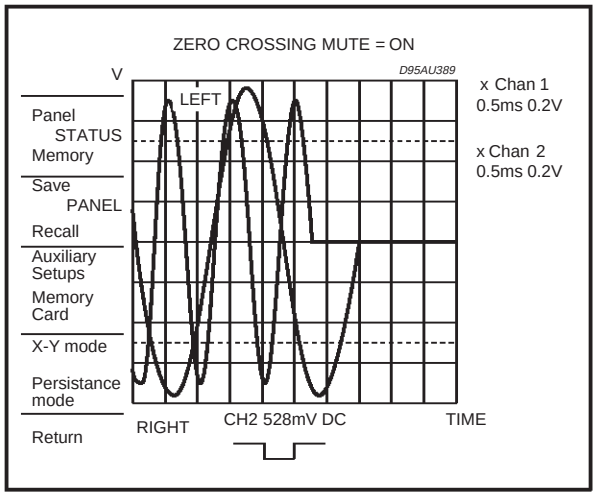


Figure 15: Zero Crossing Mute OFF

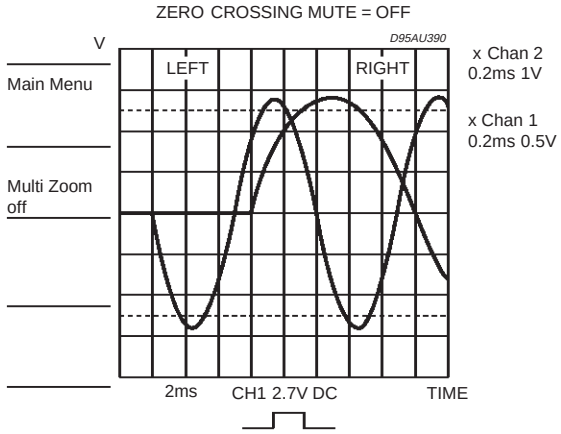


Figure 16: Pause Detector

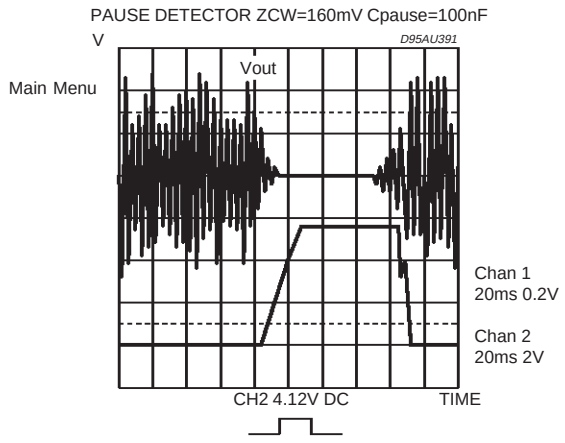


Figure 17: Pause Detector

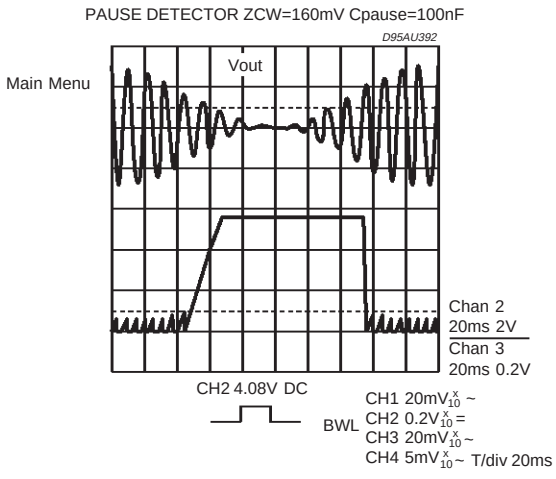


Figure 18: Sym_Bass

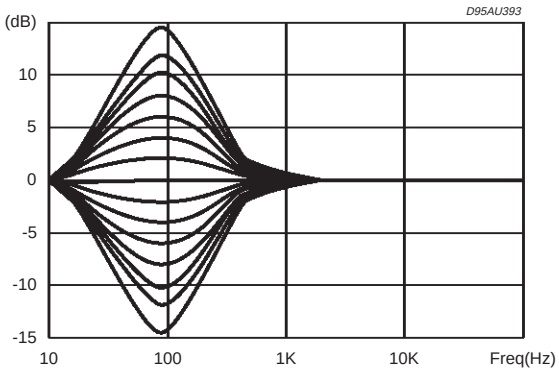


Figure 19: Non_Sym_Bass

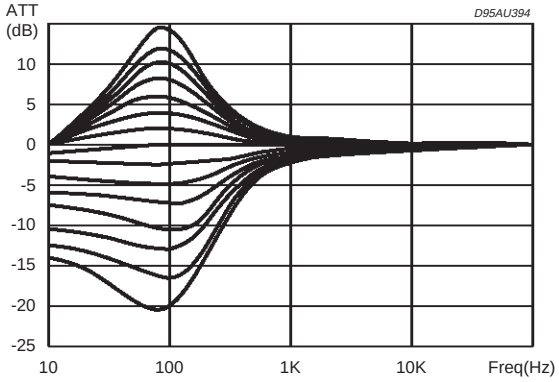
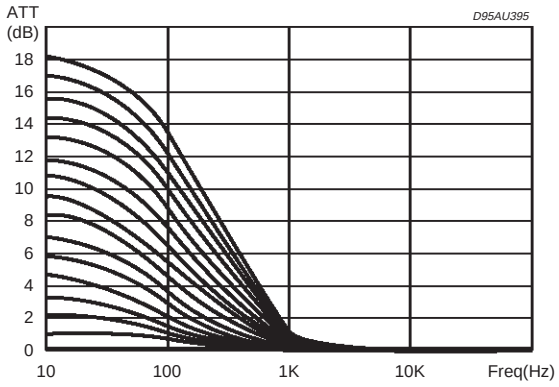
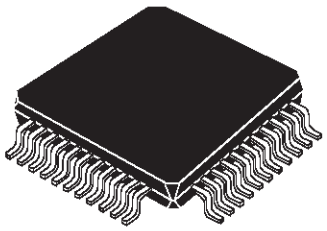


Figure 20: Loudness



DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.45			0.096
A1	0.25			0.010		
A2	1.95	2.00	2.10	0.077	0.079	0.083
B	0.30		0.45	0.012		0.018
c	0.13		0.23	0.005		0.009
D	12.95	13.20	13.45	0.51	0.52	0.53
D1	9.90	10.00	10.10	0.390	0.394	0.398
D3		8.00			0.315	
e		0.80			0.031	
E	12.95	13.20	13.45	0.510	0.520	0.530
E1	9.90	10.00	10.10	0.390	0.394	0.398
E3		8.00			0.315	
L	0.65	0.80	0.95	0.026	0.031	0.037
L1		1.60			0.063	
K	0°(min.), 7°(max.)					

OUTLINE AND MECHANICAL DATA



PQFP44 (10 x 10)