DATA SHEET

TDA8767
12-bit high-speed Analog-to-Digital Converter (ADC)

Preliminary specification
Supersedes data of 1997 Jun 27
File under Integrated Circuits, IC02

1999 Feb 16

Philips Semiconductors

PHILIPS

12-bit high-speed Analog-to-Digital Converter (ADC)

TDA8767

FEATURES

- 12-bit resolution
- Sampling rate up to 30 MHz
- –3 dB bandwidth of 18 MHz
- No missing codes guaranteed
- 5 V power supplies
- Binary or two's complement CMOS outputs
- In-range CMOS output
- TTL/CMOS compatible static digital inputs
- 3 to 5 V CMOS digital outputs
- TTL compatible clock input
- Power dissipation 335 mW (typ.)
- Low analog input capacitance (typ. 2 pF), no buffer amplifier required
- No external sample-and-hold circuit required
- Differential or single analog Input
- External amplitude range control
- Voltage controlled regulator included.

APPLICATIONS

- High-speed analog-to-digital conversion for:
  - Video signal digitizing
  - High Definition TV (HDTV)
  - Imaging (camera, scanner)
  - Medical imaging
  - Telecommunication
  - Base-station receiver.

GENERAL DESCRIPTION

The TDA8767 is a bipolar 12-bit Analog-to-Digital Converter (ADC) for imaging or other applications. It converts the analog input signal into 12-bit binary coded digital words at a maximum sampling rate of 30 MHz. All digital inputs and outputs are CMOS compatible.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output supply voltage		3.0	3.3	5.25	V
I_{CCA}	analog supply current		–	40	tbf	mA
I_{CCD}	digital supply current		–	22	tbf	mA
I_{CCO}	output supply current	f_{clk} = 4 MHz; f_i = 400 kHz	–	3.2	tbf	mA
ILE	integral non-linearity	f_{clk} = 4 MHz; f_i = 400 kHz	–	±3.0	±4.0	LSB
DLE	differential non-linearity	f_{clk} = 4 MHz; f_i = 400 kHz; no missing codes	–	±0.6	±1	LSB
$f_{clk(max)}$	maximum clock frequency					
	TDA8767H/1		10	–	–	MHz
	TDA8767H/2		20	–	–	MHz
	TDA8767H/3		30	–	–	MHz
P_{tot}	total power dissipation		–	335	–	mW

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			SAMPLING FREQUENCY (MHz)
	NAME	DESCRIPTION	VERSION	
TDA8767H/1	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2	10
TDA8767H/2				20
TDA8767H/3				30

BLOCK DIAGRAM

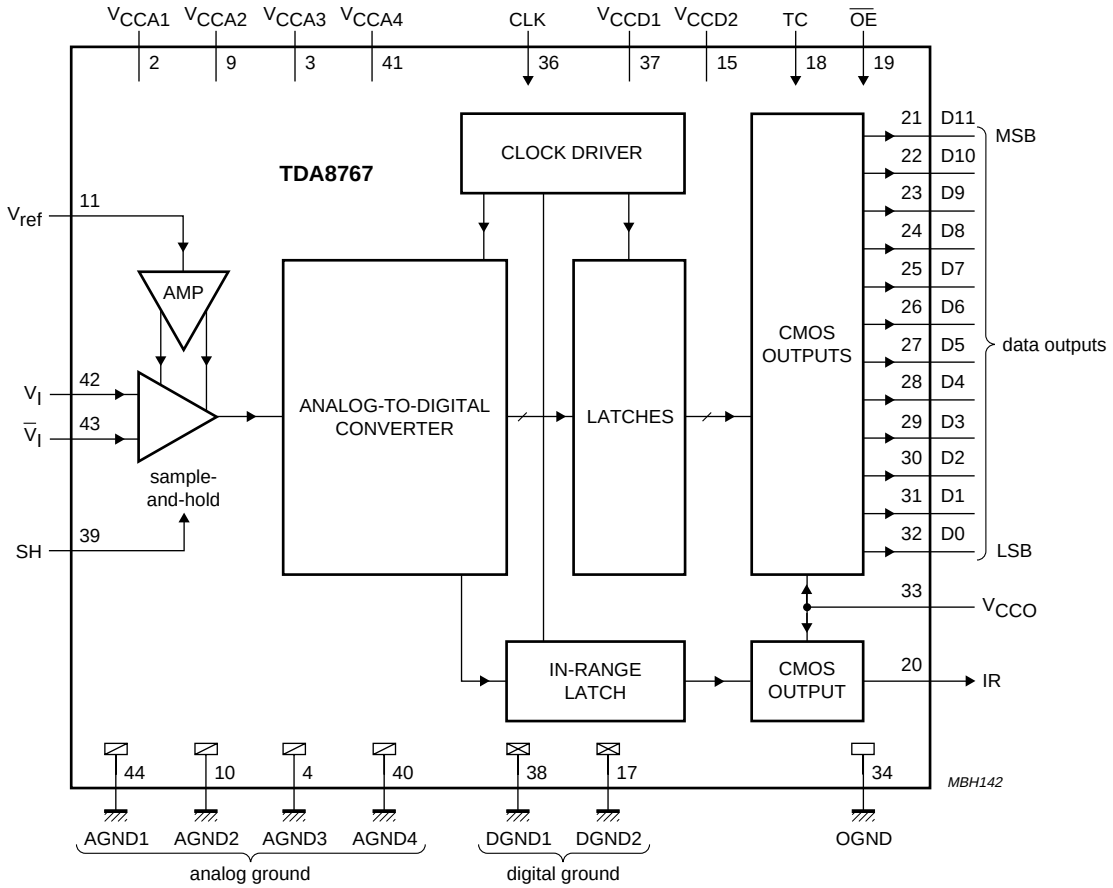


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
V_{CCA1}	2	analog supply voltage 1 (+5 V)
V_{CCA3}	3	analog supply voltage 3 (+5 V)
AGND3	4	analog ground 3
n.c.	5	not connected
n.c.	6	not connected
n.c.	7	not connected
n.c.	8	not connected
V_{CCA2}	9	analog supply voltage 2 (+5 V)
AGND2	10	analog ground 2
V_{ref}	11	reference voltage
n.c.	12	not connected
n.c.	13	not connected
n.c.	14	not connected
V_{CCD2}	15	digital supply voltage 2 (+5 V)
n.c.	16	not connected
DGND2	17	digital ground 2
TC	18	output two's complement
$\overline{OE}$	19	output enable input (CMOS level; active LOW)
IR	20	in-range output
D11	21	data output; bit 11 (MSB)
D10	22	data output; bit 10

SYMBOL	PIN	DESCRIPTION
D9	23	data output; bit 9
D8	24	data output; bit 8
D7	25	data output; bit 7
D6	26	data output; bit 6
D5	27	data output; bit 5
D4	28	data output; bit 4
D3	29	data output; bit 3
D2	30	data output; bit 2
D1	31	data output; bit 1
D0	32	data output; bit 0 (LSB)
V_{CCO}	33	output supply voltage (3 to 5.25 V)
OGND	34	output ground
n.c.	35	not connected
CLK	36	clock input
V_{CCD1}	37	digital supply voltage 1 (+5 V)
DGND1	38	digital ground 1
SH	39	sample-and-hold enable input (CMOS level; active HIGH)
AGND4	40	analog ground 4
V_{CCA4}	41	analog supply voltage 4 (+5 V)
V_I	42	complementary analog input voltage
$\overline{V}_I$	43	analog input voltage
AGND1	44	analog ground 1

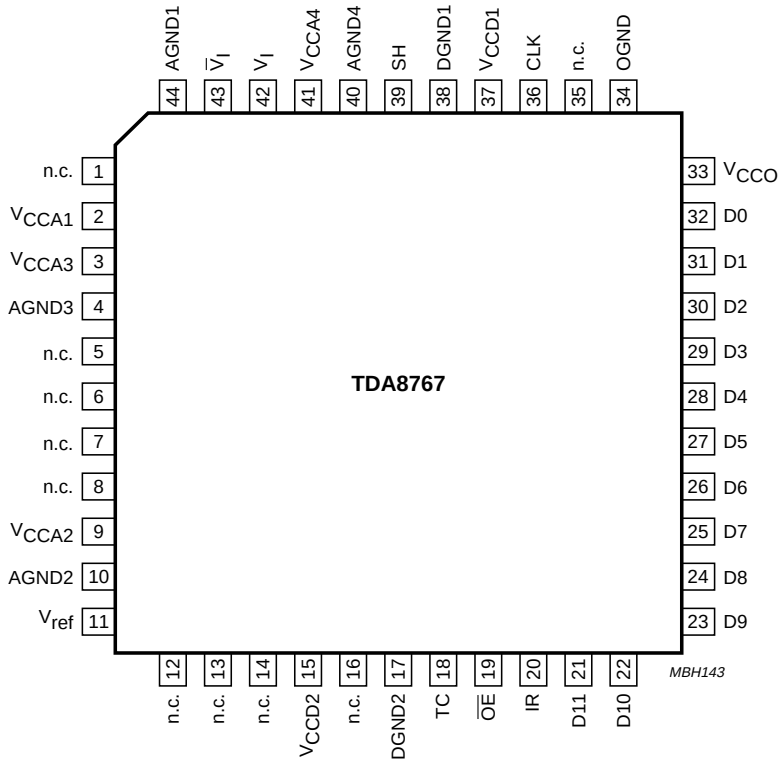


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage	note 1	–0.3	+7.0	V
V_{CCD}	digital supply voltage	note 1	–0.3	+7.0	V
V_{CCO}	output supply voltage	note 1	–0.3	+7.0	V
ΔV_{CC}	supply voltage difference				
	$V_{CCA} - V_{CCD}$		–1.0	+1.0	V
	$V_{CCO} - V_{CCD}$		–1.0	+4.0	V
	$V_{CCA} - V_{CCO}$		–1.0	+4.0	V
V_I	input voltage	referenced to AGND	0.3	V_{CCA}	V
$V_{i(p-p)}$	input voltage for differential clock drive (peak-to-peak value)		–	V_{CCD}	V
I_O	output current		–	10	mA
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		0	70	°C
T_j	junction temperature		–	+150	°C

Note

1. The supply voltages V_{CCA}, V_{CCD} and V_{CCO} may have any value between –0.3 V and +7.0 V provided that the supply voltage differences ΔV_{CC} are respected.

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE (TYP.)	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air	75	K/W

CHARACTERISTICS

V_{CCA} = V_2 to V_{44}, V_9 to V_{10}, V_3 to V_4 and V_{41} to V_{40} = 4.75 to 5.25 V; V_{CCD} = V_{37} to V_{38} and V_{15} to V_{17} = 4.75 to 5.25 V; V_{CCO} = V_{33} to V_{34} = 3.0 to 5.25 V; AGND and DGND shorted together; T_{amb} = 0 to +70 °C; typical values measured at V_{CCA} = V_{CCD} = 5 V and V_{CCO} = 3.3 V; $V_{i(p-p)} - \overline{V}_{i(p-p)}$ = 2.0 V; C_L = 15 pF and T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output supply voltage		3.0	3.3	5.25	V
I_{CCA}	analog supply current		–	40	tbf	mA
I_{CCD}	digital supply current		–	22	tbf	mA
I_{CCO}	output supply current	f_{clk} = 20 MHz; f_i = 4.43 MHz	–	12	tbf	mA
Inputs						
CLK (REFERENCED TO DGND)						
V_{IL}	LOW-level input voltage		0	–	0.8	V
V_{IH}	HIGH-level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW-level input current	V_{clk} = 0.3V_{CCD}	–400	–	–	µA
I_{IH}	HIGH-level input current	V_{clk} = 0.7V_{CCD}	–	–	100	µA
		V_{clk} = V_{CCD}	–	–	300	µA
Z_i	input impedance	f_{clk} = 30 MHz	–	2	–	kΩ
C_i	input capacitance	f_{clk} = 30 MHz	–	2	–	pF
TC; SH AND $\overline{OE}$ (REFERENCED TO DGND); see Tables 3 and 4						
V_{IL}	LOW-level input voltage		0	–	0.8	V
V_{IH}	HIGH-level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW-level input current	V_{IL} = 0.3V_{CCD}	–400	–	–	µA
I_{IH}	HIGH-level input current	V_{IH} = 0.7V_{CCD}	–	–	20	µA
V_I AND $\overline{V}_I$ (REFERENCED TO AGND; see Tables 1 AND 2); V_{ref} = V_{CCA} – 2 V						
I_{IL}	LOW-level input current	V_i = $\overline{V}_i$	–	10	–	µA
I_{IH}	HIGH-level input current	V_i = $\overline{V}_i$	–	10	–	µA
Z_i	input impedance	f_i = 4.43 MHz	–	10	–	kΩ
C_i	input capacitance	f_i = 4.43 MHz	–	2	–	pF
$V_{ios(d)}$	input offset voltage in differential mode	V_I = $\overline{V}_I$; output code 2047				
		V_{CCA} = 5 V	tbf	2.5	tbf	V
		V_{CCA} = 4.75 V	tbf	2.25	tbf	V
		V_{CCA} = 5.25 V	tbf	2.75	tbf	V
$V_{ios(s)}$	input offset voltage in single mode	V_I = $V_{ios(s)}$; output code 2047				
		V_{CCA} = 5 V	tbf	2.5	tbf	V
		V_{CCA} = 4.75 V	tbf	2.25	tbf	V
		V_{CCA} = 5.25 V	tbf	2.75	tbf	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Voltage controlled regulator input V_{ref} (referenced to V_{CCA})						
$V_{ref(FS)}$	full scale fixed voltage	V_{CCA} = 5 V	–	3.175	–	V
$V_{i(p-p)} - \overline{V}_{i(p-p)}$	input voltage amplitude (peak-to-peak value)	differential mode	–	2.0	–	V
		single mode; $\overline{V}_i$ = 2.5 V	–	2.0	–	V
I_{ref}	input current at V_{ref}		–	10	–	μA
Outputs (referenced to DGND)						
DIGITAL OUTPUTS D11 TO D0 AND IR (REFERENCED TO DGND)						
V_{OL}	LOW-level output voltage	I_{OL} = 2 mA	0	–	0.5	V
V_{OH}	HIGH-level output voltage	I_{OH} = –0.4 mA	V_{CCO} – 0.5	–	V_{CCD}	V
I_O	output current in 3-state	0.5 V < V_O < V_{CCO}	–20	–	+20	μA
Switching characteristics						
CLOCK FREQUENCY f_{clk} (see Fig.3)						
$f_{clk(min)}$	minimum clock frequency	SH = HIGH	–	–	1	MHz
		SH = LOW	–	–	1	kHz
$f_{clk(max)}$	maximum clock frequency					
	TDA8767H/1		10	–	–	MHz
	TDA8767H/2		20	–	–	MHz
	TDA8767H/3		30	–	–	MHz
t_{CPH}	clock pulse width HIGH		8.5	–	–	ns
t_{CPL}	clock pulse width LOW		8.5	–	–	ns
Analog signal processing; 50% clock duty factor; $V_i - \overline{V}_i$ = 2.0 V; $V_{ref} = V_{CCA} - 2$ V; see Table 1						
LINEARITY						
ILE	integral non-linearity	f_{clk} = 4 MHz; ramp input	–	±3.0	±4.0	LSB
DLE	differential non-linearity	f_{clk} = 4 MHz; ramp input; no missing codes	–	±0.6	±1	LSB
OFER	offset error	$V_{CCA} = V_{CCD} = V_{CCO}$ = 5 V; T_{amb} = 25 °C; $V_i = \overline{V}_i$; output code = 2047	tbf	–	tbf	LSB
GER	gain error amplitude; spread from device to device	$V_{CCA} = V_{CCD} = V_{CCO}$ = 5 V; T_{amb} = 25 °C; $V_i - \overline{V}_i$ = 2.0 V	tbf	–	tbf	LSB
BANDWIDTH (f_{clk} = 30 MHz); note 1						
B	analog bandwidth	–1 dB	–	9	–	MHz
		–3 dB	–	18	–	MHz
t_{STLH}	analog input settling time LOW-to-HIGH transition	full scale square wave; note 3	–	tbf	–	ns
t_{STHL}	analog input settling time HICH-to-LOW transition	full scale square wave; note 3	–	tbf	–	ns
HARMONICS						
THD	total harmonic distortion	f_{clk} = 30 MHz; f_i = 4.43 MHz; note 2	–	–64	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SIGNAL-TO-NOISE RATIO						
S/N	signal-to-noise ratio	without harmonics; f_{clk} = 30 MHz; f_i = 4.43 MHz	–	61	–	dB
Timing (C_L = 15 pF); note 4; see Fig.3						
t_{ds}	sampling delay time		–	–	2	ns
t_h	output hold time		8	–	–	ns
t_d	output delay time	V_{CCO} = 4.75 V	–	12	15	ns
		V_{CCO} = 3.15 V		15	18	ns
3-state output delay times; see Fig.4						
t_{dZH}	enable HIGH		–	14	18	ns
t_{dZL}	enable LOW		–	16	20	ns
t_{dHZ}	disable HIGH		–	16	20	ns
t_{dLZ}	disable LOW		–	14	18	ns

Notes to the characteristics

1. The –3 dB (or –1 dB) analog bandwidth is determined by the 3 dB (or 1 dB) reduction in the reconstructed output, the input being a full-scale sine wave.
2. THD (total harmonic distortion) is obtained with the addition of the first five harmonics:

$$THD = 20 \log \frac{F}{\sqrt{(2nd)^2 + (3rd)^2 + (4th)^2 + (5th)^2 + (6th)^2}}$$

   F being the fundamental harmonic referenced at 0 dB for a full-scale sine wave input.
3. The analog input settling time is the minimum time required for the input signal to be stabilized after a sharp full-scale input (square wave signal) in order to sample the signal and obtain correct output data (see Fig.5).
4. Output data acquisition: the output data is available after the maximum delay of t_d.

Table 1 Output coding with differential inputs (typical values to AGND); $V_{I(p-p)} - \overline{V}_{I(p-p)}$ = 2.0 V; $V_{ref} = V_{CCA} - 2$ V

CODE	V_I	$\overline{V}_I$	IR	BINARY OUTPUTS	TWO'S COMPLEMENT OUTPUTS
				D11 to D0	D11 to D0
underflow	<2.0	>3.0	0	0 0 0 0 0 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0 0 0 0 0
0	2.0	3.0	1	0 0 0 0 0 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0 0 0 0 0
1	–	–	1	0 0 0 0 0 0 0 0 0 0 0 1	1 0 0 0 0 0 0 0 0 0 0 1
↓	–	–	↓	↓	↓
2047	2.5	2.5	1	0 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1
↓	–	–	↓	↓	↓
4094	–	–	1	1 1 1 1 1 1 1 1 1 1 1 0	0 1 1 1 1 1 1 1 1 1 1 0
4095	3.0	2.0	1	1 1 1 1 1 1 1 1 1 1 1 1	0 1 1 1 1 1 1 1 1 1 1 1
overflow	>3.0	<2.0	0	1 1 1 1 1 1 1 1 1 1 1 1	0 1 1 1 1 1 1 1 1 1 1 1

Table 2 Output coding with single input (typical values to AGND); V_{FS} = 2.0 V (p-p); $V_{ref} = V_{CCA} - 2$ V

CODE	V_I	IR	BINARY OUTPUTS	TWO'S COMPLEMENT OUTPUTS
			D11 to D0	D11 to D0
underflow	<1.5	0	0 0 0 0 0 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0 0 0 0 0
0	1.5	1	0 0 0 0 0 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0 0 0 0 0
1	–	1	0 0 0 0 0 0 0 0 0 0 0 1	1 0 0 0 0 0 0 0 0 0 0 1
↓	–	↓	↓	↓
2047	2.5	1	0 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1
↓	–	↓	↓	↓
4094	–	1	1 1 1 1 1 1 1 1 1 1 1 0	0 1 1 1 1 1 1 1 1 1 1 0
4095	3.5	1	1 1 1 1 1 1 1 1 1 1 1 1	0 1 1 1 1 1 1 1 1 1 1 1
overflow	>3.5	0	1 1 1 1 1 1 1 1 1 1 1 1	0 1 1 1 1 1 1 1 1 1 1 1

Table 3 Mode selection

TC	$\overline{OE}$	D0 to D11 and IR
0	0	binary; active
1	0	two's complement; active
X[1]	1	high impedance

Note

1. Where: X = don't care.

Table 4 Sample-and-hold selection

SH	SAMPLE-AND-HOLD
1	active
0	inactive; tracking mode

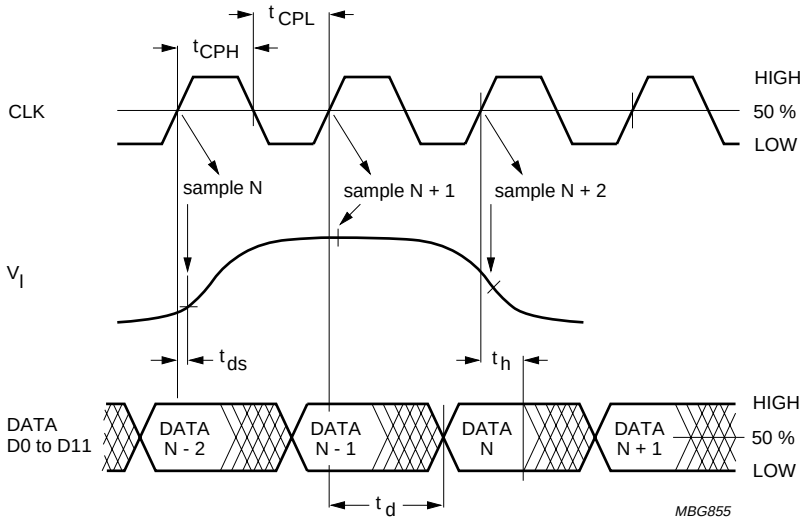
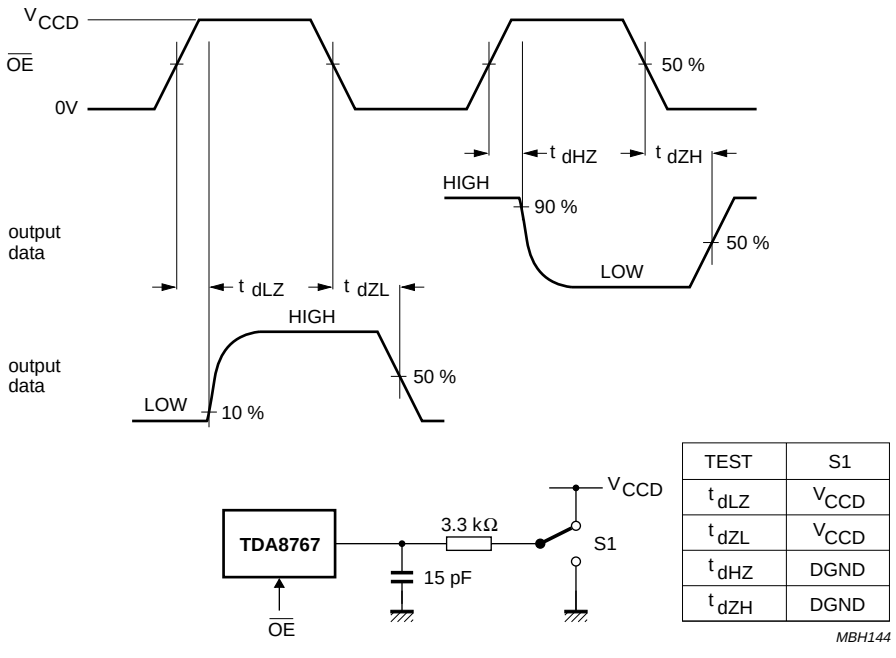


Fig.3 Timing diagram.



$f_{\overline{OE}}$ = 100 kHz.

Fig.4 Timing diagram and test conditions of 3-state output delay time.

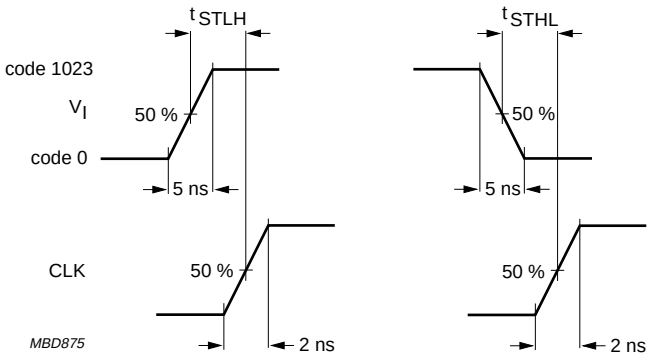
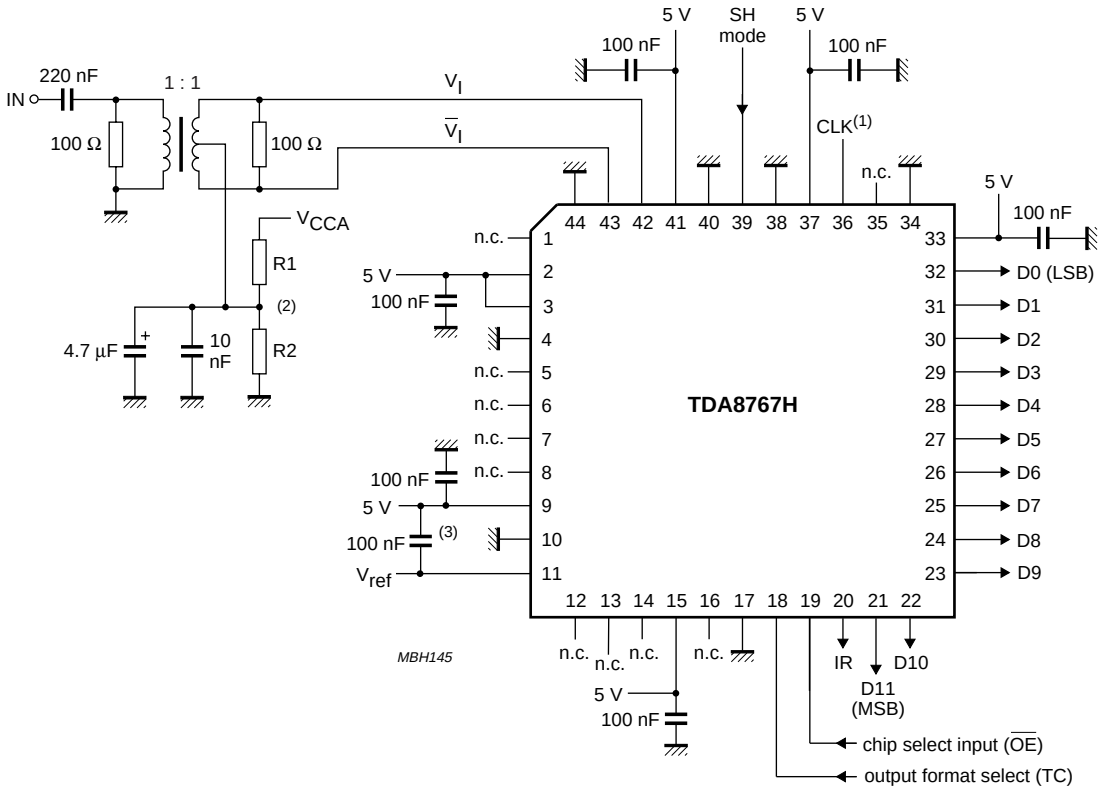


Fig.5 Analog input settling time diagram.

APPLICATION INFORMATION



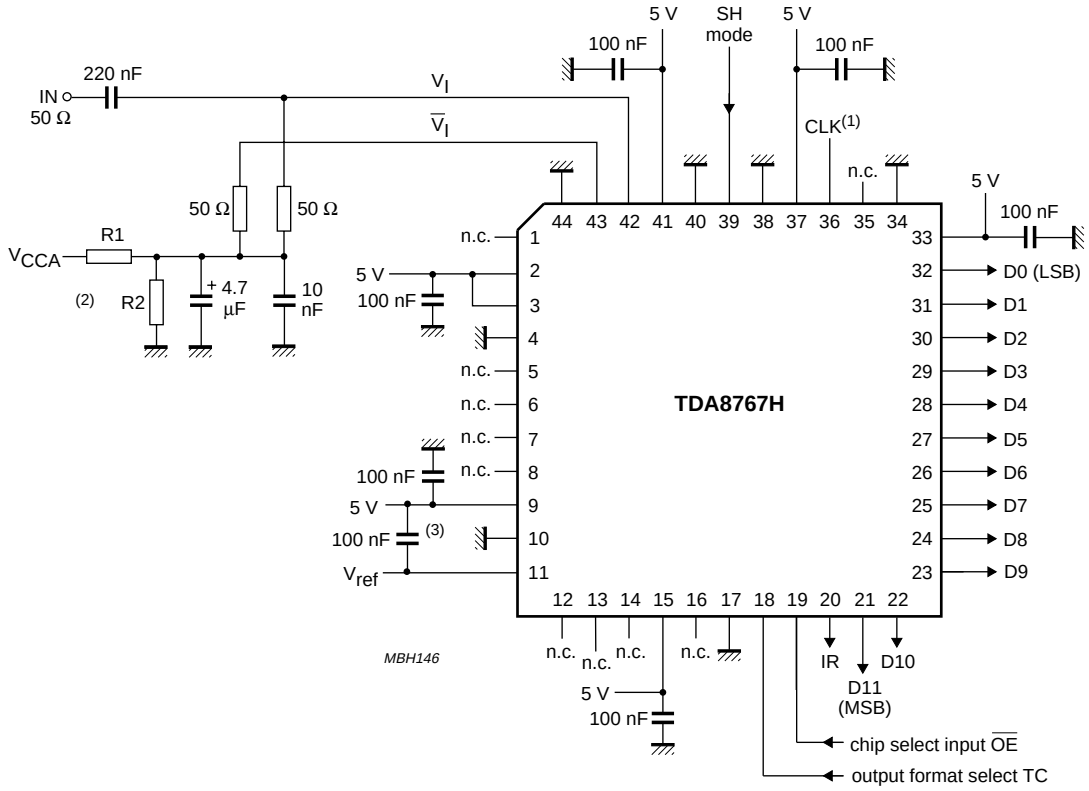
The analog, digital and output supplies should be separated and decoupled.

(1) At power-up a high level clock must be provided within less than 1 µs or a pull-up resistor must be connected between CLK and V_{CCD}.

(2) R1, and R2 must be determined in order to obtain a middle voltage of 2.5 V; see Table 1. To ensure a sufficient analog input stability, the minimum current into these resistors must be about 1 mA.

(3) V_{ref} must be decoupled to V_{CCA}.

Fig.6 Application diagram (differential input mode).



The analog, digital and output supplies should be separated and decoupled.

(1) At power-up a high level clock must be provided within less than 1 µs or a pull-up resistor must be connected between CLK and V_{CCD}.

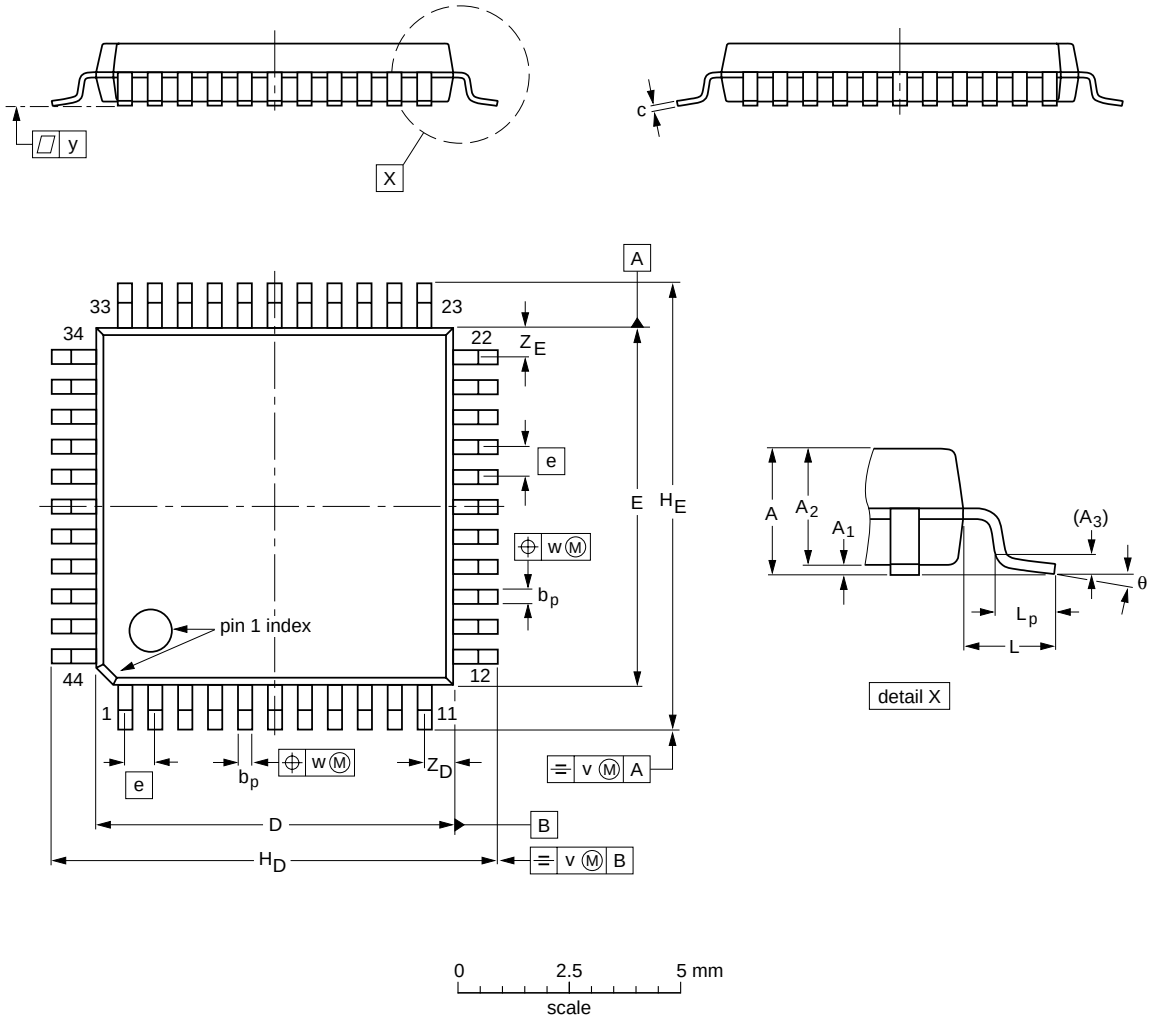
(2) R1, and R2 must be determined in order to obtain a voltage of 2.5 V on V_I and $\overline{V}_I$; see Table 1. To ensure a sufficient analog input stability, the minimum current into these resistors must be about 1 mA.

(3) V_{ref} must be decoupled to V_{CCA}.

Fig.7 Application diagram (single input mode).

PACKAGE OUTLINE

QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm **SOT307-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.10	0.25 0.05	1.85 1.65	0.25	0.40 0.20	0.25 0.14	10.1 9.9	10.1 9.9	0.8	12.9 12.3	12.9 12.3	1.3	0.95 0.55	0.15	0.15	0.1	1.2 0.8	1.2 0.8	10^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT307-2						~~95-02-04~~ 97-08-01

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

NOTES

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Printed in The Netherlands 545004/750/03/pp20 Date of release: 1999 Feb 16 Document order number: 9397 750 04713

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