



MOTOROLA

DESCRIPTION — The SN54LS/74LS682 thru SN54LS/74LS689 are 8-bit magnitude comparators. These device types are designed to perform comparisons between two eight-bit binary or BCD words. All device types provide $\overline{P} = \overline{Q}$ outputs and the LS682 thru LS687 have $\overline{P} > \overline{Q}$ outputs also.

The LS682, LS684, LS686 and LS688 are totem pole devices. The LS683, LS685, LS687 and LS689 are open-collector devices.

The LS682 and LS683 have a 20 kΩ pullup resistor on the Q inputs for analog or switch data.

加急出货

**SN54LS/74LS682
thru
SN54LS/74LS689**

**8-BIT MAGNITUDE
COMPARATORS**

LOW POWER SCHOTTKY

FUNCTION TABLE

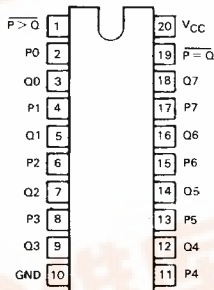
INPUTS			OUTPUTS	
DATA	ENABLES		$\overline{P} = \overline{Q}$	$\overline{P} > \overline{Q}$
P, Q	$\overline{G}, \overline{G}_1$	$\overline{G}_2$		
$P = Q$	L	L	L	H
$P > Q$	L	L	H	L
$P < Q$	L	L	H	H
X	H	H	H	H

H = high level, L = low level, X = irrelevant

TYPE	$\overline{P} = \overline{Q}$	$\overline{P} > \overline{Q}$	OUTPUT ENABLE	OUTPUT CONFIGURATION	PULLUP
LS682	yes	yes	no	totem-pole	yes
LS683	yes	yes	no	open-collector	yes
LS684	yes	yes	no	totem-pole	no
LS685	yes	yes	nc	open-collector	no
LS686	yes	yes	yes	totem-pole	no
LS687	yes	yes	yes	open-collector	no
LS688	yes	no	yes	totem-pole	no
LS689	yes	no	yes	open-collector	no

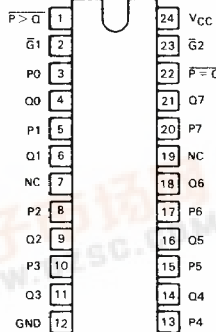
**CONNECTION DIAGRAMS
(TOP VIEW)**

**SN54LS/74LS682
THRU
SN54LS/74LS685**



J Suffix — Case 732-03 (Ceramic)
N Suffix — Case 738-01 (Plastic)

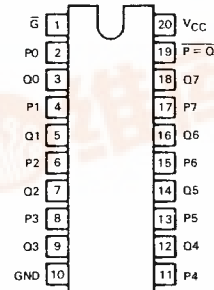
**SN54LS/74LS686
SN54LS/74LS687**



NC = no connection

J Suffix — Case 758-01 (Ceramic)
N Suffix — Case 724-02 (Plastic)

**SN54LS/74LS688
SN54LS/74LS689**



J Suffix — Case 732-03 (Ceramic)
N Suffix — Case 738-01 (Plastic)



SN54LS/74LS682 • SN54LS/74LS684
SN54LS/74LS686 • SN54LS/74LS688

GUARANTEED OPERATING RANGES

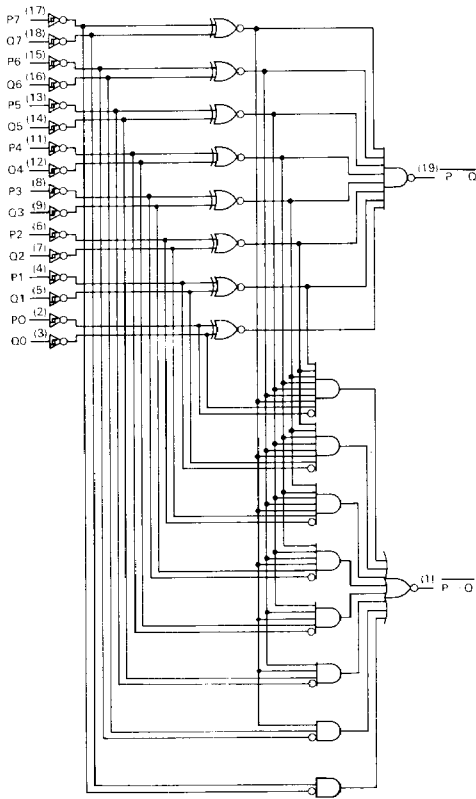
SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54,74			-0.4	mA
I _{OL}	Output Current — Low	54 74			12 24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

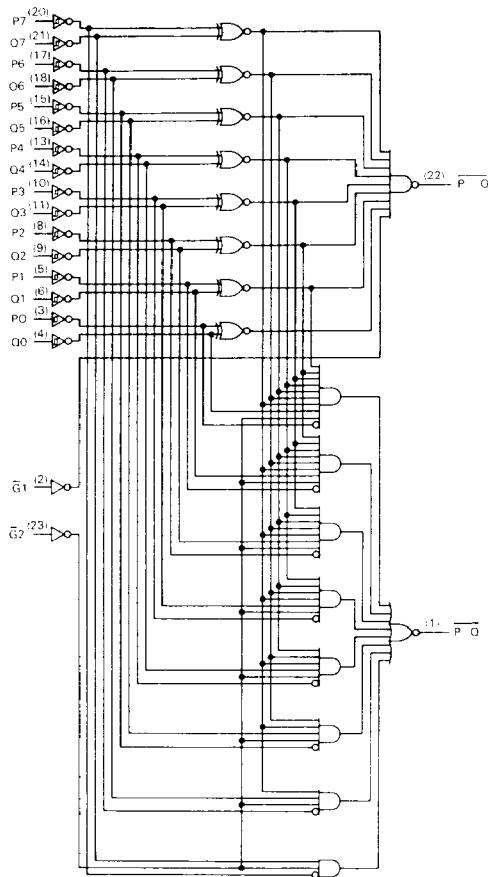
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74		0.8		
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54	2.5	3.5	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table
		74	2.7	3.5	V	
V _{OL}	Output LOW Voltage	54,74		0.25	V	I _{OL} = 12 mA V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	V	I _{OL} = 24 mA
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
		LS682-Q Inputs		0.1	mA	V _{CC} = MAX, V _{IN} = 5.5 V
		Others		0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current	LS682-Q Inputs		-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V
		Others		-0.2	mA	
I _{OS}	Short Circuit Current		-30	-130	mA	V _{CC} = MAX
I _{CC}	Power Supply Current	LS682		70	mA	V _{CC} = MAX
		LS684		65	mA	
		LS686		75	mA	
		LS688		65	mA	

SN54LS/74LS683 • SN54LS/74LS685
 SN54LS/74LS687 • SN54LS/74LS689

BLOCK DIAGRAMS



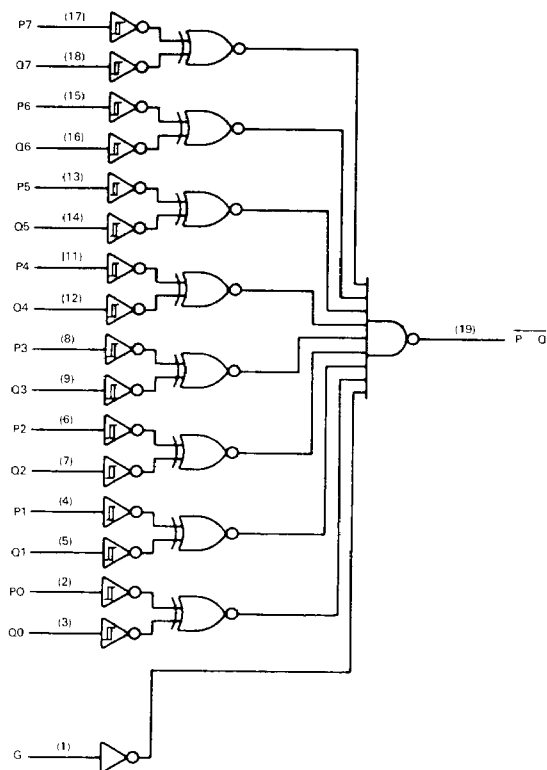
SN54LS/74LS682 thru LS685



SN54LS/74LS686, LS687

SN54LS/74LS683 • SN54LS/74LS685
 SN54LS/74LS687 • SN54LS/74LS689

BLOCK DIAGRAM



SN54LS/74LS688, LS689

SN54LS/74LS683 • SN54LS/74LS685
SN54LS/74LS687 • SN54LS/74LS689

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
V _{OH}	Output Voltage — High	54,74			5.5	V
I _{OL}	Output Current — Low	54 74			12 24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS
			MIN	TYP	MAX		
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V _{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V _{IK}	Input Clamp Diode Voltage			-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA
I _{OH}	Output HIGH Current	54			250	μA	V _{CC} = MIN, V _{OH} = MAX
		74			100	μA	
V _{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I _{OL} = 12 mA, V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	I _{OL} = 24 mA
I _{IH}	Input HIGH Current				20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
		LS683-Q Inputs			0.1	mA	V _{CC} = MAX, V _{IN} = 5.5 V
		Others			0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current	LS683-Q Inputs			-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V
		Others			-0.2	mA	
I _{CC}	Power Supply Current	LS683			70	mA	V _{CC} = MAX
		LS685			65	mA	
		LS687			75	mA	
		LS689			65	mA	

SN54LS/74LS682 THRU SN54LS/74LS685

AC CHARACTERISTICS: $T_A = 25^\circ\text{C}$

SN54LS/74LS682

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t _{PLH} t _{PHL}	Propagation Delay, P to $\overline{P} = \overline{Q}$		13 15	25 25	ns	$V_{CC} = 5.0\text{ V}$ $C_L = 45\text{ pF}$ $R_L = 667\ \Omega$
t _{PLH} t _{PHL}	Propagation Delay, Q to $\overline{P} = \overline{Q}$		14 15	25 25	ns	
t _{PLH} t _{PHL}	Propagation Delay, P to $\overline{P} > \overline{Q}$		20 15	30 30	ns	
t _{PLH} t _{PHL}	Propagation Delay, Q to $\overline{P} > \overline{Q}$		21 19	30 30	ns	

SN54LS/74LS683

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t _{PLH} t _{PHL}	Propagation Delay, P to $\overline{P} = \overline{Q}$		30 20	45 30	ns	$V_{CC} = 5.0\text{ V}$ $C_L = 45\text{ pF}$ $R_L = 667\ \Omega$
t _{PLH} t _{PHL}	Propagation Delay, Q to $\overline{P} = \overline{Q}$		24 23	35 35	ns	
t _{PLH} t _{PHL}	Propagation Delay, P to $\overline{P} > \overline{Q}$		31 17	45 30	ns	
t _{PLH} t _{PHL}	Propagation Delay, Q to $\overline{P} > \overline{Q}$		30 21	45 30	ns	

SN54LS/74LS684

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t _{PLH} t _{PHL}	Propagation Delay, P to $\overline{P} = \overline{Q}$		15 17	25 25	ns	$V_{CC} = 5.0\text{ V}$ $C_L = 45\text{ pF}$ $R_L = 667\ \Omega$
t _{PLH} t _{PHL}	Propagation Delay, Q to $\overline{P} = \overline{Q}$		16 15	25 25	ns	
t _{PLH} t _{PHL}	Propagation Delay, P to $\overline{P} > \overline{Q}$		22 17	30 30	ns	
t _{PLH} t _{PHL}	Propagation Delay, Q to $\overline{P} > \overline{Q}$		24 20	30 30	ns	

SN54LS/74LS685

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t _{PLH} t _{PHL}	Propagation Delay, P to $\overline{P} = \overline{Q}$		30 19	45 35	ns	$V_{CC} = 5.0\text{ V}$ $C_L = 45\text{ pF}$ $R_L = 667\ \Omega$
t _{PLH} t _{PHL}	Propagation Delay, Q to $\overline{P} = \overline{Q}$		24 23	45 35	ns	
t _{PLH} t _{PHL}	Propagation Delay, P to $\overline{P} > \overline{Q}$		32 16	45 35	ns	
t _{PLH} t _{PHL}	Propagation Delay, Q to $\overline{P} > \overline{Q}$		30 20	45 35	ns	

SN54LS/74LS686 • SN54LS/74LS687
SN54LS/74LS688 • SN54LS/74LS689

AC CHARACTERISTICS: $T_A = 25^\circ\text{C}$

SN54LS/74LS686

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, P to $\overline{P} = \overline{Q}$		13 20	25 30	ns	$V_{CC} = 5.0\text{ V}$ $C_L = 45\text{ pF}$ $R_L = 667\ \Omega$
t_{PLH} t_{PHL}	Propagation Delay, Q to $\overline{P} = \overline{Q}$		13 21	25 30	ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{G}$, $\overline{G1}$ to $\overline{P} = \overline{Q}$		11 19	20 30	ns	
t_{PLH} t_{PHL}	Propagation Delay, P to $\overline{P} > \overline{Q}$		19 15	30 30	ns	
t_{PLH} t_{PHL}	Propagation Delay, Q to $\overline{P} > \overline{Q}$		18 19	30 30	ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{G2}$ to $\overline{P} > \overline{Q}$		21 16	30 25	ns	

SN54LS/74LS687

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, P to $\overline{P} = \overline{Q}$		24 20	35 30	ns	$V_{CC} = 5.0\text{ V}$ $C_L = 45\text{ pF}$ $R_L = 667\ \Omega$
t_{PLH} t_{PHL}	Propagation Delay, Q to $\overline{P} = \overline{Q}$		24 20	35 30	ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{G}$, $\overline{G1}$ to $\overline{P} = \overline{Q}$		21 18	35 30	ns	
t_{PLH} t_{PHL}	Propagation Delay, P to $\overline{P} > \overline{Q}$		24 16	35 30	ns	
t_{PLH} t_{PHL}	Propagation Delay, Q to $\overline{P} > \overline{Q}$		24 16	35 30	ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{G2}$ to $\overline{P} > \overline{Q}$		24 15	35 30	ns	

SN54LS/74LS688

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, P to $\overline{P} = \overline{Q}$		12 17	18 23	ns	$V_{CC} = 5.0\text{ V}$ $C_L = 45\text{ pF}$ $R_L = 667\ \Omega$
t_{PLH} t_{PHL}	Propagation Delay, Q to $\overline{P} = \overline{Q}$		12 17	18 23	ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{G}$, $\overline{G1}$ to $\overline{P} = \overline{Q}$		12 13	18 20	ns	

SN54LS/74LS689

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, P to $\overline{P} = \overline{Q}$		24 22	40 35	ns	$V_{CC} = 5.0\text{ V}$ $C_L = 45\text{ pF}$ $R_L = 667\ \Omega$
t_{PLH} t_{PHL}	Propagation Delay, Q to $\overline{P} = \overline{Q}$		24 22	40 35	ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{G}$, $\overline{G1}$ to $\overline{P} = \overline{Q}$		22 19	35 30	ns	