CY7C168A

4Kx4 RAM

Features

- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **High speed**
  - **— t_{AA} = 15 ns**
- **Low active power**
  - **— 633 mW**
- **Low standby power**
  - **— 110 mW**
- **TTL-compatible inputs and outputs**
- **V_{IH} of 2.2V**
- **Capable of withstanding greater than 2001V electrostatic discharge**

Functional Description

The CY7C168A is a high-performance CMOS static RAM organized as 4096 by 4 bits. Easy memory expansion is provided by an active LOW Chip Enable ($\overline{CE}$) and three-state drivers. The CY7C168A has an automatic power-down feature, reducing the power consumption by 77% when deselected.

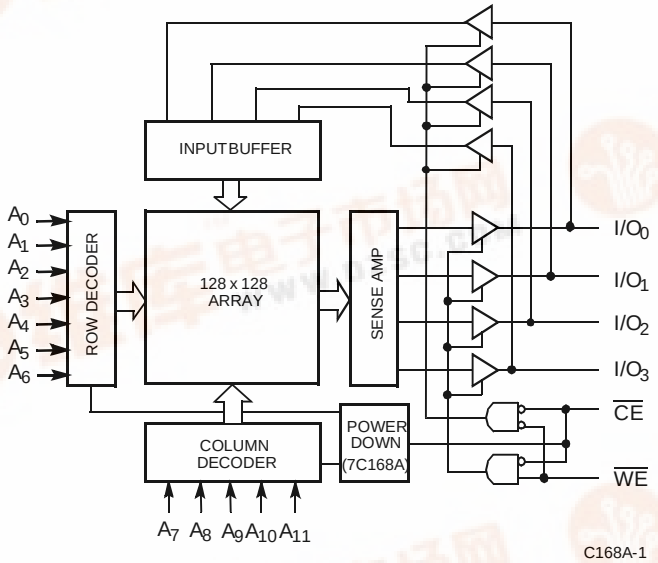
Writing to the device is accomplished when the Chip Select ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs are both LOW. Data on the four data input/output pins (I/O_0 through I/O_3) is written into the memory location specified on the address pins (A_0 through A_{11}).

Reading the device is accomplished by taking the Chip Enable ($\overline{CE}$) LOW, while Write Enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the location specified on the address pins will appear on the four data input/output pins (I/O_0 through I/O_3).

The input/output pins remain in a high-impedance state when Chip Enable ($\overline{CE}$) is HIGH or Write Enable ($\overline{WE}$) is LOW.

A die coat is used to insure alpha immunity.

Logic Block Diagram



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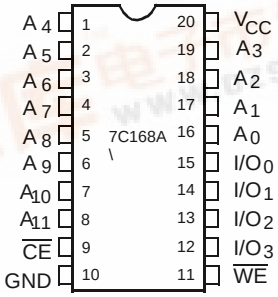
Pin Configurations

DIP/SOJ
Top View



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Selection Guide

		7C168A-15	7C168A-20	7C168A-25	7C168A-35	7C168A-45
Maximum Access Time (ns)		15	20	25	35	45
Maximum Operating Current (mA)	Commercial	115	90	90	90	90
	Military	-	100	100	100	100

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage to Ground Potential (Pin 20 to Pin 10)..... –0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State..... –0.5V to +7.0V

DC Input Voltage .....–3.0V to +7.0V

Output Current into Outputs (Low) ..... 20 mA

Static Discharge Voltage .....>2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[1]	–55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions		7C168A-15		7C168A-20		Unit
				Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[3]			–0.5	0.8	–0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		–10	+10	–10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		–10	+10	–10	+10	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			–350		–350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		115		90	mA
			Mil		-		100	
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}	Com'l		40		40	mA
			Mil		-		40	
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3V	Com'l		20		20	mA
			Mil		-		20	

Notes:
1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. V_{IL} min. = –3.0V for pulse durations less than 30 ns.
4. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

Electrical Characteristics Over the Operating Range[2] (continued)

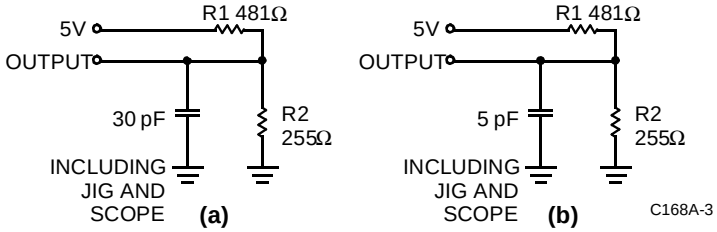
Parameter	Description	Test Conditions		7C168A-25		7C168A-35		7C168A-45		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[3]			–0.5	0.8	–0.5	0.8	–0.5	0.8	V
I_{IX}	Input Load Current	$GND \le V_I \le V_{CC}$		–10	+10	–10	10	–10	10	µA
I_{OZ}	Output Leakage Current	$GND \le V_O \le V_{CC}$ Output Disabled		–10	+10	–50	50	–50	50	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			–350		–350		–350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		90		90		90	mA
			Mil		100		100		100	
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current	Max. V_{CC}, $\overline{CE} \ge V_{IH}$	Com'l		20		20		20	mA
			Mil		20		20		20	
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current	Max. V_{CC}, $\overline{CE} \ge$ VCC – 0.3 V	Com'l		20		20		20	mA
			Mil		20		20		20	

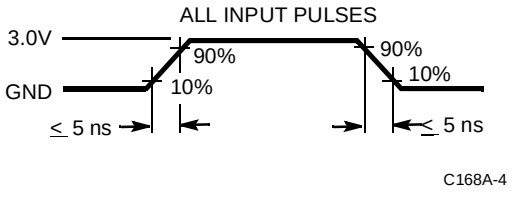
Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

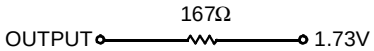
Note:
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT

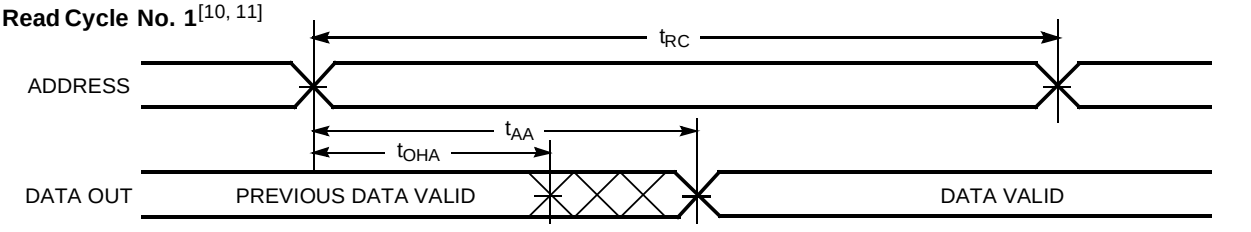


Switching Characteristics Over the Operating Range[2,6]

Parameter	Description	7C168A-15		7C168A-20		7C168A-25		7C168A-35		7C168A-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	15		20		25		35		45		ns
t_{AA}	Address to Data Valid		15		20		25		35		45	ns
t_{OHA}	Output Hold from Address Change	5		5		5		5		5		ns
t_{ACE}	Power Supply Current		15		20		25		35		45	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[7]	5		5		5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[7, 8]		8		8		10		15		15	ns
t_{PU}	$\overline{CE}$ LOW to Power Up	0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		15		20		20		20		25	ns
t_{RCS}	Read Command Set-Up	0		0		0		0		0		ns
t_{RCH}	Read Command Hold	0		0		0		0		0		ns
WRITE CYCLE[9]												
t_{WC}	Write Cycle Time	15		20		20		25		40		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	12		15		20		25		30		ns
t_{AW}	Address Set-Up to Write End	12		15		20		25		30		ns
t_{HA}	Address Hold from Write End	0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	12		15		15		20		20		ns
t_{SD}	Data Set-Up to Write End	10		10		10		15		15		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[7]	7		7		7		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7, 8]	5		5		5		5		10		ns

Switching Waveforms

Read Cycle No. 1[10, 11]



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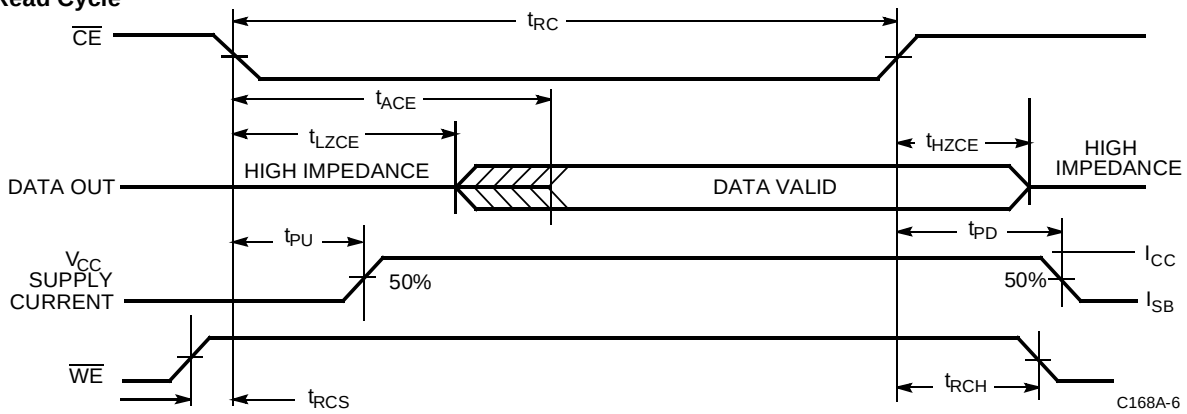
Notes:

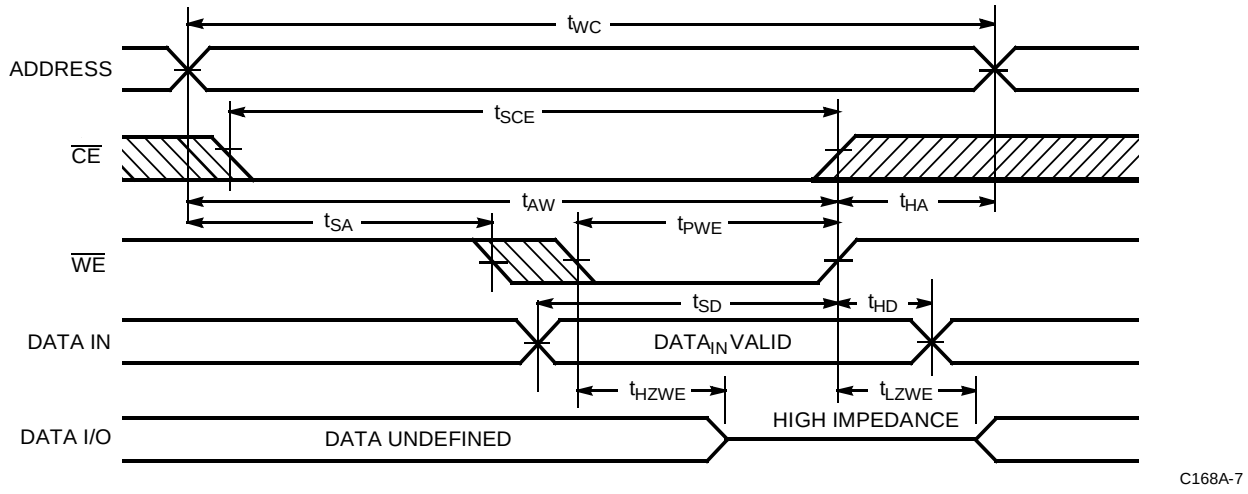
6. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
7. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for all devices. Transition is measured ±500 mV from steady state voltage with specified loading in part (b) of AC Test Loads and Waveforms.
8. t_{HZCE} and t_{HZWE} are tested with C_L = 5 pF as in part (a) of Test Loads and Waveforms. Transition is measured ±500 mV from steady state voltage.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signal must be LOW to initiate a write and either signal can terminate a write by going high. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
10. $\overline{WE}$ is HIGH for read cycle.
11. Device is continuously selected, $\overline{CE} = V_{IL}$.

Switching Waveforms (continued)

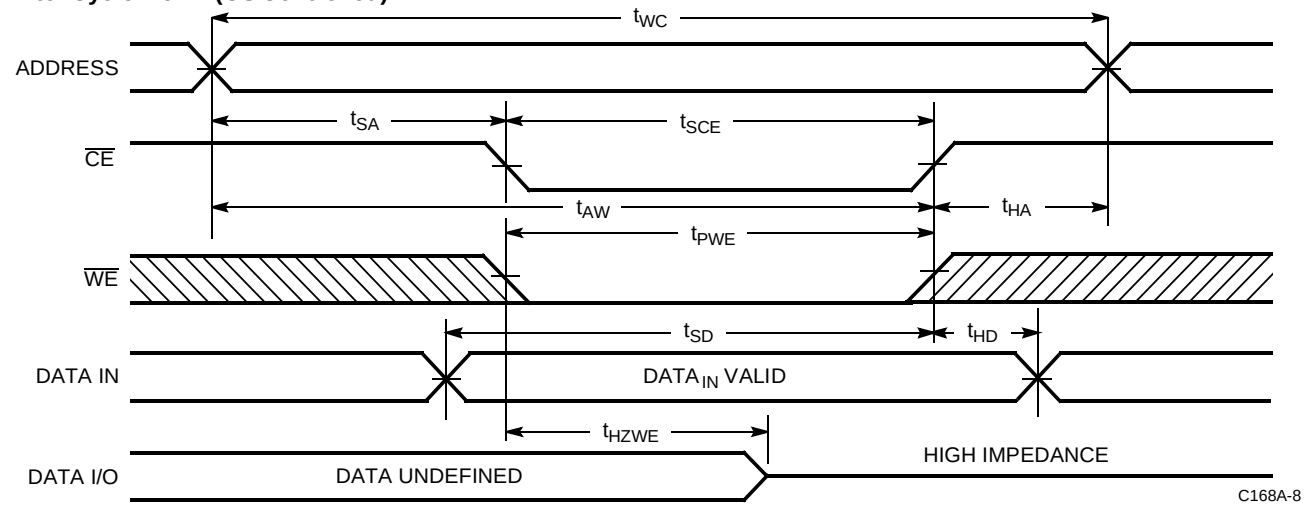
Read Cycle [10, 12]



Write Cycle No. 1 ($\overline{WE}$ Controlled) [9]



Write Cycle No. 2 ($\overline{CS}$ Controlled) [9, 13]

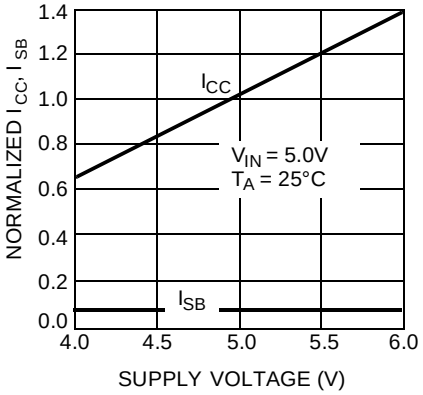


Notes:

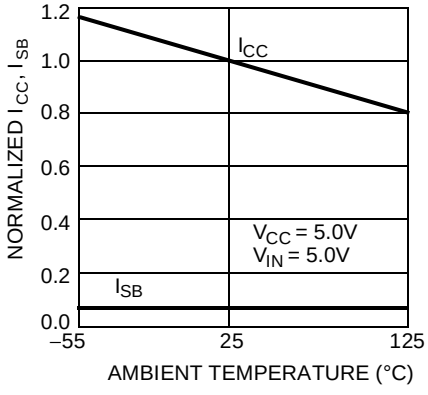
12. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
13. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Typical DC and AC Characteristics

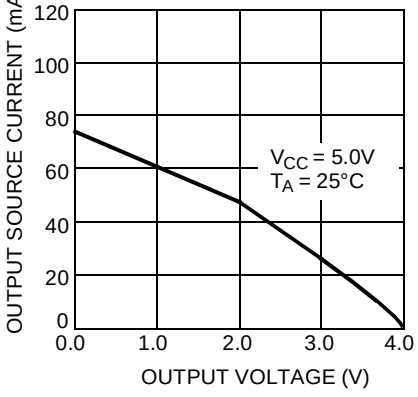
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



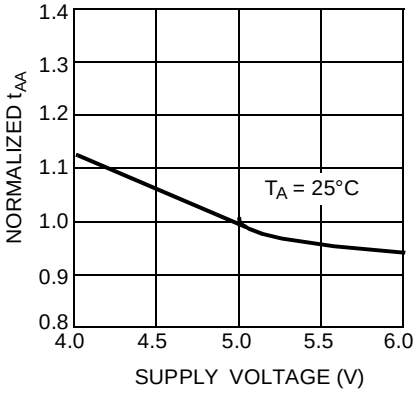
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



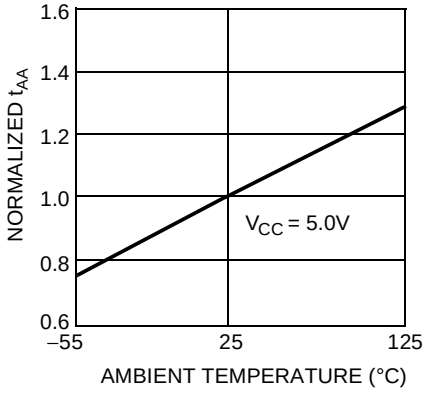
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



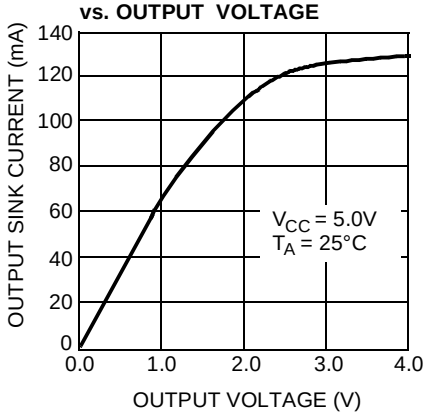
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



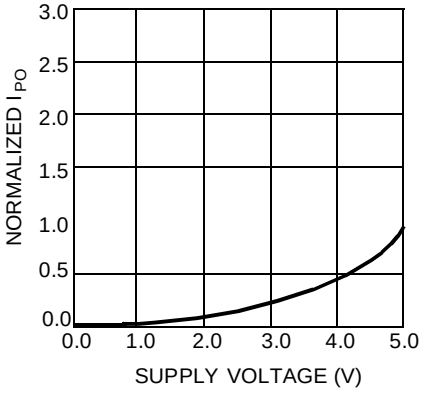
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



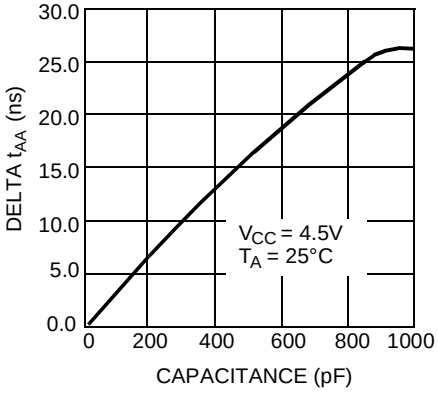
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



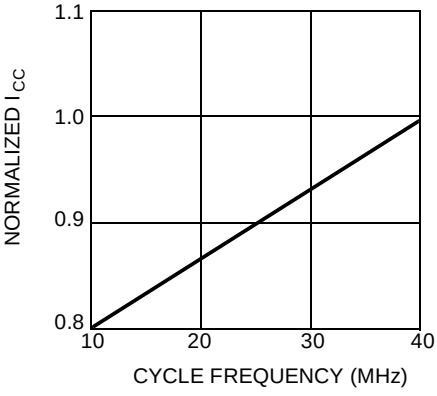
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Ordering Information

Speed (ns)	I_{CC} (mA)	Ordering Code	Package Name	Package Type	Operating Range
15	115	CY7C168A-15PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
		CY7C168A-15VC	V5	20-Lead Molded SOJ	
20	90	CY7C168A-20PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
		CY7C168A-20VC	V5	20-Lead Molded SOJ	
		CY7C168A-20DMB	D6	20-Lead (300-Mil) CerDIP	Military
25	70	CY7C168A-25PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
		CY7C168A-25VC	V5	20-Lead Molded SOJ	
	80	CY7C168A-25DMB	D6	20-Lead (300-Mil) CerDIP	Military
35	70	CY7C168A-35PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
		CY7C168A-35VC	V5	20-Lead Molded SOJ	
		CY7C168A-35DMB	D6	20-Lead (300-Mil) CerDIP	Military
45	70	CY7C168A-45PC	P5	20-Lead (300-Mil) Molded DIP	Commercial
		CY7C168A-45VC	V5	20-Lead Molded SOJ	
		CY7C168A-45DMB	D6	20-Lead (300-Mil) CerDIP	Military

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

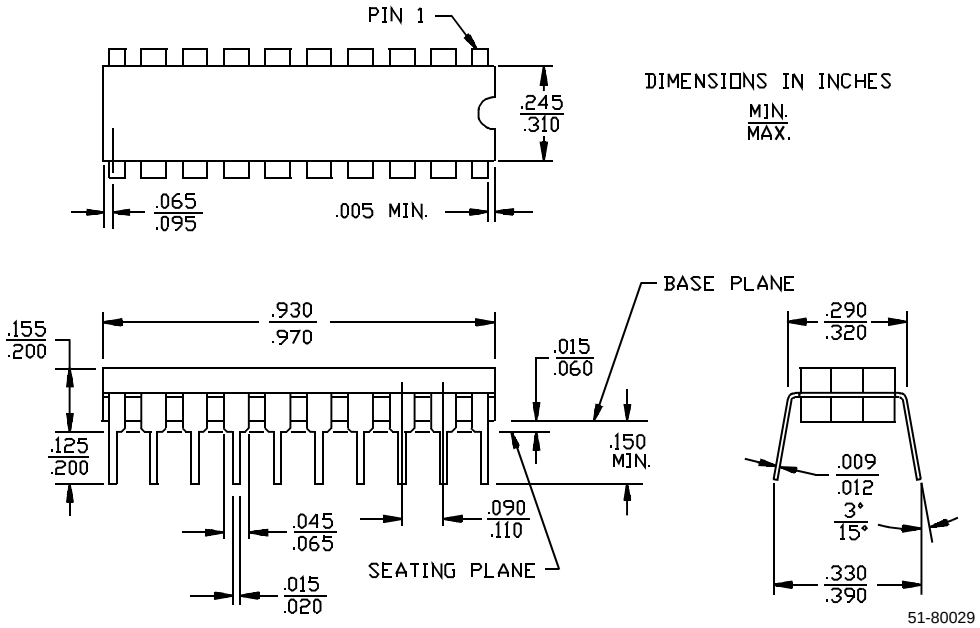
Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{RCS}	7, 8, 9, 10, 11
t_{RCH}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

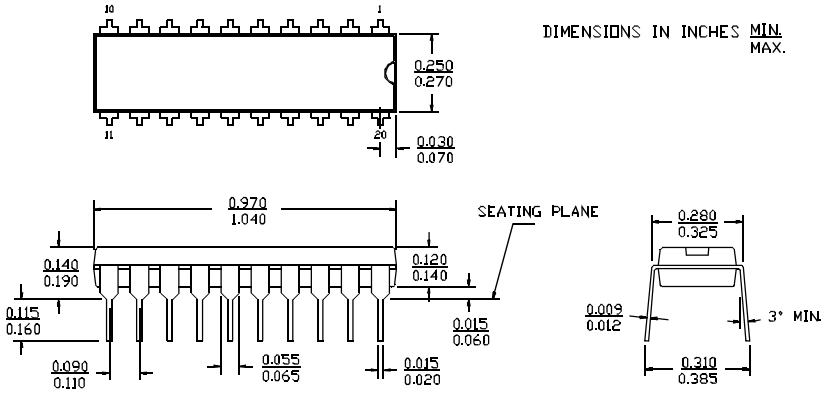
Package Diagrams

20-Lead (300-Mil) CerDIP D6
MIL-STD-1835 D-8 Config. A



51-80029

20-Lead (300-Mil) Molded DIP P5



51-85011-A

Package Diagrams (continued)

20-Lead (300-Mil) Molded SOJ V5