

INTEGRATED CIRCUITS

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4068B gates 8-input NAND gate

Product specification
File under Integrated Circuits, IC04

January 1995

8-input NAND gate

HEF4068B gates

DESCRIPTION

The HEF4068B provides the 8-input NAND function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

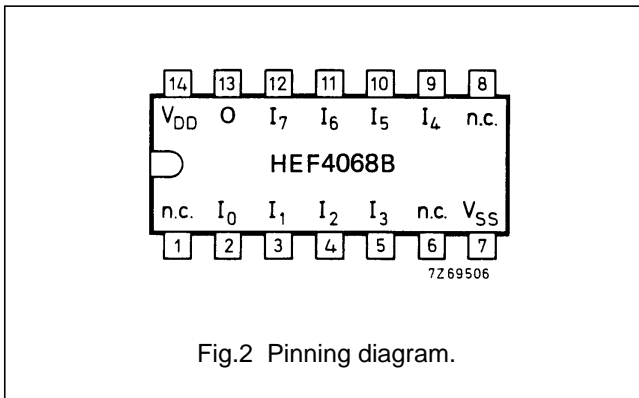


Fig.2 Pinning diagram.

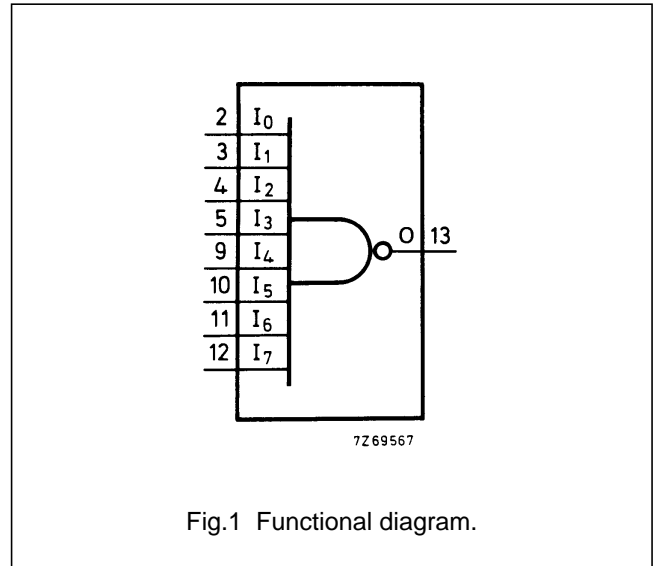


Fig.1 Functional diagram.

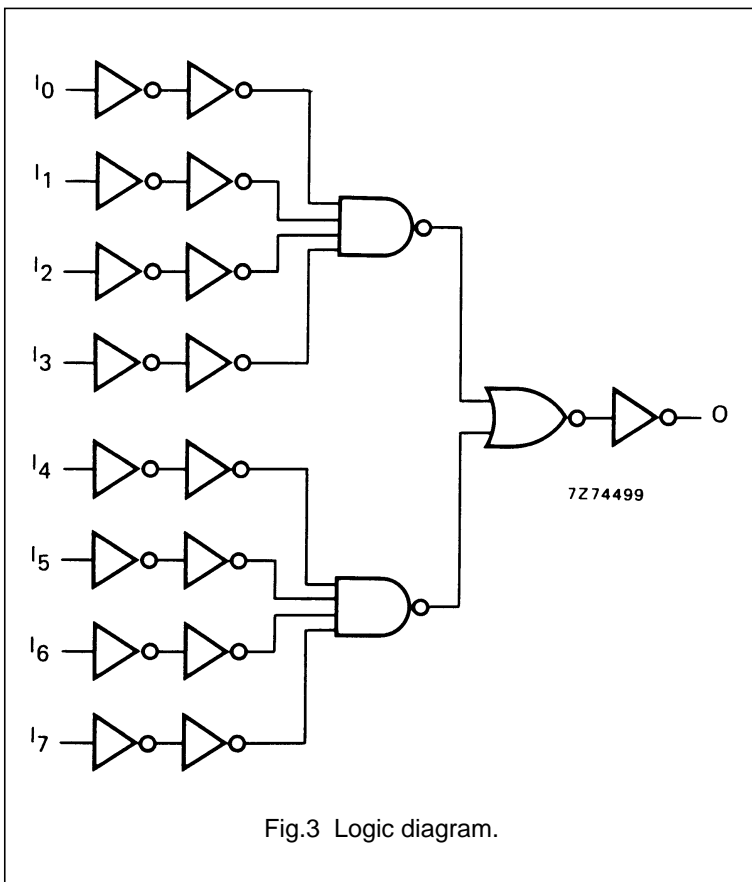


Fig.3 Logic diagram.

- HEF4068BP(N): 14-lead DIL; plastic (SOT27-1)
- HEF4068BD(F): 14-lead DIL; ceramic (cerdip) (SOT73)
- HEF4068BT(D): 14-lead SO; plastic (SOT108-1)
- (): Package Designator North America

FAMILY DATA, I_{DD} LIMITS category GATES

See Family Specifications

8-input NAND gate

HEF4068B
gates**AC CHARACTERISTICS** $V_{SS} = 0 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$; $C_L = 50 \text{ pF}$; input transition times $\leq 20 \text{ ns}$

	V_{DD} V	SYMBOL	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA	
Propagation delays $I_n \rightarrow O$ HIGH to LOW	5	t_{PHL}	95	195	ns	$68 \text{ ns} + (0,55 \text{ ns/pF}) C_L$	
	10		40	85	ns	$29 \text{ ns} + (0,23 \text{ ns/pF}) C_L$	
	15		30	65	ns	$22 \text{ ns} + (0,16 \text{ ns/pF}) C_L$	
	LOW to HIGH	5	t_{PLH}	80	165	ns	$53 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
		10		35	70	ns	$24 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
		15		30	60	ns	$22 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
Output transition times HIGH to LOW	5	t_{THL}	60	120	ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$	
	10		30	60	ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$	
	15		20	40	ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$	
	LOW to HIGH	5	t_{TLH}	60	120	ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$
		10		30	60	ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$
		15		20	40	ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$

	V_{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5	$700 f_i + \sum(f_o C_L) \times V_{DD}^2$	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\sum(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$2900 f_i + \sum(f_o C_L) \times V_{DD}^2$	
	15	$7200 f_i + \sum(f_o C_L) \times V_{DD}^2$	