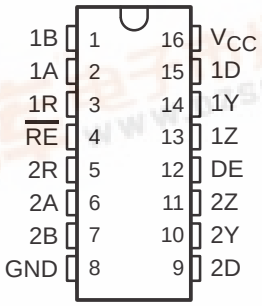
DUAL DIFFERENTIAL DRIVERS AND RECEIVERS

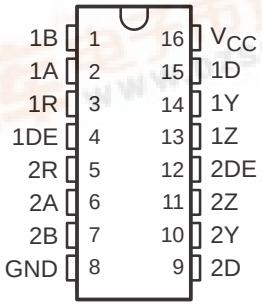
SLLS159C – MARCH 1993 – REVISED APRIL 1998

- **Meet or Exceed Standards TIA/EIA-422-B and ITU Recommendation V.11**
- **BiCMOS Process Technology**
- **Low Supply-Current Requirements: 9 mA Max**
- **Low Pulse Skew**
- **Receiver Input Impedance . . . 17 kΩ Typ**
- **Receiver Input Sensitivity . . . ±200 mV**
- **Receiver Common-Mode Input Voltage Range of −7 V to 7 V**
- **Operate From Single 5-V Power Supply**
- **Glitch-Free Power-Up/Power-Down Protection**
- **Receiver 3-State Outputs Active-Low Enable for SN75C1167 Only**
- **Improved Replacements for the MC34050 and MC34051**

SN75C1167 . . . N OR NS† PACKAGE
(TOP VIEW)



SN75C1168 . . . N OR NS† PACKAGE
(TOP VIEW)



† The NS package is only available left-ended taped and reeled (order device SNx5C116xNSLE).

description

The SN75C1167 and SN75C1168 dual drivers and receivers are monolithic integrated circuits designed for balanced transmission lines. The devices meet TIA/EIA-422-B and ITU recommendation V.11.

The SN75C1167 combines dual 3-state differential line drivers and 3-state differential line receivers, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, which can be connected externally together to function as direction control. The SN75C1168 drivers have individual active-high enables.

The SN75C1167 and SN75C1168 are characterized for operation from 0°C to 70°C.

Function Tables

EACH DRIVER

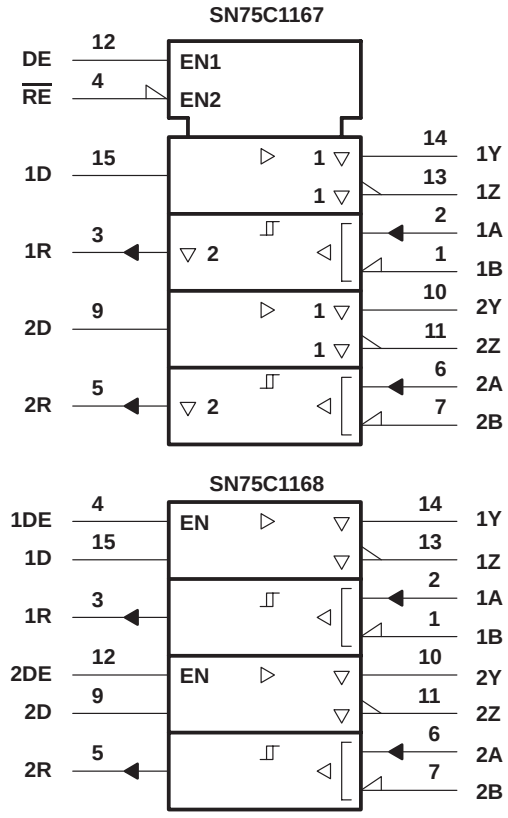
INPUT D	ENABLE DE	OUTPUTS Y	OUTPUTS Z
H	H	H	L
L	H	L	H
X	L	Z	Z

SN75C1167, EACH RECEIVER

DIFFERENTIAL INPUTS A – B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
–0.2 V < V_{ID} < 0.2 V	L	?
$V_{ID} \leq$ –0.2 V	L	L
X	H	Z
Open	L	H

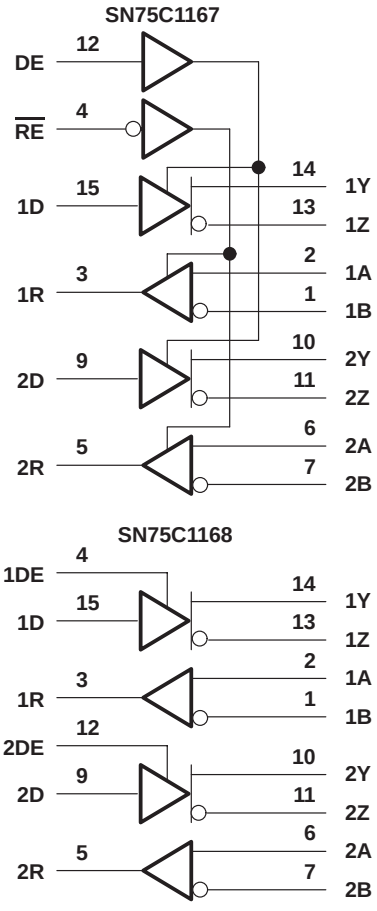
H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

logic symbol†

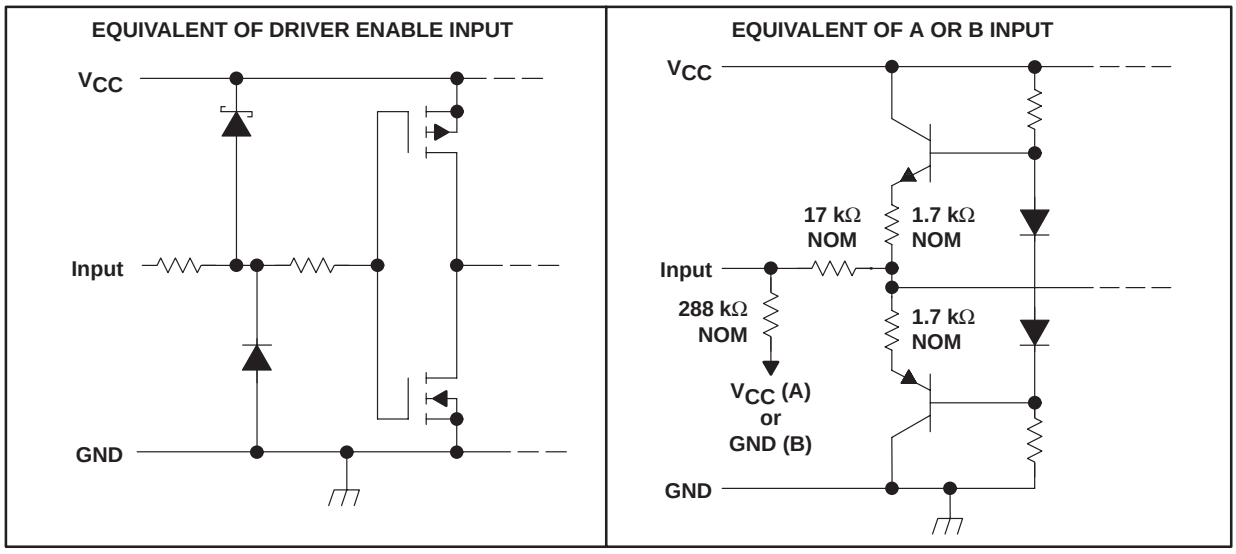


† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

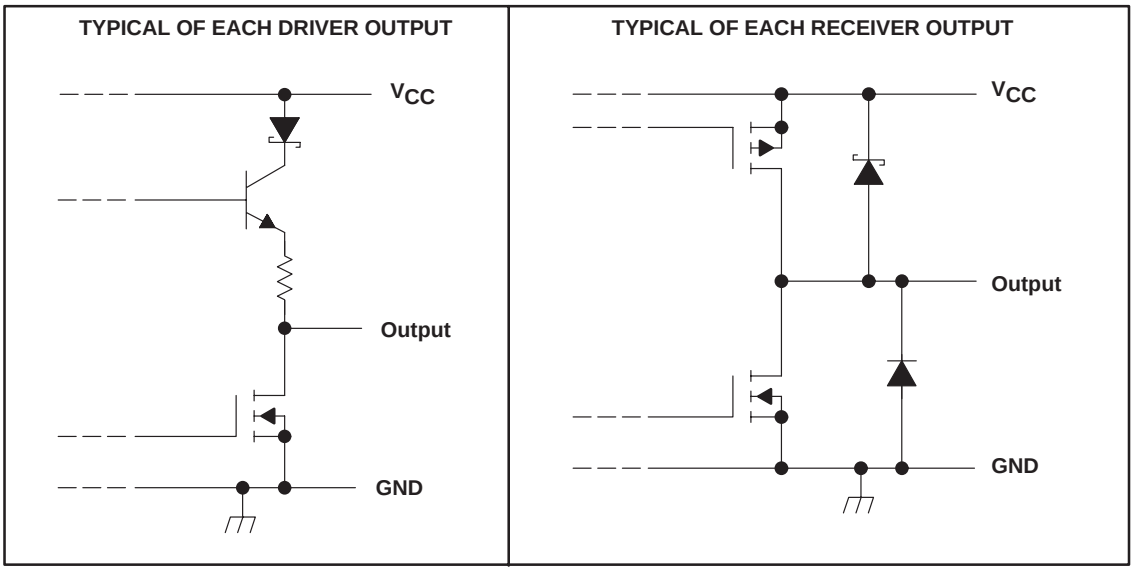
logic diagram (positive logic)



schematics of inputs



schematics of outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . –0.5 V to 7 V
Input voltage range, V_I . . . . . –0.5 V to V_{CC} + 0.5 V
Input voltage range, V_I (A or B, Receiver) . . . . . –11 V to 14 V
Differential input voltage range, V_{ID}, Receiver (see Note 2) . . . . . –14 V to 14 V
Output voltage range, V_O, Driver . . . . . –5 V to 7 V
Clamp current range, I_{IK} or I_{OK}, Driver . . . . . ±20 mA
Output current range, I_O, Driver . . . . . ±150 mA
Supply current, I_{CC} . . . . . 200 mA
GND current . . . . . –200 mA
Output current range, I_O, Receiver . . . . . ±25 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values except differential input voltage are with respect to the network GND.
2. Differential input voltage is measured at the noninverting terminal with respect to the inverting terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	OPERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
N	1250 mW	10 mW/°C	800 mW	650 mW
NS	625 mW	5 mW/°C	400 mW	325 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	5.5	V
Common-mode input voltage, V_{IC} (see Note 3)	Receiver			±7	V
Differential input voltage, V_{ID}	Receiver			±7	V
High-level input voltage, V_{IH}	Except A, B	2			V
Low-level input voltage, V_{IL}	Except A, B			0.8	V
High-level output current, I_{OH}	Receiver			–6	mA
	Driver			–20	
Low-level output current, I_{OL}	Receiver			6	mA
	Driver			20	
Operating free-air temperature, T_A		0		70	°C

NOTE 3: Refer to TIA/EIA-422-B for exact conditions.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = –18 mA				–1.5	V
V_{OH}	High-level output voltage	V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = –20 mA		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA			0.2	0.4	V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0 mA		2		6	V
$\|V_{OD2}\|$	Differential output voltage	R_L = 100 Ω, See Figure 1 and Note 3		2	3.1		V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage					±0.4	V
V_{OC}	Common-mode output voltage					±3	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage					±0.4	V
$I_{O(OFF)}$	Output current with power off (see Note 3)	V_{CC} = 0 V	V_O = 6 V			100	µA
			V_O = –0.25 V			–100	µA
I_{OZ}	High-impedance-state output current	V_O = 2.5 V				20	µA
		V_O = 5 V				–20	
I_{IH}	High-level input current	V_I = V_{CC} or V_{IH}				1	µA
I_{IL}	Low-level input current	V_I = GND or V_{IL}				–1	µA
I_{OS}	Short-circuit output current	V_O = V_{CC} or GND, See Note 4		–30		–150	mA
I_{CC}	Supply current (total package)	No load, Enabled	V_I = V_{CC} or GND		4	6	mA
			V_I = 2.4 or 0.5 V, See Note 5		5	9	
C_i	Input capacitance				6		pF

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

NOTES: 3. Refer to TIA/EIA-422-B for exact conditions.
4. Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
5. This parameter is measured per input, while the other inputs are at V_{CC} or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PHL}	Propagation delay time, high- to low-level output	R_1 = R_2 = 50 Ω, R_3 = 500 Ω, C_1 = C_2 = C_3 = 40 pF, S1 is open, See Figure 2		7	12	ns
t_{PLH}	Propagation delay time, low- to high-level output			7	12	ns
$t_{sk(p)}$	Pulse skew			0.5	4	ns
t_r	Rise time	R_1 = R_2 = 50 Ω, R_3 = 500 Ω, C_1 = C_2 = C_3 = 40 pF, S1 is open, See Figure 3		5	10	ns
t_f	Fall time			5	10	ns
t_{PZH}	Output enable time to high level	R_1 = R_2 = 50 Ω, R_3 = 500 Ω, C_1 = C_2 = C_3 = 40 pF, S1 is closed, See Figure 4		10	19	ns
t_{PZL}	Output enable time to low level			10	19	ns
t_{PHZ}	Output disable time from low level	R_1 = R_2 = 50 Ω, R_3 = 500 Ω, C_1 = C_2 = C_3 = 40 pF, S1 is closed, See Figure 4		7	16	ns
t_{PLZ}	Output disable time from high level			7	16	ns

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage, differential input						0.2	V
V_{IT-}	Negative-going input threshold voltage, differential input				–0.2‡			V
V_{hys}	Input hysteresis ($V_{IT+} - V_{IT-}$)					60		mV
V_{IK}	Input clamp voltage, $\overline{RE}$	SN75C1167	I_I = –18 mA				–1.5	V
V_{OH}	High-level output voltage		V_{ID} = 200 mV,	I_{OH} = –6 mA	3.8	4.2		V
V_{OL}	Low-level output voltage		V_{ID} = –200 mV,	I_{OL} = 6 mA		0.1	0.3	V
I_{OZ}	High-impedance-state output current	SN75C1167	V_O = V_{CC} or GND			±0.5	±5	µA
I_I	Line input current		Other input at 0 V	V_I = 10 V			1.5	mA
				V_I = –10 V			–2.5	
I_I	Enable input current, $\overline{RE}$	SN75C1167	V_I = V_{CC} or GND				±1	µA
r_i	Input resistance		V_{IC} = –7 V to 7 V,	Other input at 0 V	4	17		kΩ
I_{CC}	Supply current (total package)		No load, Enabled	V_I = V_{CC} or GND		4	6	mA
				V_{IH} = 2.4 V or 0.5 V, See Note 5		5	9	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 6)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	See Figure 5	9	17	27	ns
t_{PHL}	Propagation delay time, high- to low-level output		9	17	27	ns
t_{TLH}	Transition time, low- to high-level output	V_{IC} = 0 V, See Figure 5		4	9	ns
t_{THL}	Transition time, high- to low-level output			4	9	ns
t_{PZH}	Output enable time to high level	R_L = 1 kW, See Figure 6		13	22	ns
t_{PZL}	Output enable time to low level			13	22	ns
t_{PHZ}	Output disable time from high level			13	22	ns
t_{PLZ}	Output disable time from low level			13	22	ns

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
NOTE 6: Measured per input while the other inputs are at V_{CC} or GND

PARAMETER MEASUREMENT INFORMATION

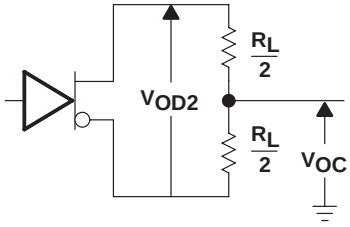
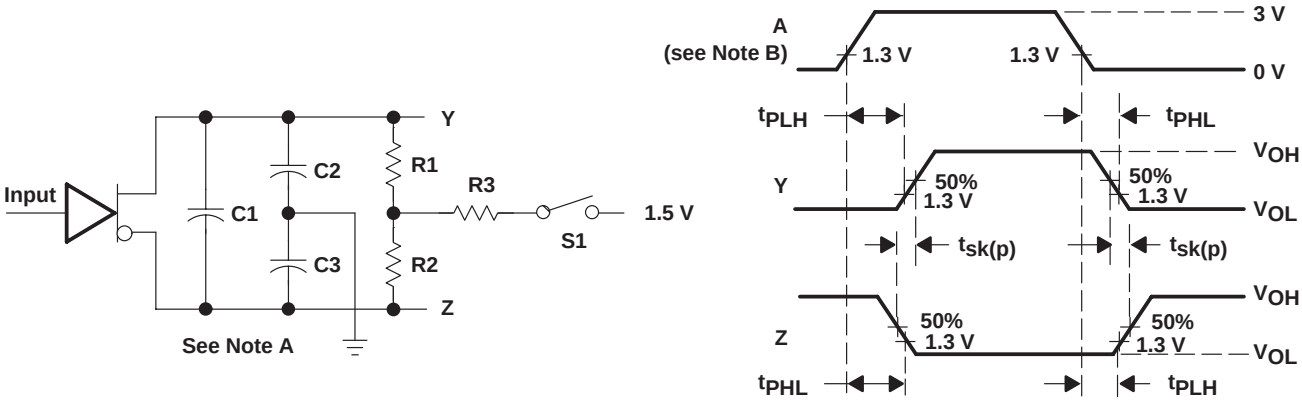


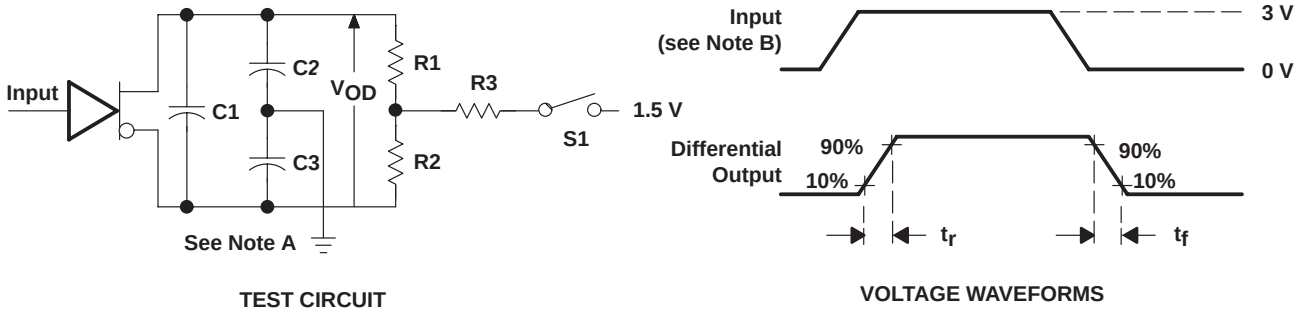
Figure 1. Driver Test Circuit, V_{OD} and V_{OC}



TEST CIRCUIT **VOLTAGE WAVEFORMS**

NOTES: A. C1, C2, and C3 include probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r = t_f \leq 6$ ns.

Figure 2. Driver Test Circuit and Voltage Waveforms

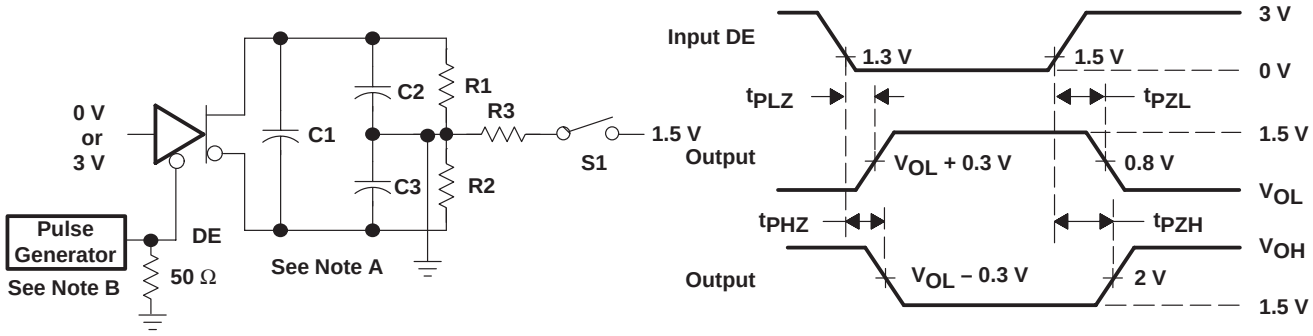


TEST CIRCUIT **VOLTAGE WAVEFORMS**

NOTES: A. C1, C2, and C3 include probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r = t_f \leq 6$ ns.

Figure 3. Driver Test Circuit and Voltage Waveforms

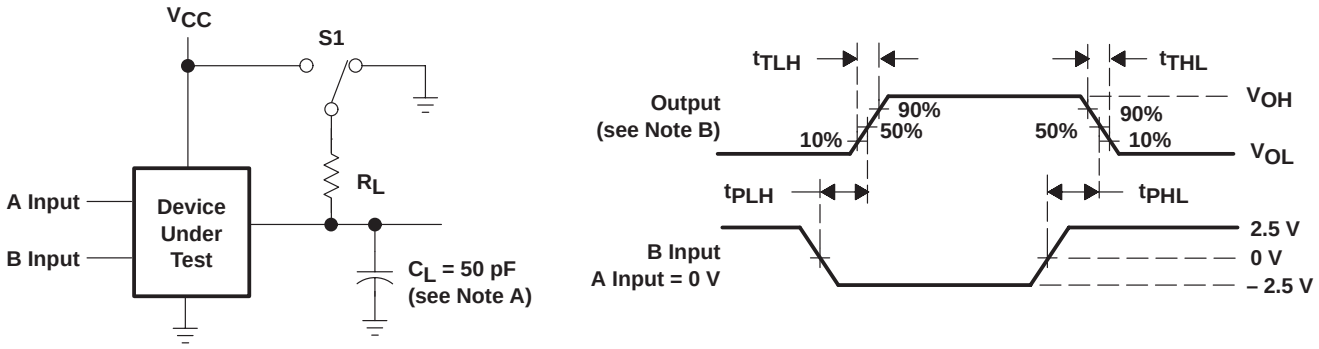
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. C1, C2, and C3 include probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r = t_f \leq 6$ ns.

Figure 4. Driver Test Circuit and Voltage Waveforms

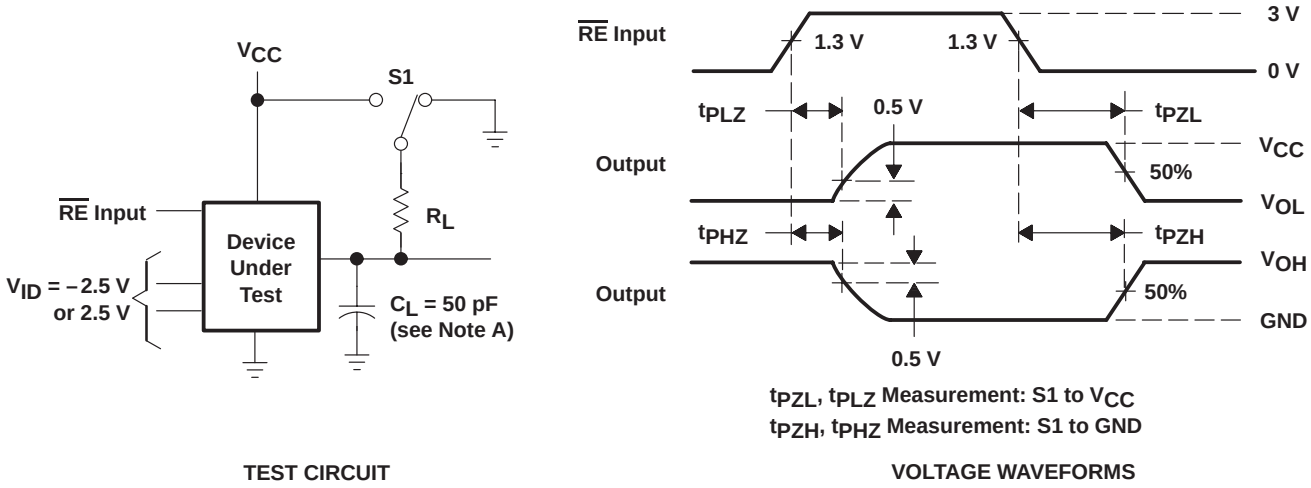


TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, $t_r = t_f \leq 6$ ns.

Figure 5. Receiver Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT **VOLTAGE WAVEFORMS**

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, $t_r = t_f \leq 6$ ns.

Figure 6. Receiver Test Circuit and Voltage Waveforms

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