19-3061; Rev 0; 10/03

MAXIM

12-Output, 76V, Serial-Interfaced VFD Tube Driver

General Description

The MAX6920 is a 12-output, 76V, vacuum fluorescent display (VFD) tube driver that interfaces a multiplexed VFD tube to a VFD controller such as the MAX6850–MAX6853 or to a microcontroller. The MAX6920 is also ideal for driving either static VFD tubes or telecom relays.

Data is inputted using an industry-standard 4-wire serial interface (CLOCK, DATA, LOAD, BLANK) for compatibility with both industry-standard drivers and Maxim's VFD controllers.

For easy display control, the active-high BLANK input forces all driver outputs low, turning the display off, and automatically puts the MAX6920 into shutdown mode. Display intensity may also be controlled by pulse-width modulating the BLANK input.

The MAX6920 has a serial interface data output pin, DOUT, allowing any number of devices to be cascaded on the same serial interface.

The MAX6920 is available in a 20-pin SO package. Maxim also offers VFD drivers with either 20 (MAX6921/MAX6931) or 32 outputs (MAX6922 and MAX6932).

Features

- ♦ 5MHz Industry-Standard 4-Wire Serial Interface
- ♦ 3V to 5.5V Logic Supply Range
- ♦ 8V to 76V Grid/Anode Supply Range
- ♦ Push-Pull CMOS High-Voltage Outputs
- ♦ Outputs can Source 40mA, Sink 4mA Continuously
- ♦ Outputs can Source 75mA Repetitive Pulses
- ♦ Outputs can be Paralleled for Higher Current Drive
- ♦ Any Output can be Used as a Grid or an Anode Driver
- ♦ Blank Input Simplifies PWM Intensity Control
- ♦ Small 20-Pin SO Package
- ♦ -40°C to +125°C Temperature Range

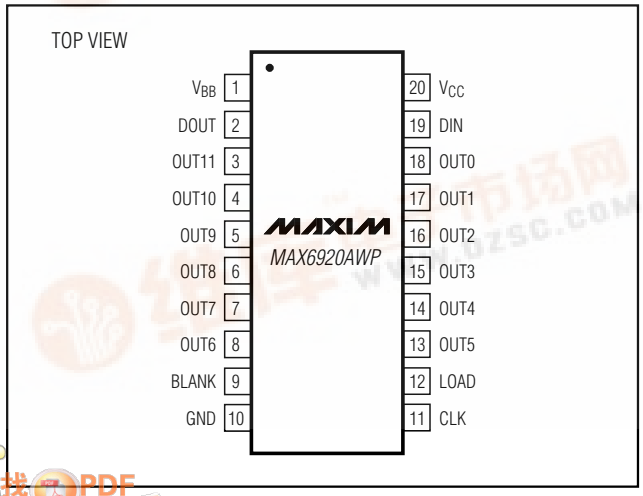
Applications

White Goods
Gaming Machines
Automotive
Avionics
Industrial Weighing
Security
Telecom

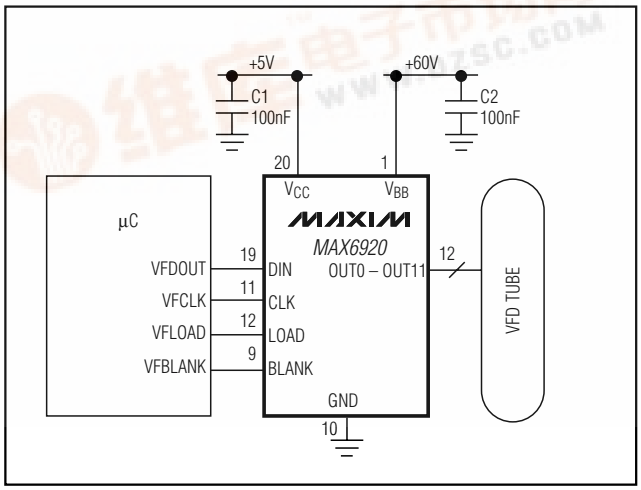
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX6920AWP	-40°C to +125°C	20 Wide SO

Pin Configuration



Typical Operating Circuit



12-Output, 76V, Serial-Interfaced VFD Tube Driver

ABSOLUTE MAXIMUM RATINGS

Voltage (with respect to GND)
- V_{BB} ..... -0.3V to +80V
- V_{CC} ..... -0.3V to +6V
- OUT_ ..... -0.3V to (V_{BB} + 0.3V)
- All Other Pins ..... -0.3V to (V_{CC} + 0.3V)

OUT_ Continuous Source Current ..... -45mA
OUT_ Pulsed (1ms max, 1/4 max duty) Source Current ... -80mA
Total OUT_ Continuous Source Current ..... -540mA
Total OUT_ Continuous Sink Current 60mA
Total OUT_ Pulsed (1ms max, 1/4 max duty)
Source Current ..... -960mA
OUT_ Sink Current 15mA
CLK, DIN, LOAD, BLANK, DOUT Current ..... ±10mA
Continuous Power Dissipation
20-Pin Wide SO (derate 10mW/°C over T_A = +70°C) .. 800mW
Operating Temperature Range (T_{MIN} to T_{MAX}) . -40°C to +125°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Typical Operating Circuit, V_{BB} = 8V to 76V, V_{CC} = 3V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Logic Supply Voltage	V_{CC}			3		5.5	V
Tube Supply Voltage	V_{BB}			8		76	V
Logic Supply Operating Current	I_{CC}	All outputs OUT_ low, CLK = idle	T_A = +25°C		72	170	µA
			T_A = -40°C to +125°C			200	
		All outputs OUT_ high, CLK = idle	T_A = +25°C		350	650	
			T_A = -40°C to +125°C			700	
Tube Supply Operating Current	I_{BB}	All outputs OUT_ low	T_A = +25°C		1	2	mA
			T_A = -40°C to +125°C			4.2	
		All outputs OUT_ high	T_A = +25°C		0.53	0.85	
			T_A = -40°C to +125°C			0.9	
High-Voltage OUT_	V_H	V_{BB} ≥ 15V, I_{OUT} = -25mA	T_A = +25°C	V_{BB} - 1.1			V
			T_A = -40°C to +85°C	V_{BB} - 2			
			T_A = -40°C to +125°C	V_{BB} - 2.5			
		V_{BB} ≥ 15V, I_{OUT} = -40mA	T_A = -40°C to +85°C	V_{BB} - 3.5			
			T_A = -40°C to +125°C	V_{BB} - 4.0			
		8V < V_{BB} < 15V, I_{OUT} = -25mA	T_A = +25°C	V_{BB} - 1.2			
			T_A = -40°C to +85°C	V_{BB} - 2.5			
			T_A = -40°C to +125°C	V_{BB} - 3.0			
Low-Voltage OUT_	V_L	V_{BB} ≥ 15V, I_{OUT} = 1mA	T_A = +25°C		0.75	1	V
			T_A = -40°C to +85°C			1.5	
			T_A = -40°C to +125°C			1.9	
		8V < V_{BB} < 15V, I_{OUT} = 1mA	T_A = +25°C		0.8	1.1	
			T_A = -40°C to +85°C			1.6	
			T_A = -40°C to +125°C			2.0	

ELECTRICAL CHARACTERISTICS (continued)

(Typical Operating Circuit, V_{BB} = 8V to 76V, V_{CC} = 3V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Rise Time OUT_ (20% to 80%)	t_R	V_{BB} = 60V, C_L = 50pF, R_L = 2.3kΩ			0.9	2	µs
Fall Time OUT_ (80% to 20%)	t_F	V_{BB} = 60V, C_L = 50pF, R_L = 2.3kΩ			0.6	1.5	µs
SERIAL INTERFACE TIMING CHARACTERISTICS							
LOAD Rising to OUT_ Falling Delay		(Notes 2, 3)			0.9	1.8	µs
LOAD Rising to OUT_ Rising Delay		(Notes 2, 3)			1.2	2.4	µs
BLANK Rising to OUT_ Falling Delay		(Notes 2, 3)			0.9	1.8	µs
BLANK Falling to OUT_ Rising Delay		(Notes 2, 3)			1.3	2.5	µs
Input Leakage Current CLK, DIN, LOAD, BLANK	I_{IH}, I_{IL}				0.05	10	µA
Logic-High Input Voltage CLK, DIN, LOAD, BLANK	V_{IH}			0.8 x V_{CC}			V
Logic-Low Input Voltage CLK, DIN, LOAD, BLANK	V_{IL}					0.3 x V_{CC}	V
Hysteresis Voltage DIN, CLK, LOAD, BLANK	ΔV_I				0.6		V
High-Voltage DOUT	V_{OH}	I_{SOURCE} = -1.0mA		V_{CC} - 0.5			V
Low-Voltage DOUT	V_{OL}	I_{SINK} = 1.0mA				0.5	V
Rise and Fall Time DOUT		C_{DOUT} = 10pF (Note 2)	3V to 4.5V		60	100	ns
			4.5V to 5.5V		30	80	
CLK Clock Period	t_{CP}			200			ns
CLK Pulse-Width High	t_{CH}			90			ns
CLK Pulse-Width Low	t_{CL}			90			ns
CLK Rise to LOAD Rise Hold	t_{CSH}	(Note 2)		100			ns
DIN Setup Time	t_{DS}			5			ns
DIN Hold Time	t_{DH}	3V to 4.5V		20			ns
		4.5V to 5.5V		15			
DOUT Propagation Delay	t_{DO}	C_{DOUT} = 10pF	3.0V to 4.5V	25	120	240	ns
			4.5V to 5.5V	20	75	150	
LOAD Pulse High	t_{CSW}			55			ns

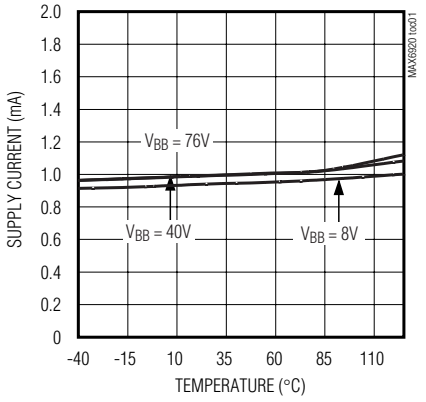
Note 1: All parameters are tested at T_A = +25°C. Specifications over temperature are guaranteed by design.
Note 2: Guaranteed by design.
Note 3: Delay measured from control edge to when output OUT_ changes by 1V.

12-Output, 76V, Serial-Interfaced VFD Tube Driver

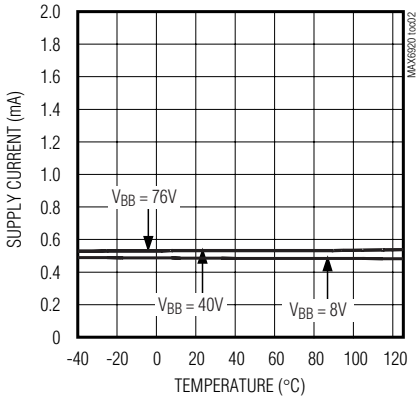
Typical Operating Characteristics

(V_{CC} = 5.0V, V_{BB} = 76V, and T_A = +25°C, unless otherwise noted.)

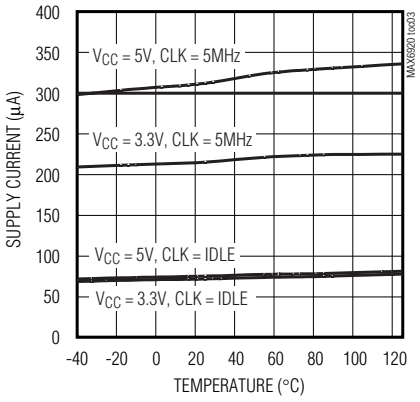
TUBE SUPPLY CURRENT (I_{BB}) vs. TEMPERATURE (OUTPUTS LOW)



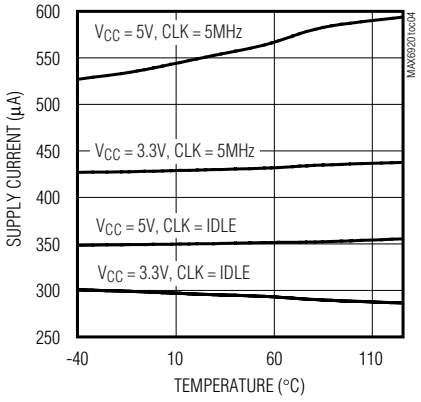
TUBE SUPPLY CURRENT (I_{BB}) vs. TEMPERATURE (OUTPUTS HIGH)



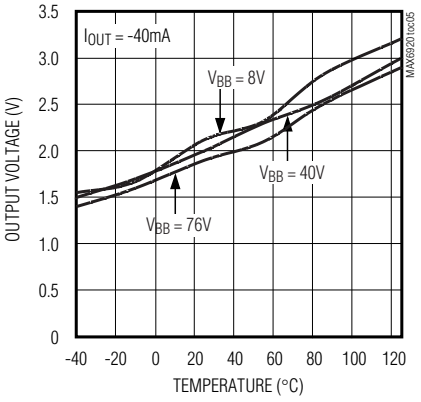
LOGIC SUPPLY CURRENT (I_{CC}) vs. TEMPERATURE (OUTPUTS LOW)



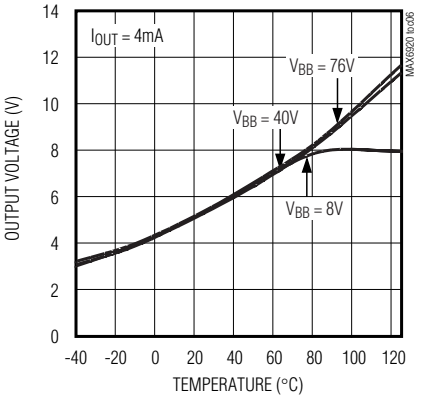
SUPPLY CURRENT (I_{CC}) vs. TEMPERATURE (OUTPUTS HIGH)



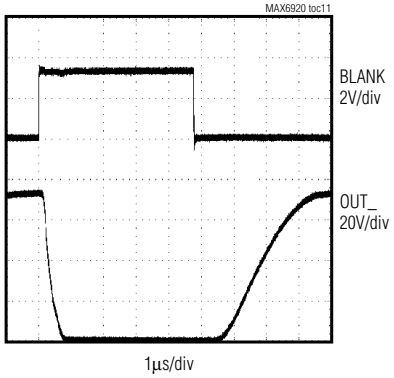
OUTPUT VOLTAGE (V_{BB} - V_H) vs. TEMPERATURE (OUTPUT HIGH)



OUTPUT VOLTAGE vs. TEMPERATURE (OUTPUT LOW)



OUTPUT RISE AND FALL WAVEFORM



Pin Description

PIN	NAME	FUNCTION
1	V_{BB}	VFD Tube Supply Voltage
2	DOUT	Serial-Clock Output. Data is clocked out of the internal shift register to DOUT on CLK's rising edge.
3–8, 13–18	OUT0 to OUT11	VFD Anode and Grid Drivers. OUT0 to OUT11 are push-pull outputs swinging from V_{BB} to GND.
9	BLANK	Blanking Input. High forces outputs OUT0 to OUT11 low, without altering the contents of the output latches. Low enables outputs OUT0 to OUT11 to follow the state of the output latches.
10	GND	Ground
11	CLK	Serial-Clock Input. Data is loaded into the internal shift register on CLK's rising edge.
12	LOAD	Load Input. Data is loaded transparently from the internal shift register to the output latch while LOAD is high. Data is latched into the output latch on LOAD's rising edge, and retained while LOAD is low.
19	DIN	Serial-Data Input. Data is loaded into the internal shift register on CLK's rising edge.
20	V_{CC}	Logic Supply Voltage

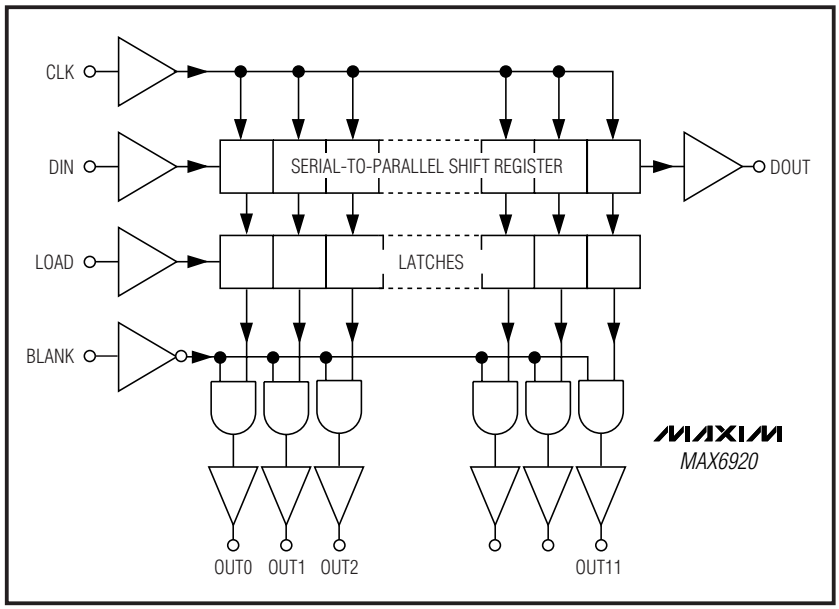


Figure 1. MAX6920 Functional Diagram

12-Output, 76V, Serial-Interfaced VFD Tube Driver

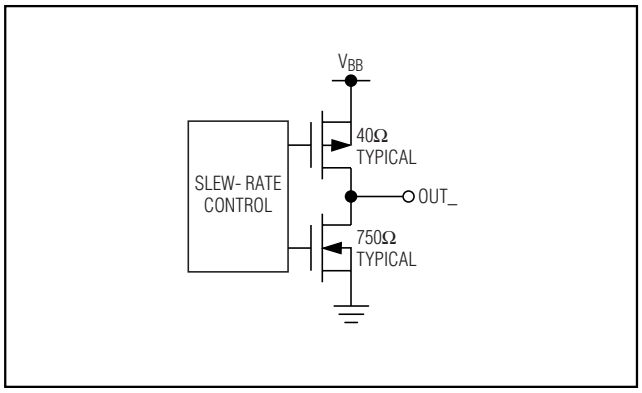


Figure 2. MAX6920 CMOS Output Driver Structure

Detailed Description

The MAX6920 is a VFD tube driver comprising a 4-wire serial interface driving 12 high-voltage Rail-to-Rail® output ports. The driver is suitable for both static and multiplexed displays.

The output ports feature high current-sourcing capability to drive current into grids and anodes of static or multiplex VFDs. The ports also have active current sinking for fast discharge of capacitive display electrodes in multiplexing applications.

The 4-wire serial interface comprises a 12-bit shift register and a 12-bit transparent latch. The shift register is written through a clock input CLK and a data input DIN and the data propagates to a data output DOUT. The data output allows multiple drivers to be cascaded and operated together. The output latch is transparent to the shift register outputs when LOAD is high, and latches the current state on the falling edge of LOAD.

Each driver output is a slew-rated controlled CMOS push-pull switch driving between V_{BB} and GND. The output rise time is always slower than the output fall time to avoid shoot-through currents during output transitions. The output slew rates are slow enough to minimize EMI, yet are fast enough so as not to impact the typical 100µs digit multiplex period and affect the display intensity.

Initial Power-Up and Operation

An internal reset circuit clears the internal registers of the MAX6920 on power-up. All outputs OUT0 to OUT11 and the interface output DOUT initialize low regardless of the initial logic levels of the CLK, DIN, BLANK, and LOAD inputs.

4-Wire Serial Interface

The MAX6920 uses a 4-wire serial interface with three inputs (DIN, CLK, LOAD) and a data output (DOUT). This interface is used to write output data to the MAX6920 (Figure 3) (Table 1). The serial interface data word length is 12 bits, D0–D11.

The functions of the four serial interface pins are:

- CLK input is the interface clock, which shifts data into the MAX6920's 12-bit shift register on its rising edge.
- LOAD input passes data from the MAX6920's 12-bit shift register to the 12-bit output latch when LOAD is high (transparent latch), and latches the data on LOAD's falling edge.

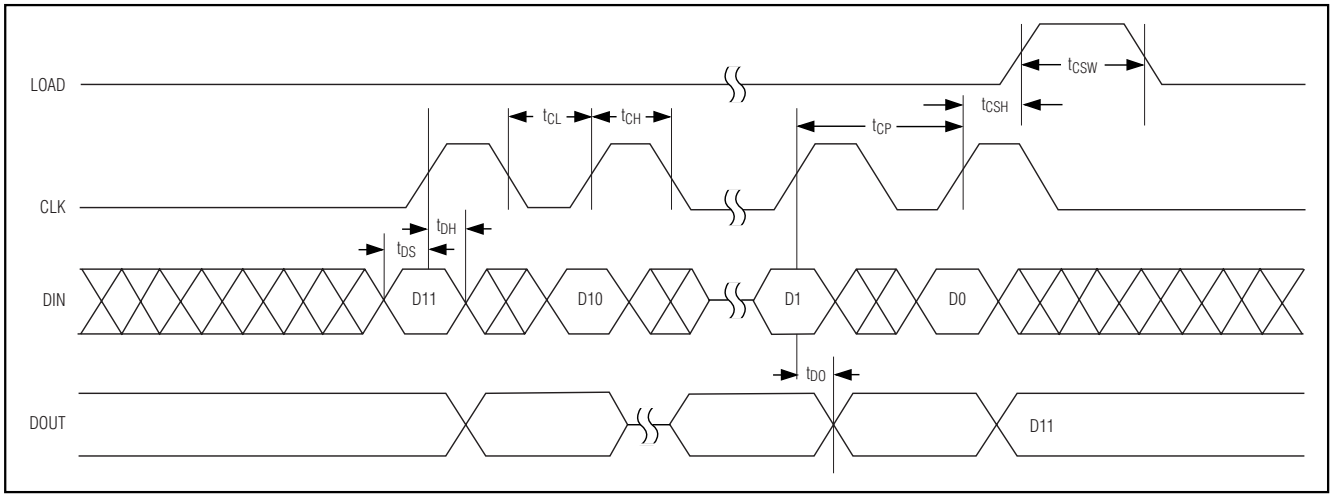


Figure 3. 4-Wire Serial Interface Timing Diagram

Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.

Table 1. 4-Wire Serial Interface Truth Table

SERIAL DATA INPUT	CLOCK INPUT	SHIFT REGISTER CONTENTS						LOAD INPUT	LATCH CONTENTS						BLANKING INPUT	OUTPUT CONTENTS					
DIN	CLK	D0	D1	D2	…	Dn-1	Dn	LOAD	D0	D1	D2	…	Dn-1	Dn	BLANK	D0	D1	D2	…	Dn-1	Dn
H	↑	H	R0	R1	…	Rn-2	Rn-1														
L	↑	L	R0	R1	…	Rn-2	Rn-1														
X	↓	R0	R1	R2	…	Rn-1	Rn														
		X	X	X	…	X	X	L	R0	R1	R2	…	Rn-1	Rn							
		P0	P1	P2	…	Pn-1	Pn	H	P0	P1	P2	…	Pn-1	Pn	L	P0	P1	P2	…	Pn-1	Pn
									X	X	X	…	X	X	H	L	L	L	…	L	L

L = Low logic level.
H = High logic level.
X = Don't care.
P = Present state (shift register).
R = Previous state (latched).

- DIN is the interface data input, and must be stable when it is sampled on the rising edge of CLK.
- DOUT is the interface data output, which shifts data out from the MAX6920's 12-bit shift register on the falling edge of CLK. Data at DIN is propagated through the shift register and appears at DOUT (20 CLK cycles + t_{DO}) later.

A fifth input pin, BLANK, can be taken high to force outputs OUT0 to OUT11 low, without altering the contents of the output latches. When the BLANK input is low, outputs OUT0 to OUT11 follow the state of the output latches. A common use of the BLANK input is PWM intensity control.

The BLANK input's function is independent of the operation of the serial interface. Data can be shifted into the serial interface shift register and latched regardless of the state of BLANK.

Writing Device Registers Using the 4-Wire Serial Interface

The MAX6920 is written using the following sequence:

1) Take CLK low.
2) Clock 12 bits of data in order D11 first to D0 last into DIN, observing the data setup and hold times.
3) Load the 12 output latches with a falling edge on LOAD.

LOAD may be high or low during a transmission. If LOAD is high, then the data shifted into the shift register at DIN appears at the OUT0 to OUT11 outputs.

CLK and DIN may be used to transmit data to other peripherals. Activity on CLK always shifts data into the MAX6920's shift register. However, the MAX6920 only updates its output latch on the rising edge of LOAD, and the last 12 bits of data are loaded. Therefore, multiple devices can share CLK and DIN as long as they have unique LOAD controls.

Determining Driver Output Voltage Drop

The outputs are CMOS drivers, and have a resistive characteristic. The typical and maximum sink and source output resistances can be calculated from the V_H and V_L electrical characteristics. Use this calculated resistance to determine the output voltage drop at different output currents.

Output Current Ratings

The continuous current source capability is 40mA per output. Outputs may drive up to 75mA as a repetitive peak current, subject to the on time (output high) being no longer than 1ms, and the duty cycle being such that the output power dissipation is no more than the dissipation for the continuous case. The repetitive peak rating allows outputs to drive a higher current in multiplex grid driver applications, where only one grid is on at a time, and the multiplex time per grid is no more than 1ms.

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Since dissipation is proportional to current squared, the maximum current that can be delivered for a given multiplex ratio is given by:

$$I_{PEAK} = (grids \times 1600)^{1/2}mA$$

where grids is the number of grids in a multiplexed display.

This means that a duplex application (two grids) can use a repetitive peak current of 56.5mA, a triplex application (three grids) can use a repetitive peak current of 69.2mA, and higher multiplex ratios are limited to 75mA.

Paralleling Outputs

Any number of outputs within the same package may be paralleled in order to raise the current drive or reduce the output resistance. Only parallel outputs directly (by shorting outputs together) if the interface control can be guaranteed to set the outputs to the same level. Although the sink output is relatively weak (typically 750Ω), that resistance is low enough to dissipate 530mW when shorted to an opposite level output at a V_{BB} voltage of only 20V. A safe way to parallel outputs is to use diodes to prevent the outputs from sinking current (Figure 4). Because the outputs cannot sink current from the VFD tube, an external discharge resistor, R, is required. For static tubes, R can be a large value such as 100kΩ. For multiplexed tubes, the value of the resistor can be determined by the load capacitance and timing characteristics required. Resistor Rl discharges tube capacitance C to 10% of the initial voltage in 2.3 x RC seconds. So, for example, a 15kΩ value for R discharges 100pF tube grid or anode from 40V to 4V in 3.5µs, but draws an additional 2.7mA from the driver when either output is high.

Power Dissipation

Take care to ensure that the maximum package dissipation ratings for the chosen package are not exceeded. Over dissipation is unlikely to be an issue when driving static tubes, but the peak currents are usually higher for multiplexed tubes. When using multiple driver devices, try to share the average dissipation evenly between the drivers.

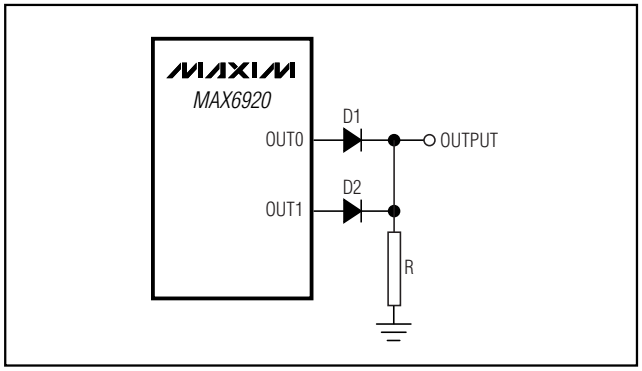


Figure 4. Paralleling Outputs

Determine the power dissipation (P_D) for the MAX6920 for static tube drivers with the following equation:

$$P_D = (V_{CC} \times I_{CC}) + (V_{BB} \times I_{BB}) + ((V_{BB} - V_H) \times I_{ANODE} \times A))$$

where:

A = number of anodes driven (a MAX6920 can drive a maximum of 12).

I_{ANODE} = maximum anode current.

(V_{BB} - V_H) is the output voltage drop at the given maximum anode current I_{OUT}.

A static tube dissipation example follows:

V_{CC} = 5V ±5%, V_{BB} = 10V to 18V, A = 12, I_{OUT} = 2mA

$$P_D = (5.25V \times 0.7mA) + (18V \times 0.9mA) + ((2.5V \times 2mA/25mA) \times 2mA \times 12) = 24.7mW$$

Determine the power dissipation (P_D) for the MAX6920 for multiplex tube drivers with the following equation:

$$P_D = (V_{CC} \times I_{CC}) + (V_{BB} \times I_{BB}) + ((V_{BB} - V_H) \times I_{ANODE} \times A) + ((V_{BB} - V_H) \times I_{GRID}))$$

where:

A = number of anodes driven

G = number of grids driven

I_{ANODE} = maximum anode current

I_{GRID} = maximum grid current

The calculation presumes all anodes are on but only one grid is on. The calculated P_D is the worst case, presuming one digit is always being driven with all its anodes lit. Actual P_D can be estimated by multiplying this P_D figure by the actual tube drive duty cycle, taking into account interdigit blanking and any PWM intensity control.

A multiplexed tube dissipation example follows:

V_{CC} = 5V ±5%, V_{BB} = 36V to 42V, A = 6, G = 6, I_{ANODE} = 0.4mA, I_{GRID} = 24mA

$$P_D = (5.25V \times 0.7mA) + (42V \times 0.9mA) + ((2.5V \times 0.4mA/25mA) \times 0.4mA \times 6) + ((2.5V \times 24mA/25mA) \times 24mA) = 99mW$$

Thus, for a 20-pin wide SO package (T_{JA} = 1 / 0.01 = +100°C/W from *Absolute Maximum Ratings*), the maximum allowed ambient temperature T_A is given by:

$$T_{J(MAX)} = T_A + (P_D \times T_{JA}) = +150°C = T_A + (0.099 \times +100°C/W)$$

So T_A = +140°C.

This means that the driver can be operated in this application up to the MAX6920's +125°C maximum operating temperature.

Power-Supply Considerations

The MAX6920 operates with multiple power-supply voltages. Bypass the V_{CC} and V_{BB} power-supply pins to GND with a 0.1µF capacitor close to the device. For multiplex applications, it may be necessary to add an additional 1µF bulk electrolytic capacitor, or greater, to the V_{BB} supply.

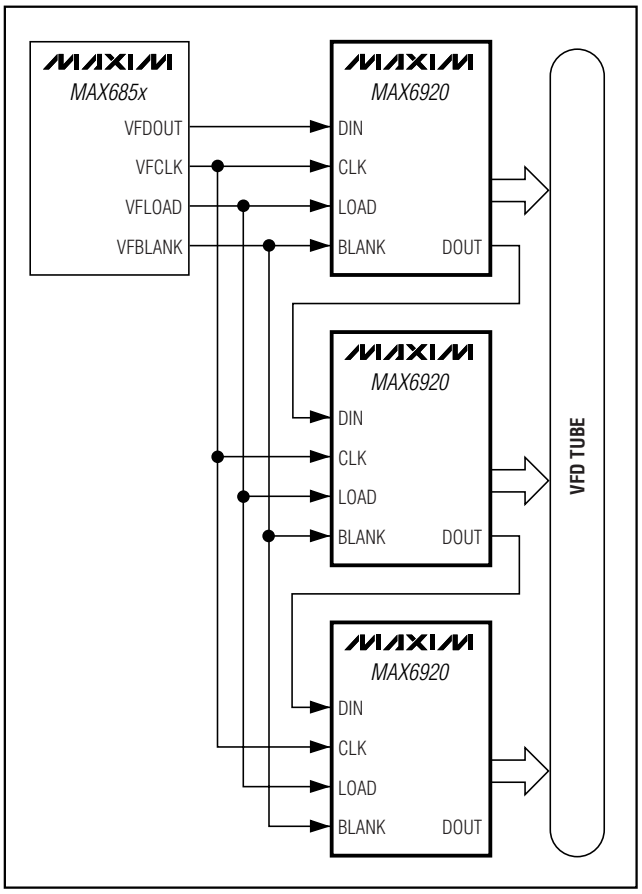
Power-Supply Sequencing

The order of the power-supply sequencing is not important. The MAX6920 will not be damaged if either V_{CC} or V_{BB} is grounded (or maintained at any other voltage below the data sheet minimum), while the other supply is maintained up to its maximum rating. However, as with any CMOS device, do not drive the MAX6920's logic inputs if the logic supply V_{CC} is not operational because the input protection diodes clamp the signals.

Chip Information

TRANSISTOR COUNT: 2743
PROCESS: BiCMOS

Typical Application Circuit

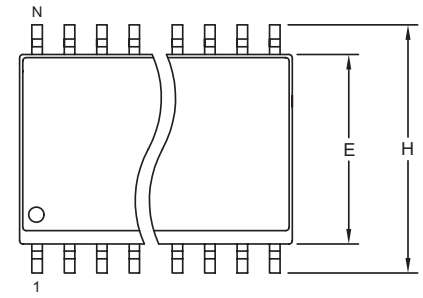


12-Output, 76V, Serial-Interfaced VFD Tube Driver

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

SOICW.EPS

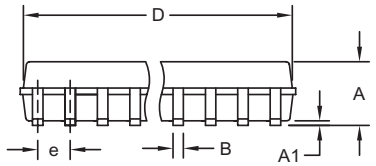


TOP VIEW

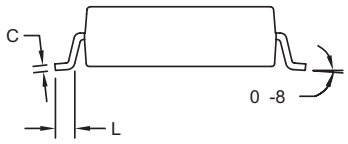
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.014	0.019	0.35	0.49
C	0.009	0.013	0.23	0.32
e	0.050		1.27	
E	0.291	0.299	7.40	7.60
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27

VARIATIONS:

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	N	MS013
D	0.398	0.413	10.10	10.50	16	AA
D	0.447	0.463	11.35	11.75	18	AB
D	0.496	0.512	12.60	13.00	20	AC
D	0.598	0.614	15.20	15.60	24	AD
D	0.697	0.713	17.70	18.10	28	AE



FRONT VIEW



SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.
5. MEETS JEDEC MS013.
6. N = NUMBER OF PINS.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, .300" SOIC

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0042	B	1/1