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This version: Jan. 1998
Previous version: Nov. 1996

OKI Semiconductor

MSM6926/6946

300 bps Single Chip FSK MODEM

GENERAL DESCRIPTION

The MSM6926 and the MSM6946 are OKI's 300 bps single chip modem series which transmit and receive serial, binary data over a switched telephone network using frequency shift keying (FSK). The MSM6926 is compatible with ITU-T V.21 series data sets, while the MSM6946 is compatible with Bell 103 series data sets.

These devices provide all the necessary modulation, demodulation, and filtering required to implement a serial, asynchronous communication link.

OKI's single chip modem series is designed for users who are not telecommunication experts and are easy to use cost effective alternative to standard discrete modem design.

CMOS LSI technology provides the advantages of small size, low power, and increased reliability.

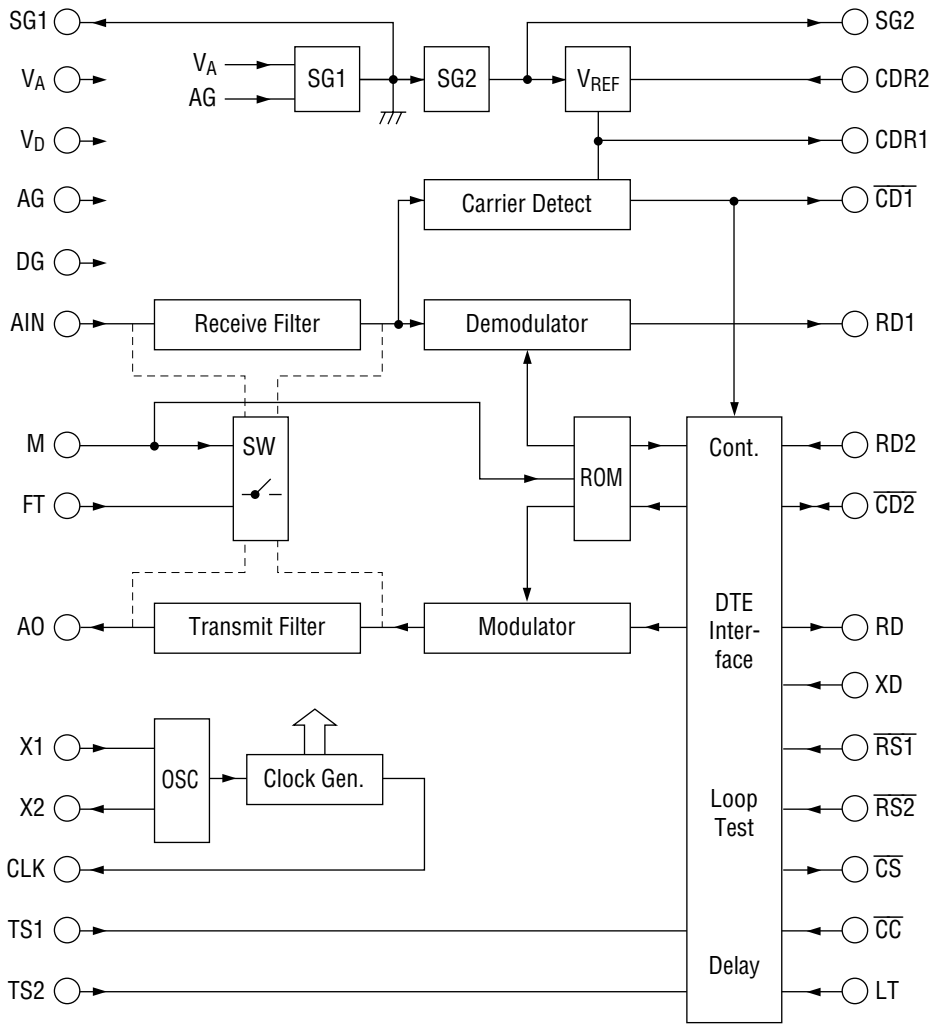
The design of the integrated circuit assures compatibility with a broad base of installed low speed modems and acoustic couplers. Applications include interactive terminals, desk top computers, point of sale equipment, and credit verification systems.

FEATURES

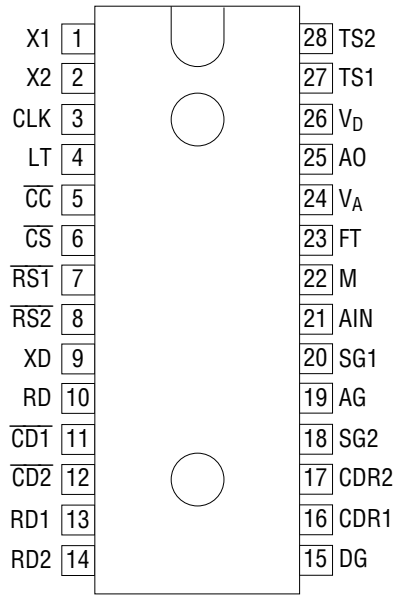
- Compatible with ITU-T V.21 (MSM6926)
- Compatible with BELL 103 (MSM6946)
- CMOS silicon gate process
- Switched capacitor and advanced CMOS analog technology
- Data rate from 0 to 300 bps
- Full duplex (2-Wire)
- Originate and Answer modes
- Selectable built-in timers and external delay timers possible
- All filtering, modulation, demodulation, and DTE interface on chip
- TTL compatible digital interface
- Low power dissipation: 90 mW Typ.
- Package options:

28-pin plastic DIP	(DIP28-P-600-2.54)	(Product name: MSM6926RS)
		(Product name: MSM6946RS)
44-pin plastic QFP	(QFP44-P-910-0.80-K)	(Product name: MSM6926GS-K)
		(Product name: MSM6946GS-K)
	(QFP44-P-910-0.80-2K)	(Product name: MSM6926GS-2K)
		(Product name: MSM6946GS-2K)

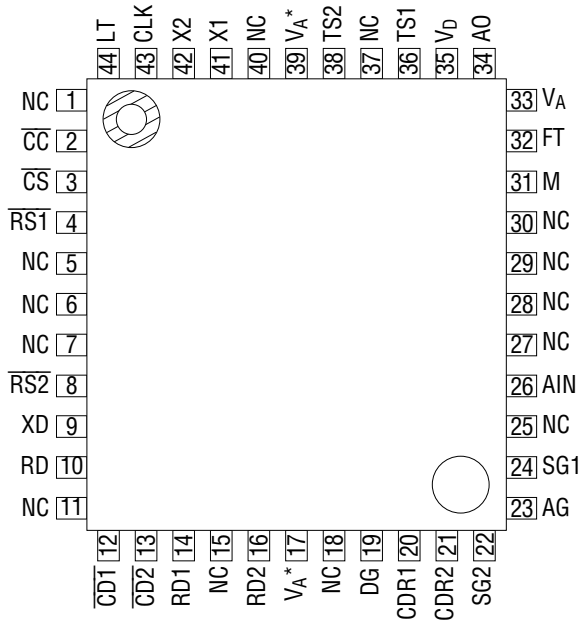
BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



28-Pin Plastic DIP



44-Pin Plastic QFP

Note: *: Both No. 17 pin and No. 39 pin are set to be at V_A level by setting No. 33 pin at V_A level.

NC: No connect pin

PIN DESCRIPTIONS

Power

Name	Pin No.		I/O	Description
	RS	GS-K		
DG	15	19	—	Ground reference of V_D (digital ground)
AG	19	23	—	Ground reference of V_A (digital ground)
V_A	24	33	—	Supply voltage (+12 V nominal)
V_D	26	35	—	Supply voltage (+5 V nominal)

Clocks

Name	Pin No.		I/O	Description
	RS	GS-K		
X1	1	41	—	Master clock timing is provided by either a series resonant crystal (3.579545 MHz ±0.01%) connected across X1 and X2, or by an external TTL/CMOS clock driving X2 with AC coupling. In this latter case, X1 is left unconnected. See Fig. 10.
X2	2	42	—	
CLK	3	43	O	873.9 Hz clock output. This clock is used to implement external delay circuits etc.

Control

Name	Pin No.		I/O	Description
	RS	GS-K		
LT	4	44	I	Digital loop back test. During digital "High", any data sent on the X_D pin will appear on the RD pin, and any data sent on the $\overline{RS1}$ pin will immediately appear on the $\overline{CS}$ pin. Any data demodulated from the received carrier on the A_{IN} pin will be the modulated data to implement the transmitted carrier. In this case, sending the transmitted carrier to the phone line depends on the $\overline{CC}$, but never on $\overline{RS1}$.
$\overline{CC}$	5	2	I	During digital loop back test, the data on this pin becomes a control signal for sending the transmitted carrier to the phone line in place of $\overline{RS1}$.
$\overline{RS2}$	8	8	I	When an external circuit gives the RS/CS delay time which is not within the device as required, this pin should be connected to the external circuit output. See Fig. 11.
$\overline{CD1}$	11	12	O	The fast carrier detection output. This pin is internally connected to the input of the built-in carrier detect delay circuit. When an external delay circuit provides the delay time which is not within the device as required, the $\overline{CD1}$ should be connected to the external circuit input. See Fig. 11.
$\overline{CD2}$	12	13	I/O	When an external circuit gives the carrier detect delay time which is not within the device as required, this pin becomes the input pin for the external circuit output signal. In other cases (when using the delay time within the device, the data on the TS1 or TS2 is not digital "High"), this pin becomes the Carrier detect signal output.
RD1	13	14	O	The RD1 data is demodulated data from the received carrier and the RD2 is the input of the following logic circuits referred to in Fig. 12. Usually, the RD1 data is input directly to RD2. In some cases, as input data to RD2, the data that is controlled by NCU (Network control unit) etc. may be required in stead of the RD1 data.
RD2	14	16	I	
CDR1	16	20	O	These two pins are the output (CRD1) and inverting input (CDR2) of the buffer operational amplifier of which the noninverting input is connected to the built-in voltage reference, stabilized to variations in the supply voltage and temperature. See Fig. 13. An adequate carrier-detect level can be set by selecting the ratio of R_8 to R_9. Therefore, the loss in the received carrier level by phone-line transformer can be compensated by adjusting the ratio of R_8 to R_9. $R_8 + R_9$ should be greater than 50 kΩ.
CDR2	17	21	I	
M	22	31	I	Answer/Originate mode select. During digital "High", the originate mode is selected. A low input selects the answer mode.
FT	23	32	I	This pin may be used for device tests only. During digital "High", the A_O pin will be connected to receiving filter output instead of transmitting filter output.
TS1	27	36	I	RS/CS delay and carrier detect delay options referred to chapter about timing characteristics are selected by TS1 and TS2 inputs. Be careful that each delay can not be individually selected. If another delay time than the ones within the device are required as an option, input a digital "High" to the TS1 and TS2 pin and implement the external delay circuits to obtain the desired delay characteristics. In this case, the CD2 pin becomes not only the input for the external circuit output signal, but also the Carrier detect output. See Fig. 11.
TS2	28	38	I	

Input/Output

Name	Pin No.		I/O	Description
	RS	GS-K		
$\overline{CS}$	6	3	O	Clear to send signal output. The digital "High" level indicates the "OFF" state and digital "Low" indicates the "ON" state. This output goes "Low" at the end of a delay (RS/CS delay) initiated when $\overline{RS1}$ (Request to send) goes "Low".
$\overline{RS1}$	7	4	I	Request to send signal input. The digital "High" level indicates the "OFF" state. The digital "Low" level indicates the "ON" state and instructs the modem to enter the transmit mode. This input must remain "Low" for the duration of data transmission. "High" turns the transmitter off.
XD	9	9	I	This is digital data to be modulated and transmitted via A_O. Digital "High" will be transmitted as "Mark". Digital "Low" will be transmitted as "Space". No signal appears at A_O unless $\overline{RS1}$ is "Low".
RD	10	10	O	Digital data demodulated from A_{IN} is serially available at this output. Digital "High" indicates "Mark" and digital "Low" indicates "Space". For example, under the following condition, this output is forced to be "Mark" state because the data may be invalid. • When $\overline{CD2}$ (Carrier detect) is in the "OFF" state.
SG2	18	22	O	The SG1 and ST2 are built-in analog signal grounds. SG2 is used only for Carrier detect function. The DC voltage of SG1 is approximately 6 V, so the analog line interface must be implemented by AC coupling. See Fig. 9. To make impedance lower and ensure the device performance, it is necessary to put bypass capacitors on SG1 and SG2 in close physical proximity to the device.
SG1	20	24	O	
A_{IN}	21	26	I	This is the input for the analog signal from the phone line. The modem extracts the information in this modulated carrier and converts it into a serial data stream for presentation at RD output.
A_O	25	34	O	This analog output is the modulated carrier to be conditioned and sent over the phone line.

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Condition	Rating	Unit
Power Supply Voltage		V_A	Ta = 25°C With respect to AG or DG	–0.3 to 15	V
		V_D		–0.3 to 7	
Analog Input Voltage	*1	V_{IA}		–0.3 to V_A + 0.3	
Digital Input Voltage	*2	V_{ID}		–0.3 to V_D + 0.3	
Operating Temperature		T_{op}	—	0 to +70	°C
Storage Temperature		T_{STG}	—	–55 to 150	

*1 CDR2, A_{IN}

*2 X1, LT, $\overline{CC}$, $\overline{RS1}$, $\overline{RS2}$, XD, $\overline{CD2}$*3, RD2, M, FT, T_{S1}, T_{S2}

*3 $\overline{CD2}$ is I/O terminal

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	VA	With respect to AG	10.8	12.0	13.2	V
	VD	With respect to DG	4.75	5.00	5.25	
	AG, DG	—	—	0	—	
Operating Temperature	T_{op}	—	0	—	70	°C
CRYSTAL	—	—	—	3.579545	—	MHz
R_1	—	Transformer impedance = 600 Ω	—	600	—	Ω
R_2	—	—	—	51	—	kΩ
R_3	—		—	51	—	
R_4	—		—	51	—	
R_5	—		—	51	—	
R_6	—		—	51	—	
R_7	—		—	51	—	
R_8	—		—	33	—	
R_9	—		—	51	—	
C_0, C_1	—	—	—	0.047	—	µF
C_2	—		—	2.2	—	
C_3	—		22	—	—	
C_4	—		0.01	—	—	
C_5	—		—	10	—	
C_6	—		—	10	—	

Application circuits using above conditions are provided in Fig. 8.

ELECTRICAL CHARACTERISTICS

DC and Digital Interface Characteristics

(V_A = 12 V ±10%, V_D = 5 V ±5%, Ta = 0 to 70°C)

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Current		I_A	Ordinary operation	—	7.5	15.0	mA
		I_D		—	1.0	2.0	
Input Leakage Currnet	*1	I_{IL}	V_I = 0 V	–10	—	10	µA
		I_{IH}	$V_I = V_D$	–10	—	10	
Input Voltage	*1	V_{IL}	—	0	—	0.8	V
		V_{IH}	—	2.2	—	V_D	
Output Voltage	*2	V_{OL}	I_{OL} = 1.6 mA	0	—	0.4	
		V_{OH}	I_{OH} = 400 µA	0.8 × VD	—	V_D	

*1 LT, $\overline{CC}$, $\overline{RS1}$, $\overline{RS2}$, XD, $\overline{CD2}$ (*3), RD2, M, FT, T_{S1}, T_{S2}

*2 CLK, $\overline{CS}$, RD, $\overline{CD1}$, $\overline{CD2}$ (*3), RD1

*3 $\overline{CD2}$ is I/O terminal.

Analog Interface Characteristics

1. MSM6926

Transmit carrier out (A_O)

(V_A = 12 V ±10%, V_D = 5 V ±5%, Ta = 0 to 70°C)

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit
ORIGINATE MODE Carrier Frequency	Mark 1	f_{OM}	$f_{CRYSTAL}$ = 3.579545 MHz	974	980	986	Hz
	Space 0	f_{OS}		1174	1180	1186	
ANSWER MODE Carrier Frequency	Mark 1	f_{AM}		1644	1650	1656	
	Space 0	f_{AS}		1844	1850	1856	
Output Resistance		R_{OXA}	—	—	—	200	Ω
Load Resistance		R_{LXA}	—	50	—	—	kΩ
Load Capacitance		C_{LXA}	—	—	—	100	pF
Transmit Level		V_{OXA}	—	4	6	8	*1 dBm
Output Offset Voltage		V_{OSX}	—	$\frac{V_A}{2}$ –1	$\frac{V_A}{2}$	$\frac{V_A}{2}$ + 1	V
Out-of-Band Energy (Referred to Carrier Level)		E_{OX}	C_1 = 0.047 µF	Refer to Fig. 1			dB

Receive carrier input (A_{IN})

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit
Input Resistance		R_{IRA}	—	100	—	—	kΩ
Receive Signal Level Range		V_{IRA}	—	–48	—	–6	*1 dBm
Carrier Detect Level	ON	V_{CD} ON	R_8 = 33 kΩ *2 R_9 = 51 kΩ	—	—	–43	
	OFF	V_{CD} OFF		–48	—	—	
Carrier Detect Hysteresis		H_{YS}	V_{CD} ON – V_{CD} OFF	2	—	—	dB

Receive filter

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Group Delay Distortion	D_{DL}	ORIG. MODE	1600 to 1900 Hz	—	800	—	µs
		ANS. MODE	930 to 1230 Hz	—	850	—	
Adjacent Channel Rejection	L_{AC}	V_{AIN} = –6 dBm		50	—	—	dB

Notes: *1 0 dBm = 0.775 Vrms
*2 The resistor values are typical

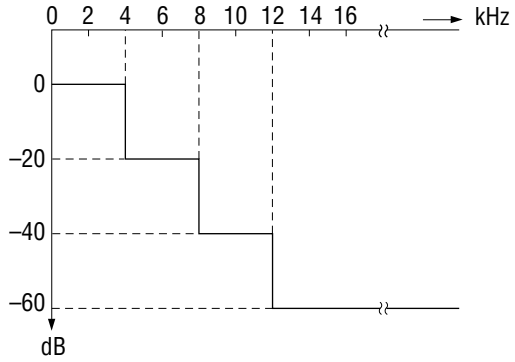


Figure 1 MSM6926 Out-of-Band Energy Referred to Carrier Level (C_1 = 0.047 μF)

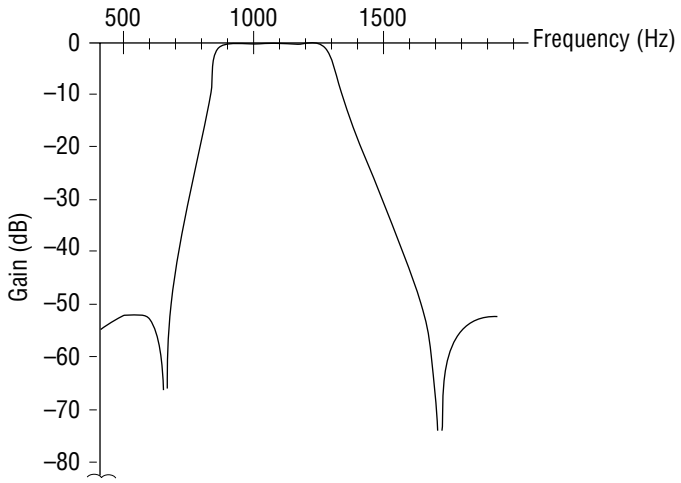


Figure 2 MSM6926 Low Band Filter

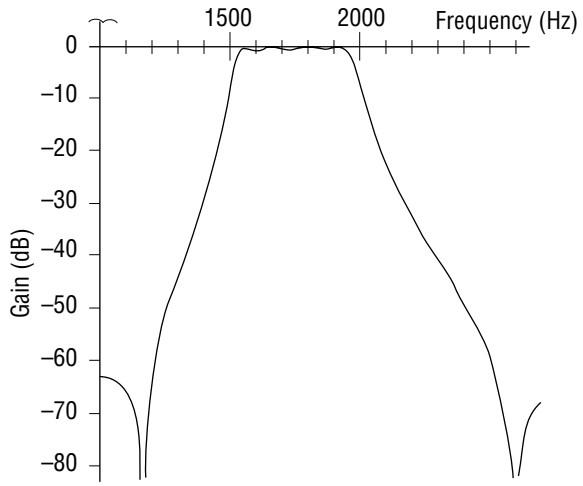


Figure 3 MSM6926 High Band Filter

2. MSM6946

Transmit carrier out (A_O)

(V_A = 12 V ±10%, V_D = 5 V ±5%, Ta = 0 to 70°C)

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit
ORIGINATE MODE Carrier Frequency	Mark 1	f_{OM}	$f_{CRYSTAL}$ = 3.579545 MHz	1264	1270	1276	Hz
	Space 0	f_{OS}		1064	1070	1076	
ANSWER MODE Carrier Frequency	Mark 1	f_{AM}		2219	2225	2231	
	Space 0	f_{AS}		2019	2025	2031	
Output Resistance		R_{OXA}	—	—	—	200	Ω
Load Resistance		R_{LXA}	—	50	—	—	kΩ
Load Capacitance		C_{LXA}	—	—	—	100	pF
Transmit Level		V_{OXA}	—	4	6	8	*1 dBm
Output Offset Voltage		V_{OSX}	—	$\frac{V_A}{2}$ –1	$\frac{V_A}{2}$	$\frac{V_A}{2}$ + 1	V
Out-of-Band Energy (Referred to Carrier Level)		E_{OX}	C_1 = 0.047 µF	Refer to Fig. 4			dB

Receive carrier input (A_{IN})

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit
Input Resistance		R_{IRA}	—	100	—	—	kΩ
Receive Signal Level Range		V_{IRA}	—	–48	—	–6	*1 dBm
Carrier Detect Level	ON	V_{CD} ON	R_8 = 33 kΩ *2 R_9 = 51 kΩ	—	—	–43	
	OFF	V_{CD} OFF		–48	—	—	
Carrier Detect Hysteresis		H_{YS}	V_{CD} ON – V_{CD} OFF	1.5	—	—	dB

Receive Filter

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Group Delay Distortion	D_{DL}	ORIG. MODE	1975 to 2275 Hz	—	650	—	µs
		ANS. MODE	1020 to 1320 Hz	—	750	—	
Adjacent Channel Rejection	L_{AC}	V_{AIN} = –6 dBm		50	—	—	dB

Notes: *1 0 dBm = 0.775 Vrms
*2 The resistor values are typical

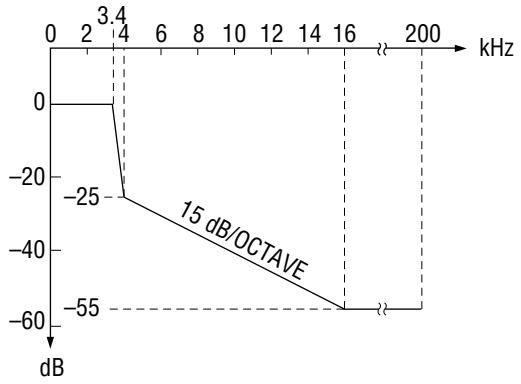


Figure 4 MSM6946 Out-of-Band Energy Referred to Carrier Level (C_1 = 0.047 μF)

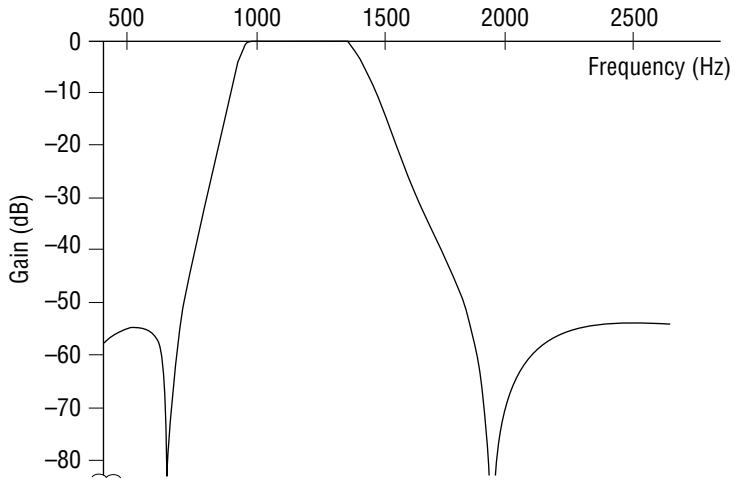


Figure 5 MSM6946 Low Band Filter

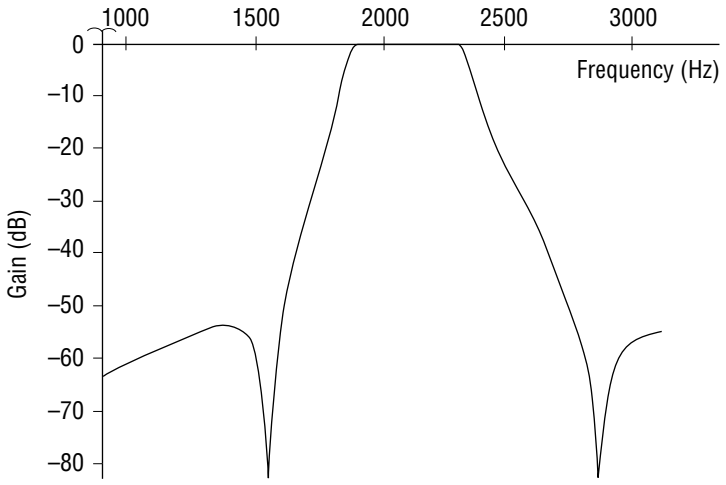


Figure 6 MSM6946 High Band Filter

Demodulated Bit Characteristics

(V_A = 12 V ±10%, V_D = 5 V ±5%, Ta = 0 to 70°C)

Parameter	Symbol	Condition			Min.	Typ.	Max.	Unit
Peak Intersymbol Distortion	ID	Back-to-back over input signal range –6 to –40 dBm. 511-bit test pattern.			—	6	—	%
Bit Error Rate	BER	Back-to-back with 0.3 to 3.4 kHz flat noise. Receive signal level –25 dBm. 511-bit test pattern	S/N	5 dB	—	10^{-5}	—	
				—				

Timing Characteristics

1. MSM6926

(V_A = 12 V ±10%, V_D = 5 V ±5%, Ta = 0 to 70°C)

Parameter	Symbol	Condition	TS2	TS1	Min.	Typ.	Max.	Unit
RS/CS Delay Time	T_{RC} ON	$\overline{RS1}$ = "0" → $\overline{CS}$ = "0"	0	0	395	400	405	ms
			0	1	25	30	35	
			1	0	345	350	355	
			1	1	External delay timer			
	T_{RC} OFF	$\overline{RS1}$ = "1" → $\overline{CS}$ = "1"	*	*	0	—	0.5	
CD/ON Delay Time	T_{CD} ON	—	0	0	300	—	320	
			0	1	5	—	20	
			1	0	150	—	170	
			1	1	External delay timer			
CD/OFF Delay Time	T_{CD} OF	—	0	0	20	—	70	
			0	1	20	—	70	
			1	0	10	—	40	
			1	1	External delay timer			
Soft Turn-OFF Time	T_{ST}	—	*	*	—	10	—	

Refer to Fig. 7
Notes: *: Irrespective of I/O condition

2. MSM6946

(V_A = 12 V ±10%, V_D = 5 V ±5%, Ta = 0 to 70°C)

Parameter	Symbol	Condition	TS2	TS1	Min.	Typ.	Max.	Unit
RS/CS Delay Time	T_{RC} ON	$\overline{RS1}$ = "0" → $\overline{CS}$ = "0"	0	0	195	200	205	ms
			0	1	—	+	—	
			1	0	—	+	—	
			1	1	External delay timer			
	T_{RC} OFF	$\overline{RS1}$ = "1" → $\overline{CS}$ = "1"	*	*	0	—	0.5	
CD/ON Delay Time	T_{CD} ON	—	0	0	100	—	120	
			0	1	—	+	—	
			1	0	—	+	—	
			1	1	External delay timer			
CD/OFF Delay Time	T_{CD} OF	—	0	0	10	—	50	
			0	1	—	+	—	
			1	0	—	+	—	
			1	1	External delay timer			
Soft Turn-OFF Time	T_{ST}	—	*	*	—	10	—	

Refer to Fig. 8

Notes: *: Irrespective of I/O condition

+: Reserved

TIMING DIAGRAM

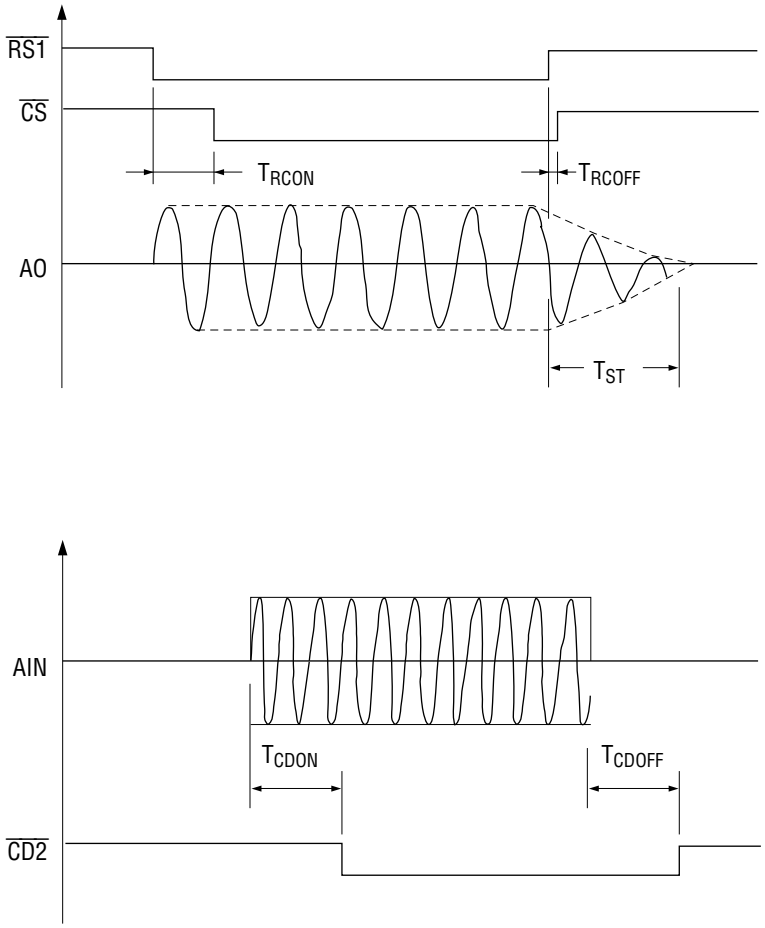
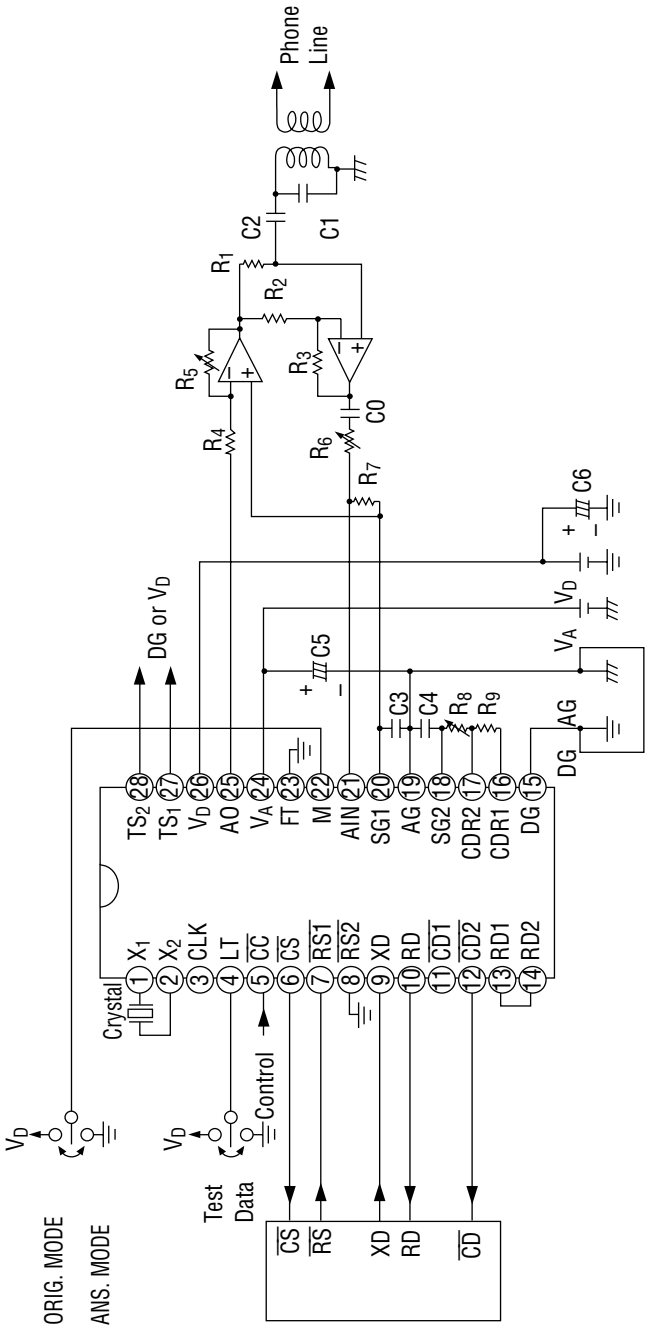


Figure 7 MSM6926/6946 Timing Diagram

APPLICATION CIRCUIT



Notes: 1. The crystal should be wired in close physical proximity to the device.
2. High level signals should not be routed next to low level signals.
3. Bypass capacitors on V_A, SG1, and SG2 should be as close to the device as possible.
4. AG and DG should be connected as close to the system ground as possible.

Figure 8 Application Circuit Using MSM6926RS/MSM6946RS

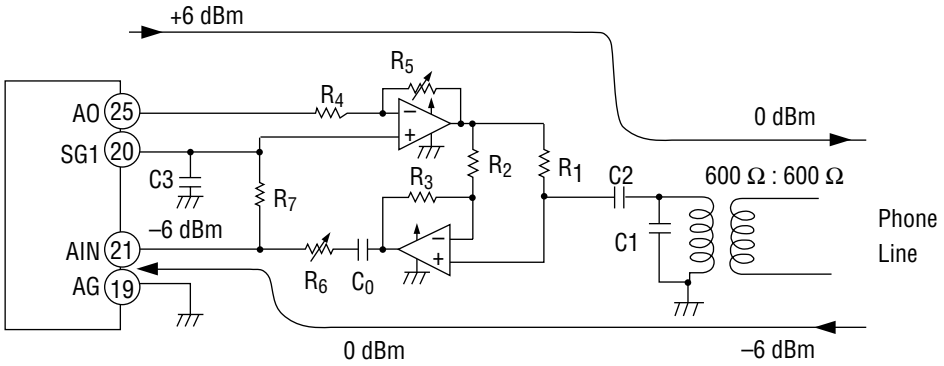
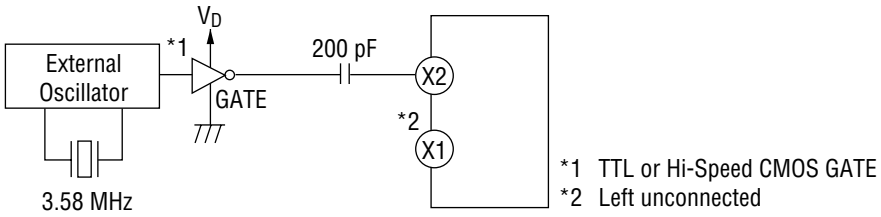


Figure 9 MSM6926RS/MSM6946RS Application

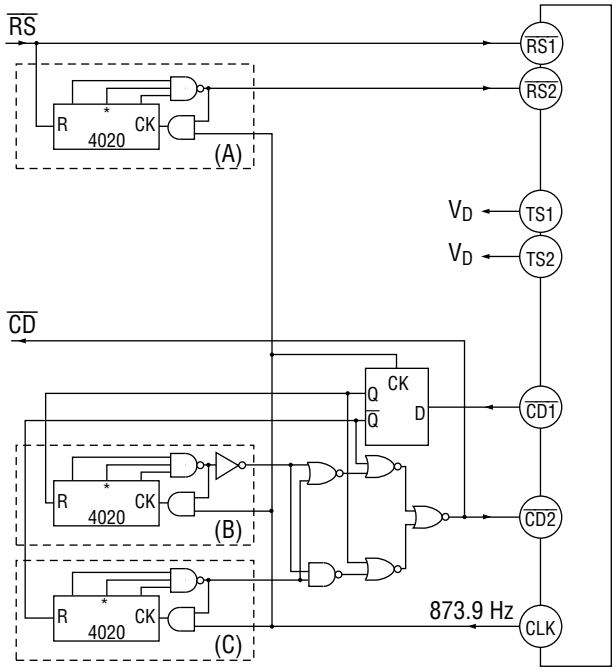
C_0, C_1	0.047 µF	R_2	51 kΩ	R_6	(51 kΩ) Receive signal level
C_2	2.2 µF	R_3	51 kΩ	R_7	51 kΩ
C_3	1 µF	R_4	51 kΩ	R_8	(33 kΩ) Carrier detect level
R_1	600 Ω	R_5	(51 kΩ) Transmit signal level	R_9	51 kΩ

Note: The signal level on the A_{IN} pin should not exceed –6 dBm.



External Oscillator Connection

Figure 10



(A) RS/CS delay, (B) CD/ON delay, (C) CD/OFF delay
Note: Supply voltage equals V_D for all gates.
*: The desired delay can be realized by selecting the appropriate bits from 4020's outputs. The number of the bits is not always 3. Each delay can be set differently from built-in delays.

Figure 11 External Delays Connection

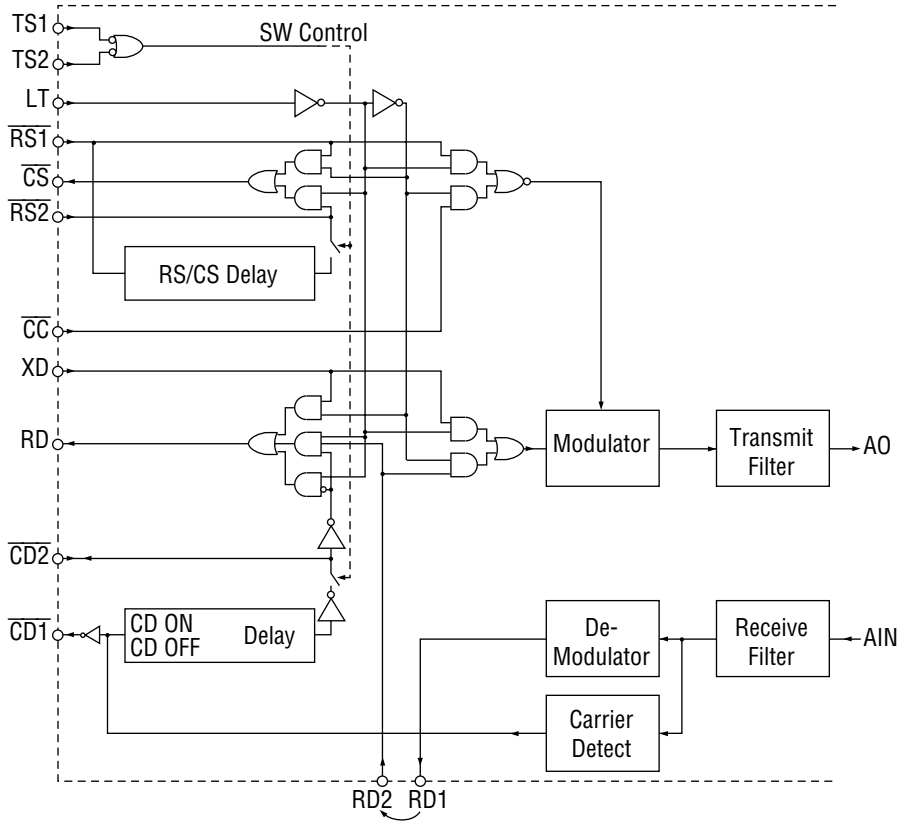


Figure 12 Equivalent Logic Interface of the Integrated Modem

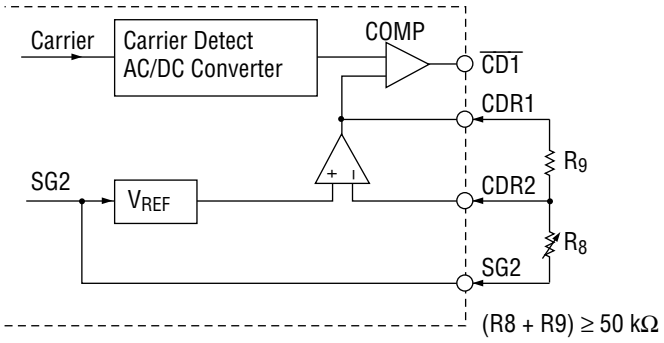
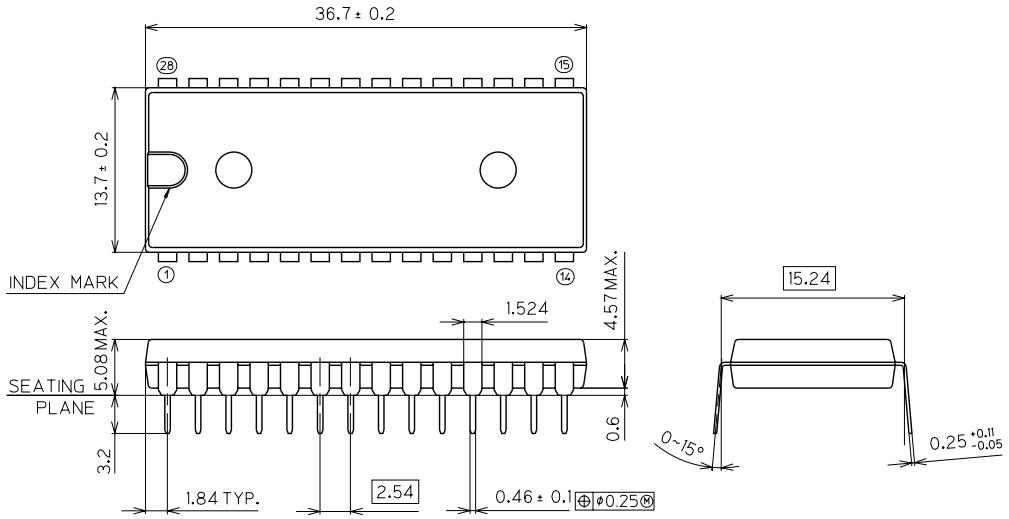


Figure 13 External Resistor Connection for the Setting of Carrier Detect Level

PACKAGE DIMENSIONS

(Unit : mm)

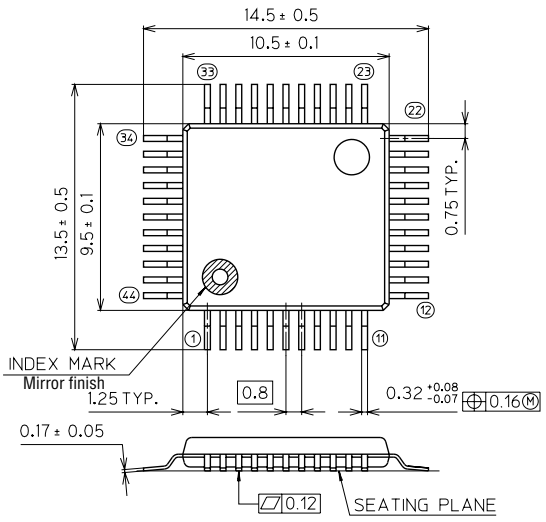
DIP28-P-600-2.54

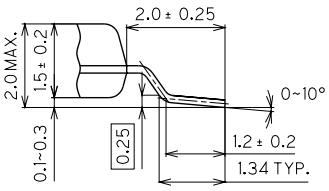


Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	4.30 TYP.

(Unit : mm)

QFP44-P-910-0.80-K





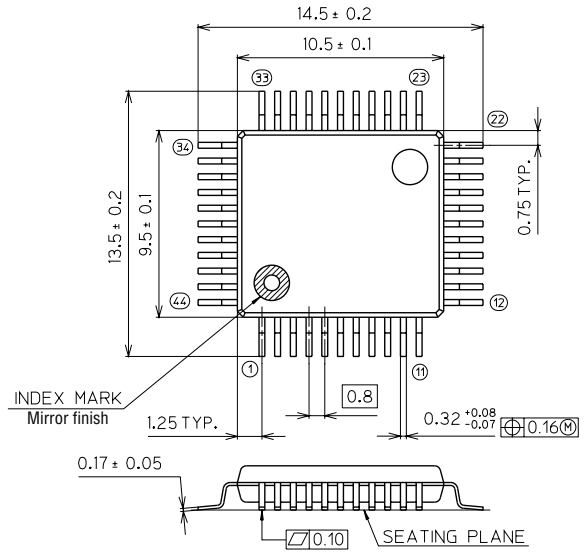
Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.35 TYP.

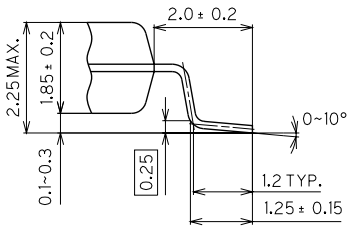
Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

QFP44-P-910-0.80-2K





Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.41 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).