

# SN54AC374, SN74AC374 OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

SCAS543E – OCTOBER 1995 - REVISED OCTOBER 2003

- 2-V to 6-V  $V_{CC}$  Operation
- Inputs Accept Voltages to 6 V
- Max  $t_{pd}$  of 9.5 ns at 5 V
- 3-State Noninverting Outputs Drive Bus Lines Directly
- Full Parallel Access for Loading

## description/ordering information

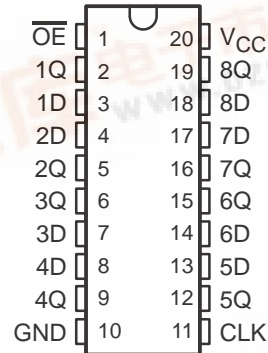
These 8-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. The devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the 'AC374 devices are D-type edge-triggered flip-flops. On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels set up at the data (D) inputs.

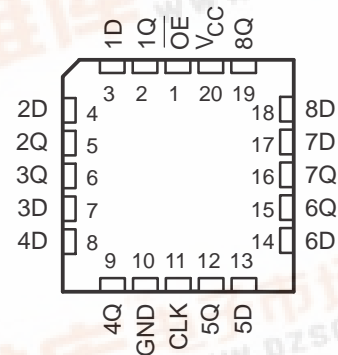
A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines in bus-organized systems without need for interface or pullup components.

$\overline{OE}$  does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

SN54AC374 . . . J OR W PACKAGE  
SN74AC374 . . . DB, DW, N, NS, OR PW PACKAGE  
(TOP VIEW)



SN54AC374 . . . FK PACKAGE  
(TOP VIEW)



## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube	SN74AC374N	SN74AC374N
	SOIC – DW	Tube	SN74AC374DW	AC374
		Tape and reel	SN74AC374DWR	
	SOP – NS	Tape and reel	SN74AC374NSR	AC374
	SSOP – DB	Tape and reel	SN74AC374DBR	AC374
-55°C to 125°C	TSSOP – PW	Tube	SN74AC374PW	AC374
		Tape and reel	SN74AC374PWR	
-55°C to 125°C	CDIP – J	Tube	SNJ54AC374J	SNJ54AC374J
	CFP – W	Tube	SNJ54AC374W	SNJ54AC374W
	LCCC – FK	Tube	SNJ54AC374FK	SNJ54AC374FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

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## recommended operating conditions (see Note 3)

		SN54AC374		SN74AC374		UNIT
		MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	2	6	2	6	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 3 V		2.1		V
		V <sub>CC</sub> = 4.5 V		3.15		
		V <sub>CC</sub> = 5.5 V		3.85		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 3 V		0.9		V
		V <sub>CC</sub> = 4.5 V		1.35		
		V <sub>CC</sub> = 5.5 V		1.65		
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 3 V		-12		mA
		V <sub>CC</sub> = 4.5 V		-24		
		V <sub>CC</sub> = 5.5 V		-24		
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 3 V		12		mA
		V <sub>CC</sub> = 4.5 V		24		
		V <sub>CC</sub> = 5.5 V		24		
Δt/Δv	Input transition rise or fall rate	8		8		ns/V
T <sub>A</sub>	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54AC374		SN74AC374		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	3 V	2.9			2.9		2.9	V	
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I <sub>OH</sub> = -12 mA	3 V	2.56			2.4		2.46		
		4.5 V	3.86			3.7		3.76		
		5.5 V	4.86			4.7		4.76		
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	3 V				0.1		0.1	V	
		4.5 V				0.1		0.1		
		5.5 V				0.1		0.1		
	I <sub>OL</sub> = 12 mA	3 V				0.36		0.44		
		4.5 V				0.36		0.44		
		5.5 V				0.36		0.44		
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V			±0.1		±1	±1	μA	
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V			±0.25		±5	±2.5	μA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			4		80	40	μA	
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		4.5					pF	

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timing requirements over recommended operating free-air temperature range,  $V_{CC} = 3.3 V \pm 0.3 V$  (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ C$		SN54AC374		SN74AC374		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$f_{clock}$	Clock frequency	60		60		60		MHz
$t_w$	Pulse duration, CLK high or low	5.5		6.5		6		ns
$t_{su}$	Setup time, data before CLK $\uparrow$	5.5		6.5		6		ns
$t_h$	Hold time, data after CLK $\uparrow$	1		1		1		ns

timing requirements over recommended operating free-air temperature range,  $V_{CC} = 5 V \pm 0.5 V$  (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ C$		SN54AC374		SN74AC374		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$f_{clock}$	Clock frequency	100		95		100		MHz
$t_w$	Pulse duration, CLK high or low	4		5		4.5		ns
$t_{su}$	Setup time, data before CLK $\uparrow$	4		5		4.5		ns
$t_h$	Hold time, data after CLK $\uparrow$	1.5		1.5		1.5		ns

switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 3.3 V \pm 0.3 V$  (unless otherwise noted) (see Figure 1)

PARAMETER	TO (INPUT)	TO (OUTPUT)	$T_A = 25^\circ C$			SN54AC374		SN74AC374		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{max}$			60	110		60		60	MHz	
$t_{PLH}$	CLK	Q	3	11	13.5	3	16.5	1.5	15.5	ns
$t_{PHL}$			2.5	10	12.5	3	15	2	14	
$t_{PZH}$	$\overline{OE}$	Q	3	9.5	11.5	1	14	1.5	13	ns
$t_{PZL}$			3.5	9	11.5	1	14	1.5	13	
$t_{PHZ}$	$\overline{OE}$	Q	3	10.5	12.5	1	16	2	14.5	ns
$t_{PLZ}$			2	8	11.5	1	13	1	12.5	

switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 5 V \pm 0.5 V$  (unless otherwise noted) (see Figure 1)

PARAMETER	TO (INPUT)	TO (OUTPUT)	$T_A = 25^\circ C$			SN54AC374		SN74AC374		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{max}$			100	155		95		100	MHz	
$t_{PLH}$	CLK	Q	2.5	8	9.5	3	12	1.5	10.5	ns
$t_{PHL}$			2	7	9	3	11	1.5	10	
$t_{PZH}$	$\overline{OE}$	Q	2	7	8.5	1.5	10	1	9.5	ns
$t_{PZL}$			2	6.5	8.5	1.5	10.5	1	9.5	
$t_{PHZ}$	$\overline{OE}$	Q	2	8	11	1.5	12.5	2	12.5	ns
$t_{PLZ}$			1.5	6.5	8.5	1.5	10.5	1	10	

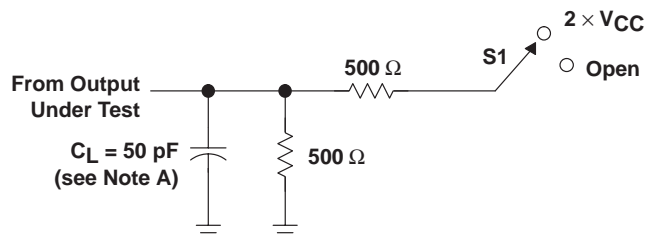
operating characteristics,  $V_{CC} = 5 V, T_A = 25^\circ C$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$	Power dissipation capacitance $C_L = 50 pF, f = 1 MHz$	40	pF

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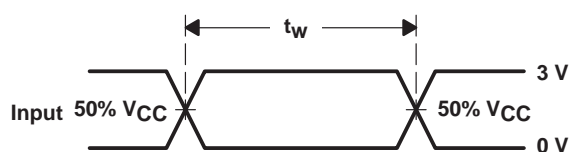
SCAS543E – OCTOBER 1995 - REVISED OCTOBER 2003

## PARAMETER MEASUREMENT INFORMATION

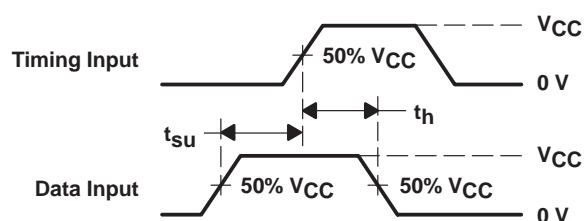


LOAD CIRCUIT

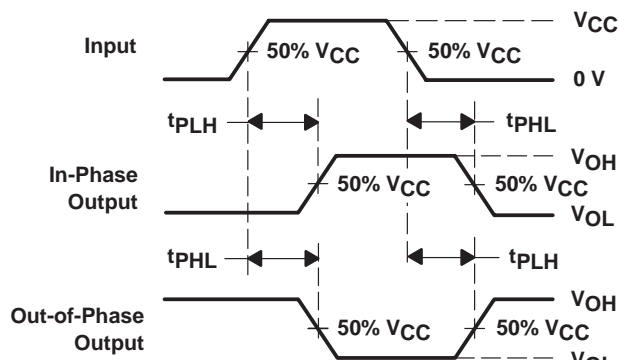
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	Open



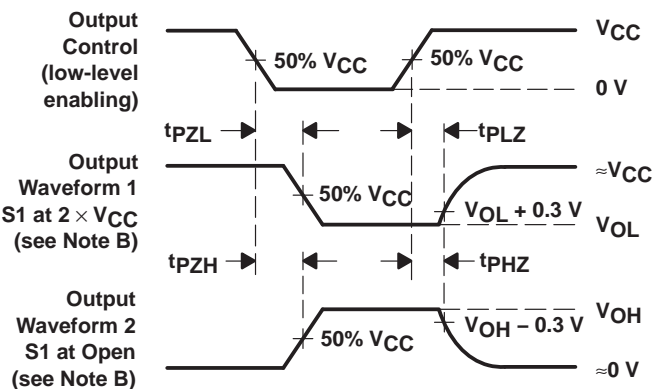
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
  - The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
5962-87694012A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
5962-8769401RA	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
5962-8769401SA	ACTIVE	CFP	W	20	1	TBD	Call TI	Level-NC-NC-NC
5962-8769401VRA	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
5962-8769401VSA	ACTIVE	CFP	W	20	1	TBD	Call TI	Level-NC-NC-NC
SN74AC374DBLE	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI
SN74AC374DBR	ACTIVE	SSOP	DB	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74AC374DBRE4	ACTIVE	SSOP	DB	20	2000	TBD	Call TI	Call TI
SN74AC374DW	ACTIVE	SOIC	DW	20	25	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN74AC374DWR	ACTIVE	SOIC	DW	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN74AC374N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74AC374NSR	ACTIVE	SO	NS	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74AC374PW	ACTIVE	TSSOP	PW	20	70	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74AC374PWE4	ACTIVE	TSSOP	PW	20	70	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74AC374PWLE	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI
SN74AC374PWR	ACTIVE	TSSOP	PW	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74AC374PWRE4	ACTIVE	TSSOP	PW	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SNJ54AC374FK	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54AC374J	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54AC374W	ACTIVE	CFP	W	20	1	TBD	Call TI	Level-NC-NC-NC

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

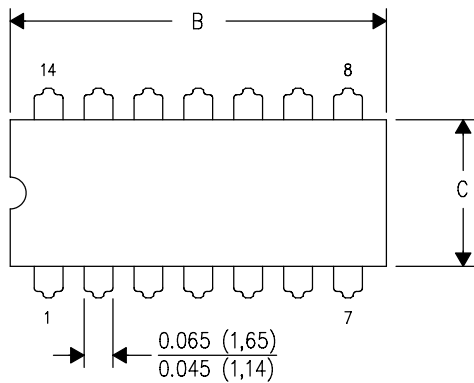
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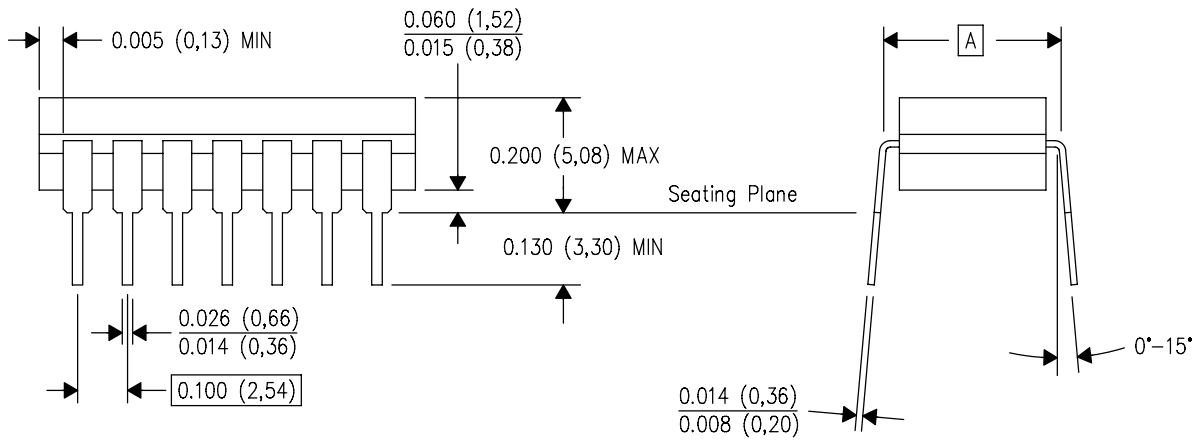
J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

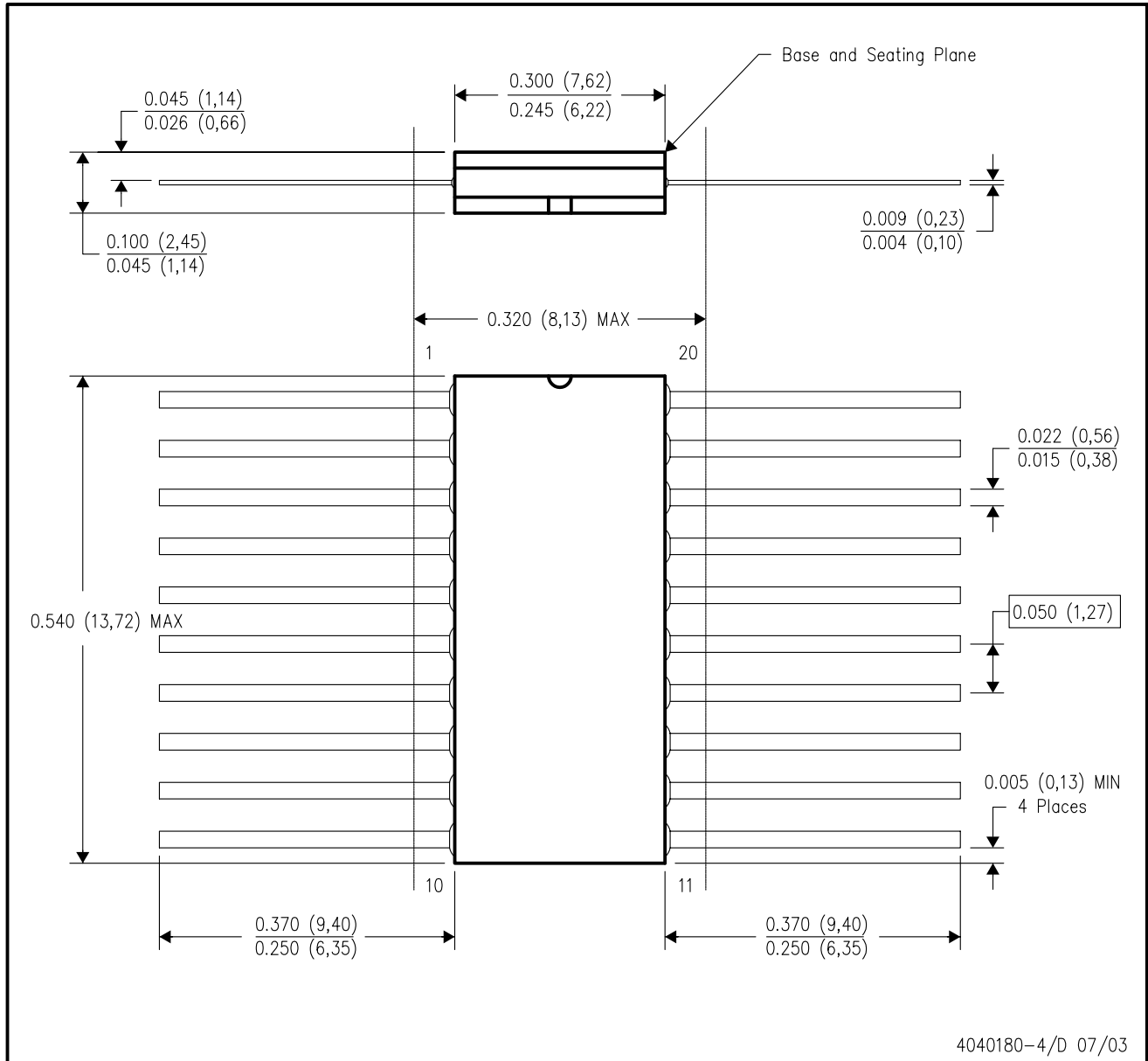
- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.



# MECHANICAL DATA

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only.
  - Falls within Mil-Std 1835 GDFP2-F20

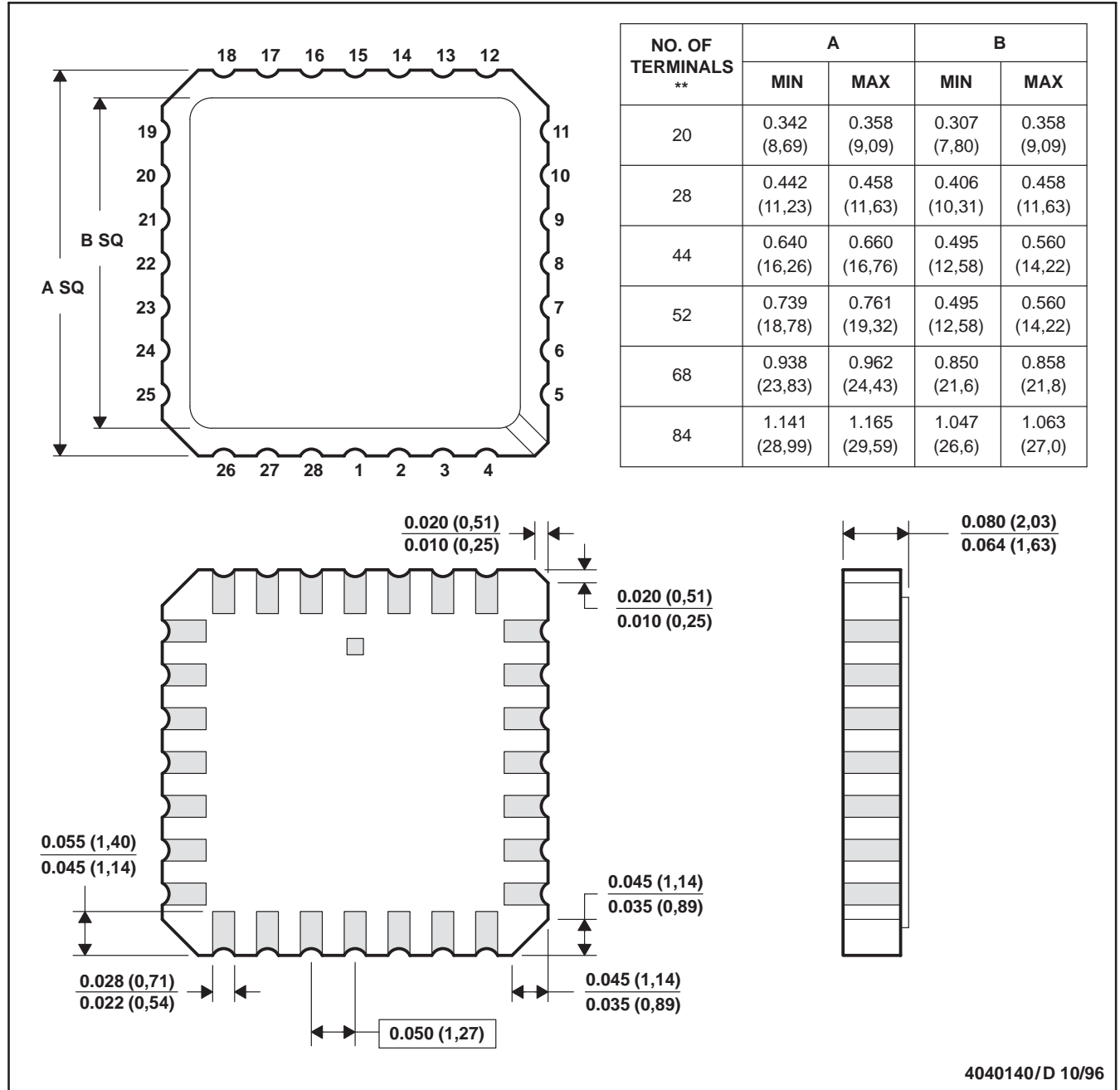
# MECHANICAL DATA

MLCC006B – OCTOBER 1996

## FK (S-CQCC-N\*\*)

## LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - The terminals are gold plated.
  - Falls within JEDEC MS-004

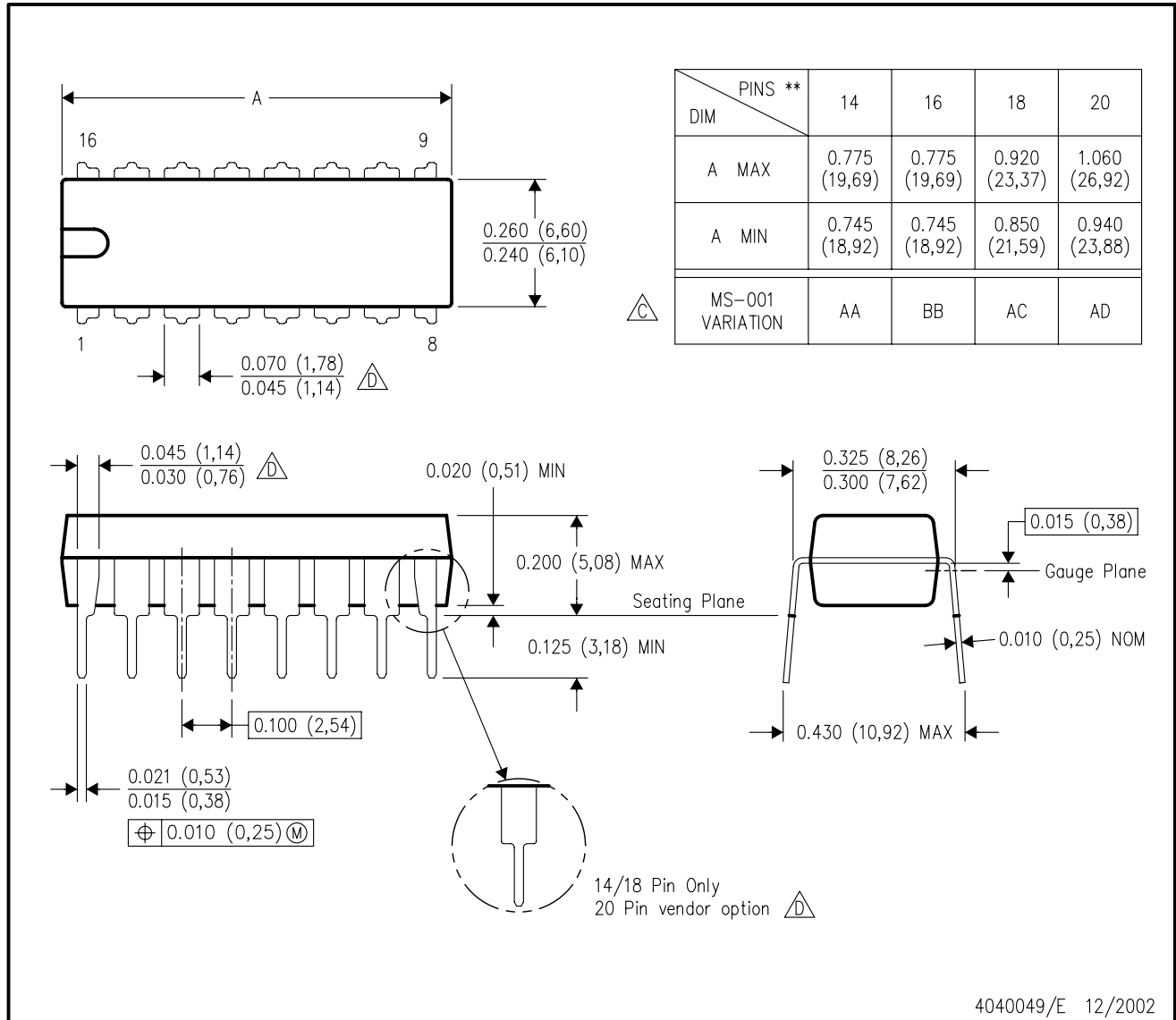
4040140/D 10/96

# MECHANICAL DATA

## N (R-PDIP-T\*\*)

16 PINS SHOWN

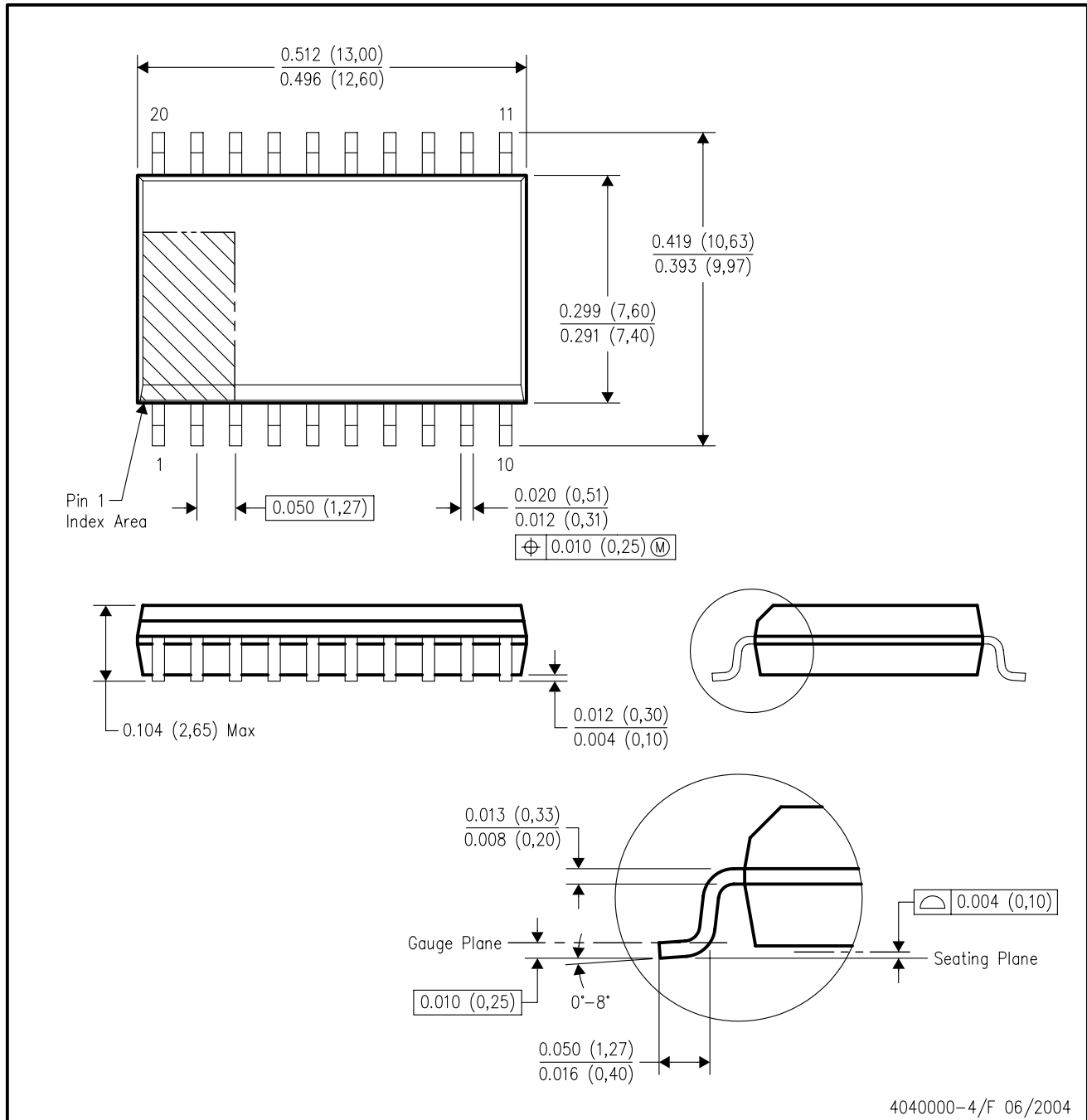
## PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



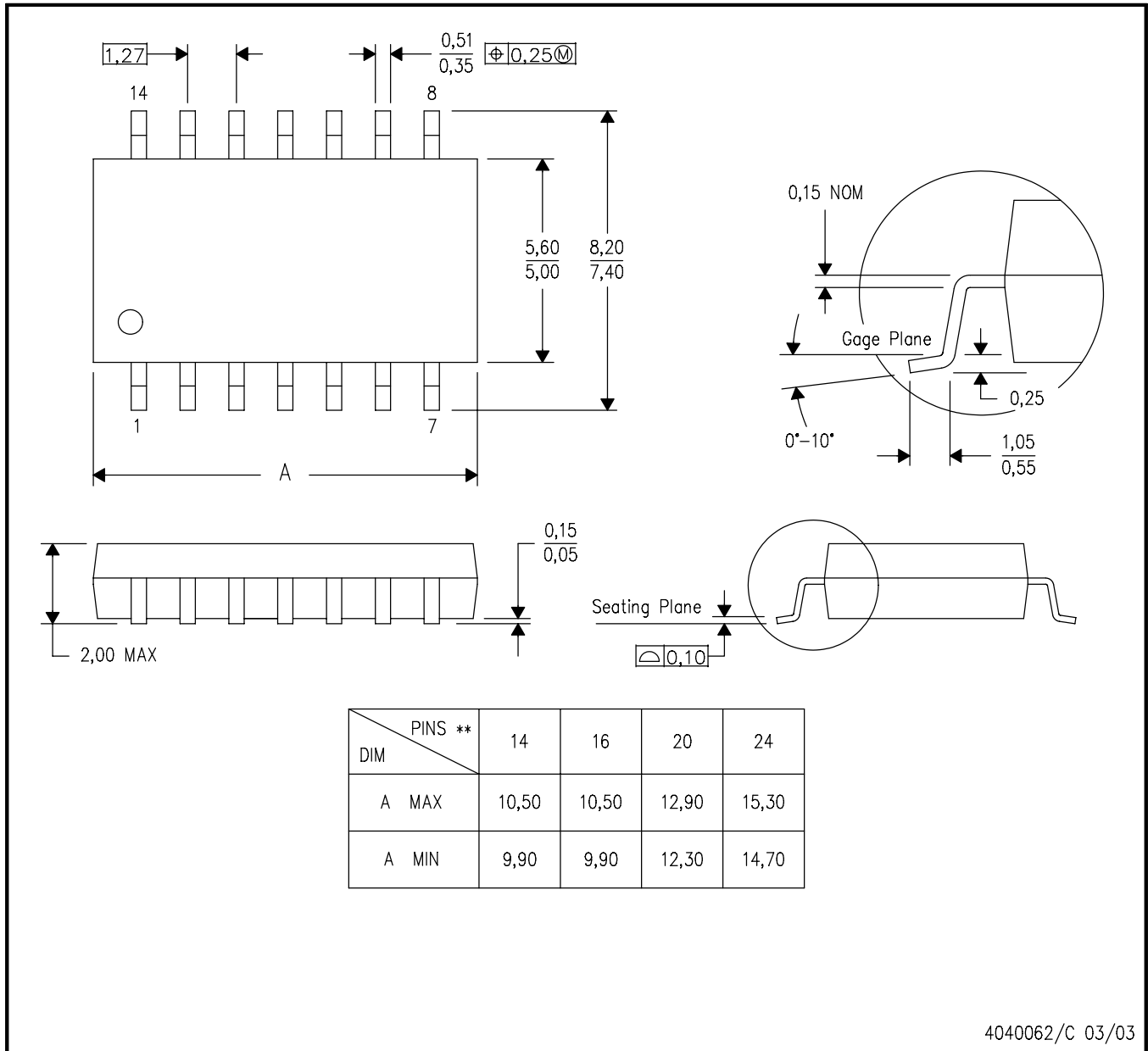
- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MS-013 variation AC.

## MECHANICAL DATA

**NS (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**



4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

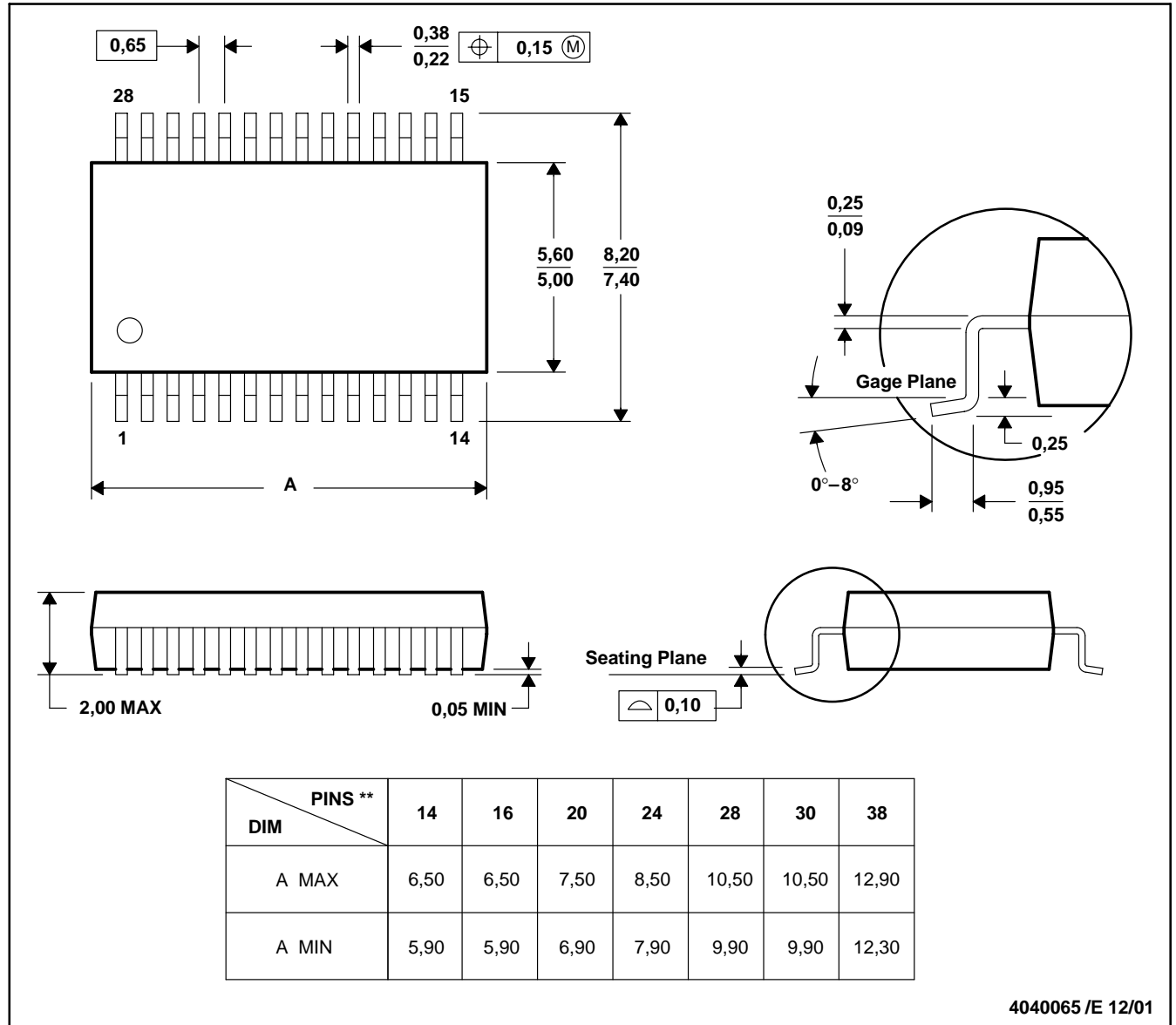
# MECHANICAL DATA

MSS0002E – JANUARY 1995 – REVISED DECEMBER 2001

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

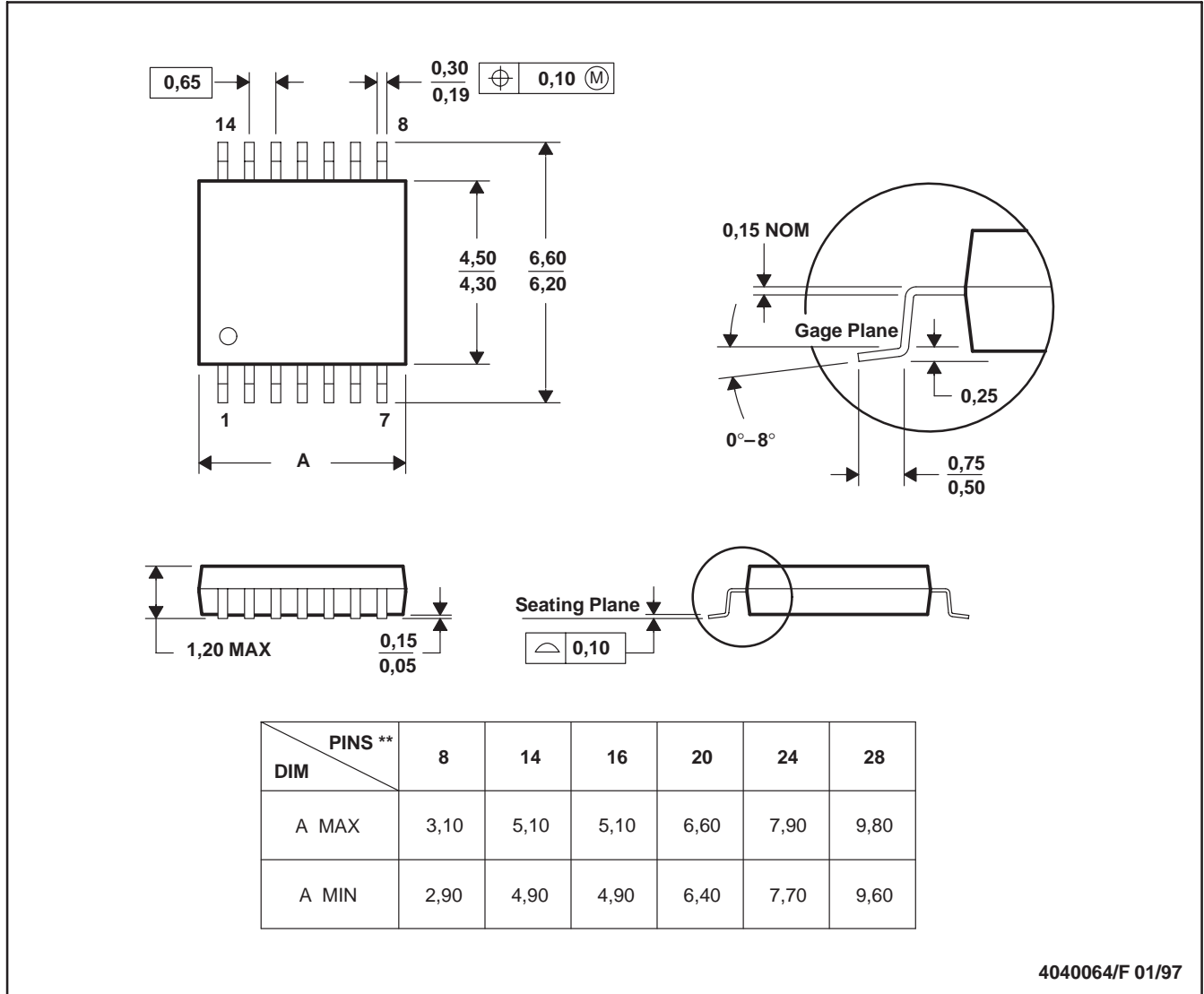
# MECHANICAL DATA

MTSS001C – JANUARY 1995 – REVISED FEBRUARY 1999

**PW (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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