

Structure Silicon Monolithic Integrated Circuit

Product LED Driver IC for Cellular

Type **BH6069GU**

Function •Built-in high efficiency charge pump circuit which can change automatically 1 time, 1.5 times and 2.0 times. (330mA/MAX)
•Built-in constant current LED driver 15ch controllable independent.
(Possible to set lighting sequence about LED12~15)
•Built-in LDO 2ch (2.6V, 1.8V ; IO=50mA) , GPI 3ch, GPO 2ch, GPIO 2ch

○Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Range	Unit	Condition
Maximum Supply Voltage	V _{MAX}	5.5	V	
Power Dissipation(*1)	Pd	1.63	W	
Operating Temperature range	T _{opr}	-35 ~ +85	°C	
Storage Temperature Range	T _{stg}	-55 ~ +125	°C	

(*1) When using more than at Ta=25°C, it is reduced 16.3mW per 1°C.

(When RHOM specification board 50mm X 58mm mounting.)

○Recommend Movement Range (Ta = -35~+85°C)

Parameter	Symbol	Range	Unit	Use
VBAT1 Input Voltage	V _{BAT1}	3.15 ~ 4.5	V	Part VREF/BGR
VBAT2 Input Voltage	V _{BAT2}		V	Part LDO
VBATCP Input Voltage	V _{BATCP}		V	Part DCDC
DVDD1 Input Voltage	V _{DVDD1}	1.7 ~ 3.1	V	Part Logic
DVDD2 Input Voltage	V _{DVDD2}	2.5 ~ 3.1	V	Part Logic

It shall be used under the conditions of DVDD1 Input Voltage ≤ DVDD2 Input Voltage.

This product is not especially designed to be protected from radioactivity.

Status of this document

The Japanese version of this document is the formal specification. A customer may use this translation version only for a reference to help reading the formal version. If there are any differences in translation version of this document, formal version takes priority.

Use-related Cautions

The product described in this specification is designed to be used with ordinary electronic equipment or devices (such as audio-visual equipment, office-automation equipment, communications devices, electrical appliances, and electronic toy).

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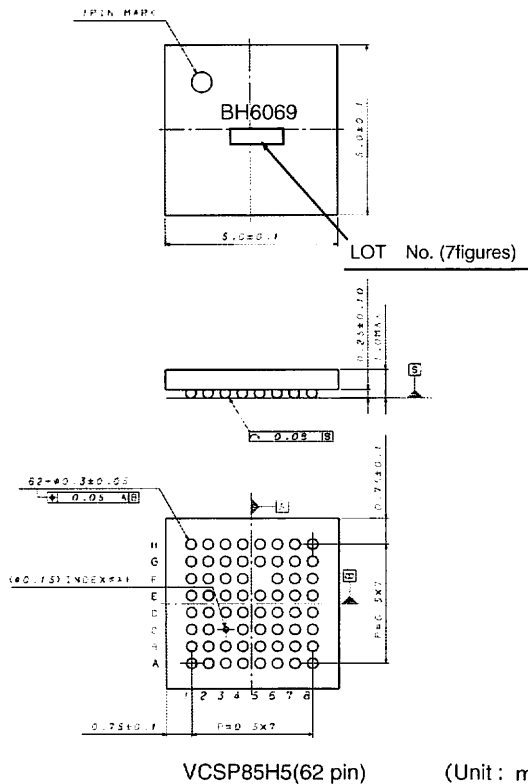
○Electrical Characteristics

Unless otherwise specified, Ta=25°C, VBAT1=VBAT2=VBATCP=3.6V, DVDD1=1.8V, DVDD2=2.6V

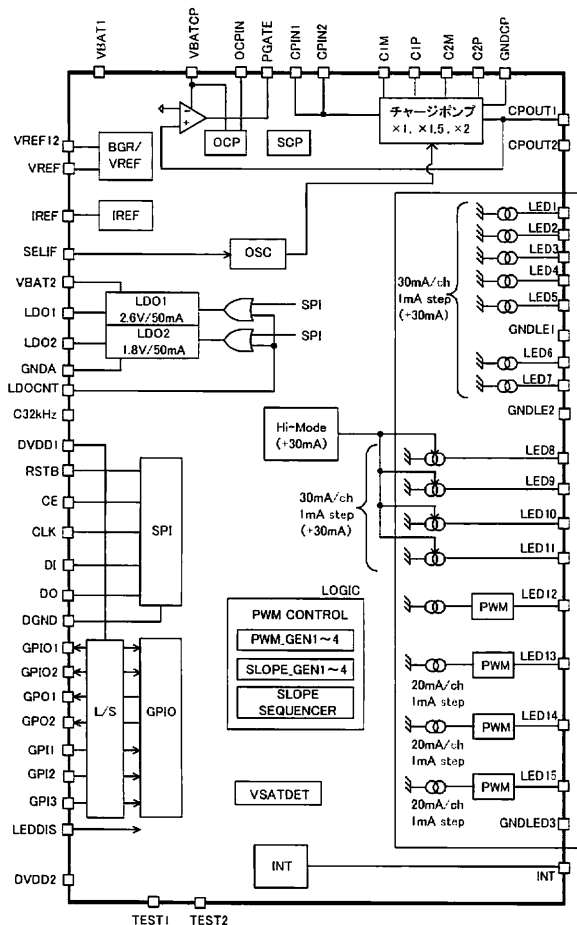
Parameter	Symbol	Spec			Unit	Condition
		MIN	TYP	MAX		
Circuit Current						
Circuit Current1	I _{Q1}	-	0	5	μA	Stand-by mode
Circuit Current2	I _{Q2}	10.8	16.8	27.0	μA	LDOCNT="H", ILOAD=0μA
Circuit Current3	I _{Q3}	5.8	9.0	13.4	mA	DC/DC CONVERTER ON, I _o =0mA, 1.5times mode, fosc=600kHz, LDOCNT="H" ALL LED drivers are active
DC-DC Converter						
Reference Voltage	V _{ref12}	1.199	1.236	1.273	V	*1
IREF Output Voltage	V _{IREF}	0.954	0.984	1.014	V	*1, R _{IREF} =100KΩ
CPOUT Voltage1	V _{CP1}	4.55	4.75	4.95	V	1.5times mode No Load
CPOUT Output Current1	I _{CP1}	-	-	330	mA	1.5times mode VCPOUT>4V, VBAT=3.6V
CPOUT Voltage2	V _{CP2}	4.55	4.75	4.95	V	2.0times mode No Load
CPOUT Output Current2	I _{CP2}	-	-	330	mA	2.0times mode VCPOUT>4V, VBAT=3.15V
Oscillator Frequency1	fosc1	480	600	720	KHz	SELIF=L
Oscillator Frequency2	fosc2	0.96	1.20	1.44	MHz	SELIF=H
Current Driver (Lo-Mode,LED1-15)						
Output Current1	I _{o1}	-5.0%	20.0	+5.0%	mA	I=20mA Setting
Output Current mutching1	Mat1	-5.0%	-	+5.0%	%	I=20mA Setting
Output Current setting range (Lo mode)	I _{Orange}	1	-	31	mA	Lo mode setting
Current step	I _{step}	-	1.0	-	mA	
Current Driver (Hi-Mode,LED8-11)						
Add Output Current a30	I _{o a30}	-5.0%	+30.0	+5.0%	mA	I=30mA~61mA Setting
Add Output Current matching a30	Mat a30	-5.0%	-	+5.0%	%	I=30mA~61mA Setting
Output Current setting range (Hi mode)	I _{Orange}	30	-	61	mA	Hi mode setting
Current step	I _{step}	-	1.0	-	mA	
Current Driver (RGB with PWM : LED12-15)						
PWM on duty1	PWMD1	-5.5	7.81	+5.5	%	PWM12~15SET=5digit
PWM on duty2	PWMD2	-5.0	50.0	+5.0	%	PWM12~15SET=32digit
PWM on duty3	PWMD3	-3.5	90.6	+3.5	%	PWM12~15SET=58digit
LDO1						
Output Voltage	V _{OUT}	2.522	2.600	2.678	V	3.15V≤VBAT≤4.5V 10μA≤I _{OUT} ≤I _{OUTmax}
Output Current	I _{OUT}	-	-	50	mA	3.15V≤VBAT≤4.5V
LDO2						
Output Voltage	V _{OUT}	1.746	1.800	1.854	V	3.15V≤VBAT≤4.5V 10μA≤I _{OUT} ≤I _{OUTmax}
Output Current	I _{OUT}	-	-	50	mA	3.15V≤VBAT≤4.5V
Protector						
UVLO Threshold	V _{UVLO}	2.00	2.25	2.50	V	VBAT falling
SCP Threshold	V _{SCP}	1.0	1.2	1.4	V	CPOUT falling
OCP Threshold 1	I _{OCP1}	150	300	450	mA	Soft Start Mode
OCP Threshold 2	I _{OCP2}	801	841	882	mA	CPIN Input Current
OVP Threshold	V _{ovp}	5.45	5.62	5.79	V	
Detect Voltage	V _{DR}	0.35	0.40	0.45	V	

*1 Design guarantee value.

○Package Diagram



○Block Diagram



○Terminal table

PIN	BALL Name	PIN	BALL Name
A1	TEST1	E1	LDO2
A2	LED4	E2	VBAT2
A3	LED3	E3	GPO1
A4	LED1	E4	GPO2
A5	LED8	E5	CE
A6	LED9	E6	DO
A7	GNDLE2	E7	DVDD1
A8	TEST2	E8	DVDD2
B1	LED6	F1	LDO1
B2	LED5	F2	GPI3
B3	GNDLE1	F3	C32KHZ
B4	LED2	F4	INT
B5	LED15	F6	PGATE
B6	LED14	F7	OCPIN
B7	LED10	F8	VBATCP
B8	LED11	G1	CPIN1
C1	GNDA	G2	LEDDIS
C2	LED7	G3	CPOUT2
C4	IREF	G4	GPIO2
C5	SELIF	G5	GPI2
C6	GNDLE3	G6	GPI1
C7	LED13	G7	GPIO1
C8	LED12	G8	GNDCP
D1	VREF	H2	C2P
D2	VBAT1	H3	CPOUT1
D3	VREF12	H4	C1P
D4	RSTB	H5	C2M
D5	LDOCNT	H6	CPIN2
D6	CLK	H7	C1M
D7	DI		
D8	DGND		

○Use-related Cautions

(1) Absolute maximum ratings

If applied voltage (VDD, VIN), operating temperature range (Topr), or other absolute maximum ratings are exceeded, there is a risk of damage. Since it is not possible to identify short, open, or other damage modes, if special modes in which absolute maximum ratings are exceeded are assumed, consider applying fuses or other physical safety measures.

(2) Recommended operating range

This is the range within which it is possible to obtain roughly the expected characteristics. For electrical characteristics, it is those that are guaranteed under the conditions for each parameter. Even when these are within the recommended operating range, voltage and temperature characteristics are indicated.

(3) Reverse connection of power supply connector

There is a risk of damaging the LSI by reverse connection of the power supply connector. For protection from reverse connection, take measures such as externally placing a diode between the power supply and the power supply pin of the LSI.

(4) Power supply lines

In the design of the board pattern, make power supply and GND line wiring low impedance.

When doing so, although the digital power supply and analog power supply are the same potential, separate the digital power supply pattern and analog power supply pattern to deter digital noise from entering the analog power supply due to the common impedance of the wiring patterns. Similarly take pattern design into account for GND lines as well.

Furthermore, for all power supply pins of the LSI, in conjunction with inserting capacitors between power supply and GND pins, when using electrolytic capacitors, determine constants upon adequately confirming that capacitance loss occurring at low temperatures is not a problem for various characteristics of the capacitors used.

(4) GND voltage

Make the potential of a GND pin such that it will be the lowest potential even if operating below that. In addition, confirm that there are no pins for which the potential becomes less than a GND by actually including transition phenomena.

(6) Shorts between pins and misinstallation

When installing in the set board, pay adequate attention to orientation and placement discrepancies of the LSI. If it is installed erroneously, there is a risk of LSI damage. There also is a risk of damage if it is shorted by a foreign substance getting between pins or between a pin and a power supply or GND.

(7) Operation in strong magnetic fields

Be careful when using the LSI in a strong magnetic field, since it may malfunction.

(8) Inspection in set board

When inspecting the LSI in the set board, since there is a risk of stress to the LSI when capacitors are connected to low impedance LSI pins, be sure to discharge for each process. Moreover, when getting it on and off of a jig in the inspection process, always connect it after turning off the power supply, perform the inspection, and remove it after turning off the power supply. Furthermore, as countermeasures against static electricity, use grounding in the assembly process and take appropriate care in transport and storage.

(9) Input pins

Parasitic elements inevitably are formed on an LSI structure due to potential relationships. Because parasitic elements operate, they give rise to interference with circuit operation and may be the cause of malfunctions as well as damage. Accordingly, take care not to apply a lower voltage than GND to an input pin or use the LSI in other ways such that parasitic elements operate. Moreover, do not apply a voltage to an input pin when the power supply voltage is not being applied to the LSI. Furthermore, when the power supply voltage is being applied, make each input pin a voltage less than the power supply voltage as well as within the guaranteed values of electrical characteristics.

(10) Ground wiring pattern

When there is a small signal GND and a large current GND, it is recommended that you separate the large current GND pattern and small signal GND pattern and provide single point grounding at the reference point of the set so that voltage variation due to resistance components of the pattern wiring and large currents do not cause the small signal GND voltage to change. Take care that the GND wiring pattern of externally attached components also does not change.

(11) Externally attached capacitors

When using ceramic capacitors for externally attached capacitors, determine constants upon taking into account a lowering of the rated capacitance due to DC bias and capacitance change due to factors such as temperature.

(12) Thermal shutdown circuit (TSD)

When junction temperatures become 150°C (typ) or higher, the thermal shutdown circuit operates and turns a switch OFF. The thermal shutdown circuit, which is aimed at isolating the LSI from thermal runaway as much as possible, is not aimed at the protection or guarantee of the LSI. Therefore, do not continuously use the LSI with this circuit operating or use the LSI assuming its operation.

(13) Thermal design

Perform thermal design in which there are adequate margins by taking into account the permissible dissipation (Pd) in actual states of use.

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