

DATA SHEET

74LVC86A

Quad 2-input exclusive OR gate

Product specification
Supercedes data of 1997 Aug 11
IC24 Data Handbook

1998 Apr 28

Quad 2-input exclusive OR gate

74LVC86A

FEATURES

- Wide supply range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- Inputs accept voltages up to 5.5V
- CMOS low power consumption
- Direct interface with TTL levels
- 5-volt tolerant inputs, for interfacing with 5-volt logic

DESCRIPTION

The 74LVC86A is a high-performance, low-power, low-voltage Si-gate CMOS device that is pin and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 V/5 V environment.

The 74LVC86A provides the 2-input EXCLUSIVE-OR function.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25^{\circ}\text{C}$; $t_r = t_f \leq 2.5 \text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL} t_{PLH}	Propagation delay nA, nB to nYn	$C_L = 50 \text{ pF}$; $V_{CC} = 3.3 \text{ V}$	3.0	ns
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per gate	$V_{CC} = 3.3 \text{ V}$, $V_I = \text{GND to } V_{CC}^1$	28	pF

NOTE:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)

$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz; C_L = output load capacity in pF;

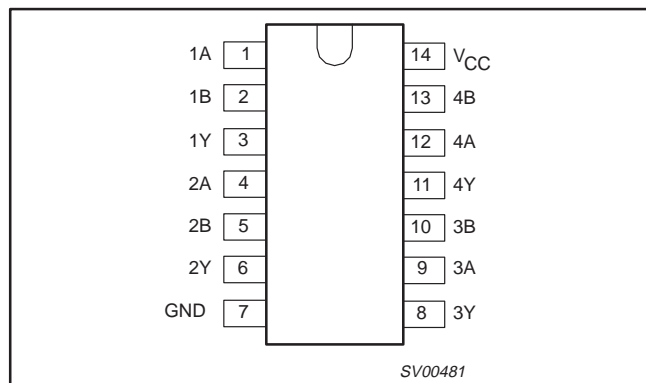
f_o = output frequency in MHz; V_{CC} = supply voltage in V;

$\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

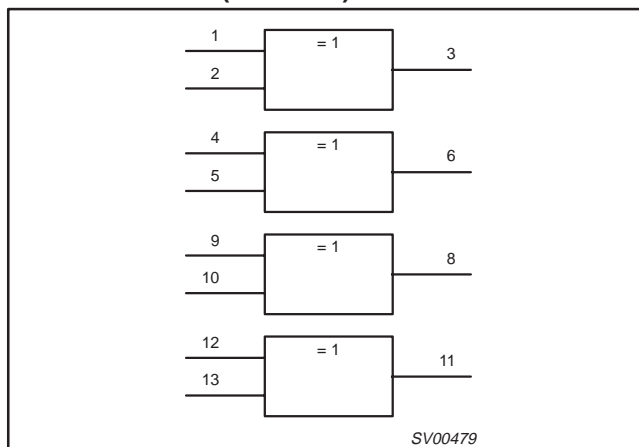
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
14-Pin Plastic DIL	-40°C to $+85^{\circ}\text{C}$	74LVC86A N	74LVC86A N	SOT27-1
14-Pin Plastic SO	-40°C to $+85^{\circ}\text{C}$	74LVC86A D	74LVC86A D	SOT108-1
14-Pin Plastic SSOP Type II	-40°C to $+85^{\circ}\text{C}$	74LVC86A DB	74LVC86A DB	SOT337-1
14-Pin Plastic TSSOP Type I	-40°C to $+85^{\circ}\text{C}$	74LVC86A PW	74LVC86APW DH	SOT402-1

PIN CONFIGURATION



LOGIC SYMBOL (IEEE/IEC)



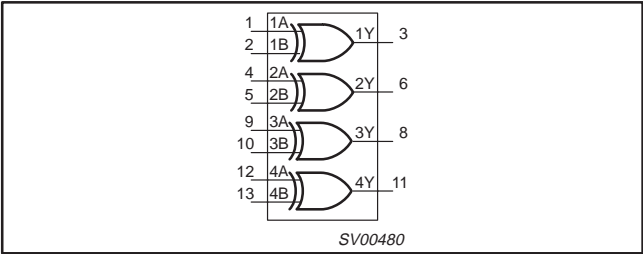
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 4, 9, 12	1A – 4A	Data inputs
2, 5, 10, 13	1B – 4B	
3, 6, 8, 11	1Y – 4Y	Data outputs
7	GND	Ground (0 V)
14	V_{CC}	Positive supply voltage

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LOGIC SYMBOL

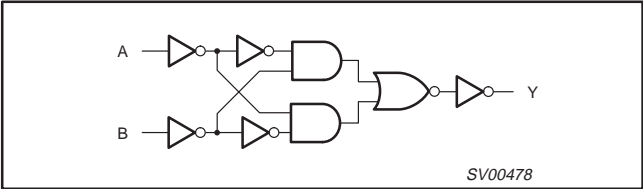


FUNCTION TABLE

INPUTS		OUTPUTS
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	L

NOTES:
H = HIGH voltage level
L = LOW voltage level

LOGIC DIAGRAM (ONE GATE)



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V _{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V _I	DC Input voltage range		0	5.5	V
V _O	DC output voltage range		0	V _{CC}	V
T _{amb}	Operating ambient temperature range in free-air		−40	+85	°C
t _r , t _f	Input rise and fall times	V _{CC} = 1.2 to 2.7V	0	20	ns/V
		V _{CC} = 2.7 to 3.6V	0	10	

ABSOLUTE MAXIMUM RATINGS¹

Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage (for max. speed performance)		−0.5 to +6.5	V
I _{IK}	DC input diode current	V _I < 0	−50	mA
V _I	DC input voltage	Note 2	−0.5 to +5.5	V
I _{OK}	DC output diode current	V _O > V _{CC} or V _O < 0	± 50	mA
V _O	DC output voltage	Note 2	−0.5 to V _{CC} + 0.5	V
I _O	DC output source or sink current	V _O = 0 to V _{CC}	± 50	mA
I _{GND} , I _{CC}	DC V _{CC} or GND current		± 100	mA
T _{stg}	Storage temperature range		−65 to +150	°C
P _{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	500 500	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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DC CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP ¹	MAX	
V _{IH}	HIGH level Input voltage	V _{CC} = 1.2V	V _{CC}			V
		V _{CC} = 2.7 to 3.6V	2.0			
V _{IL}	LOW level Input voltage	V _{CC} = 1.2V			GND	V
		V _{CC} = 2.7 to 3.6V			0.8	
V _{OH}	HIGH level output voltage	V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; I _O = -12mA	V _{CC} - 0.5			V
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = -100μA	V _{CC} - 0.2	V _{CC}		
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = -18mA	V _{CC} - 0.6			
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = -24mA	V _{CC} - 0.8			
V _{OL}	LOW level output voltage	V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; I _O = 12mA			0.40	V
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = 100μA			0.20	
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = 24mA			0.55	
I _I	Input leakage current	V _{CC} = 3.6V; V _I = 5.5V or GND		± 0.1	± 5	μA
I _{CC}	Quiescent supply current	V _{CC} = 3.6V; V _I = V _{CC} or GND; I _O = 0		0.1	10	μA
ΔI _{CC}	Additional quiescent supply current per input pin	V _{CC} = 2.7V to 3.6V; V _I = V _{CC} - 0.6V; I _O = 0		5	500	μA

NOTES:

1. All typical values are at $V_{CC} = 3.3V$ and $T_{amb} = 25^\circ C$.

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF; $R_L = 500\Omega$; $T_{amb} = -40^\circ C$ to $+85^\circ C$

SYMBOL	PARAMETER	WAVEFORM	LIMITS							UNIT
			$V_{CC} = 3.3V \pm 0.3V$			$V_{CC} = 2.7V$			$V_{CC} = 1.2V$	
			MIN	TYP ¹	MAX	MIN	TYP ¹	MAX	TYP	
t_{PHL}/t_{PLH}	Propagation delay nA, nB to nY	Figures 1, 2	1.5	3.0	5	1.5	3.4	5.8	11	ns

NOTE:

1. These typical values are at $V_{CC} = 3.3V$ and $T_{amb} = 25^\circ C$.

AC WAVEFORMS

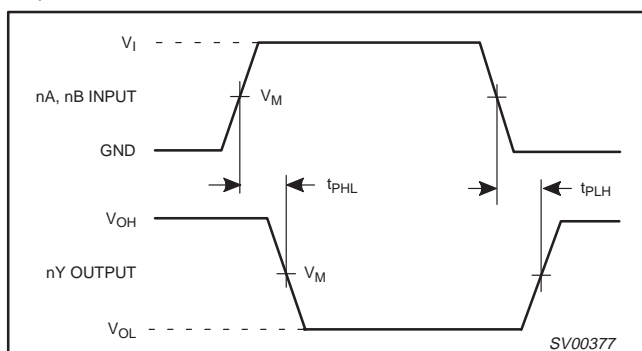
 $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V $V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

Figure 1. Input (nA, nB) to output (nY) propagation delays

TEST CIRCUIT

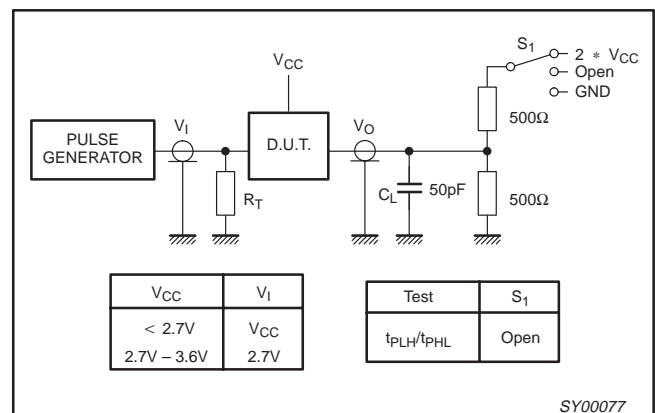


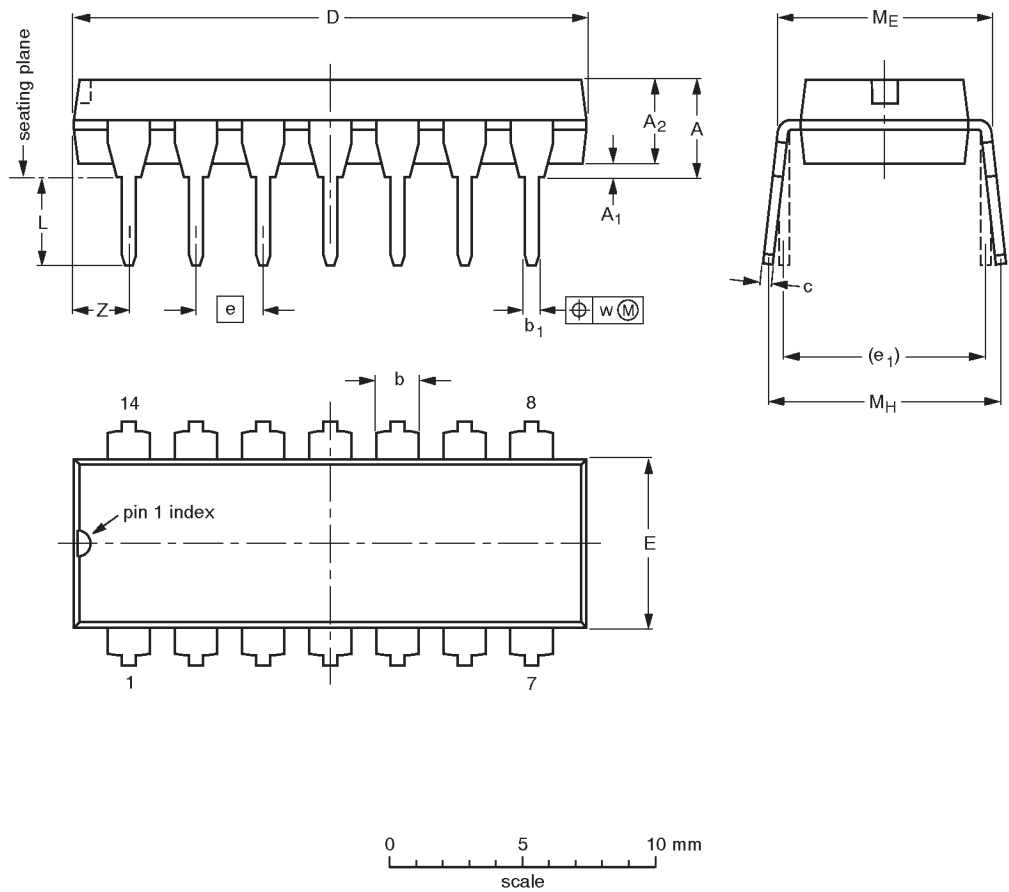
Figure 2. Load circuitry for switching times.

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DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1




DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.020	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

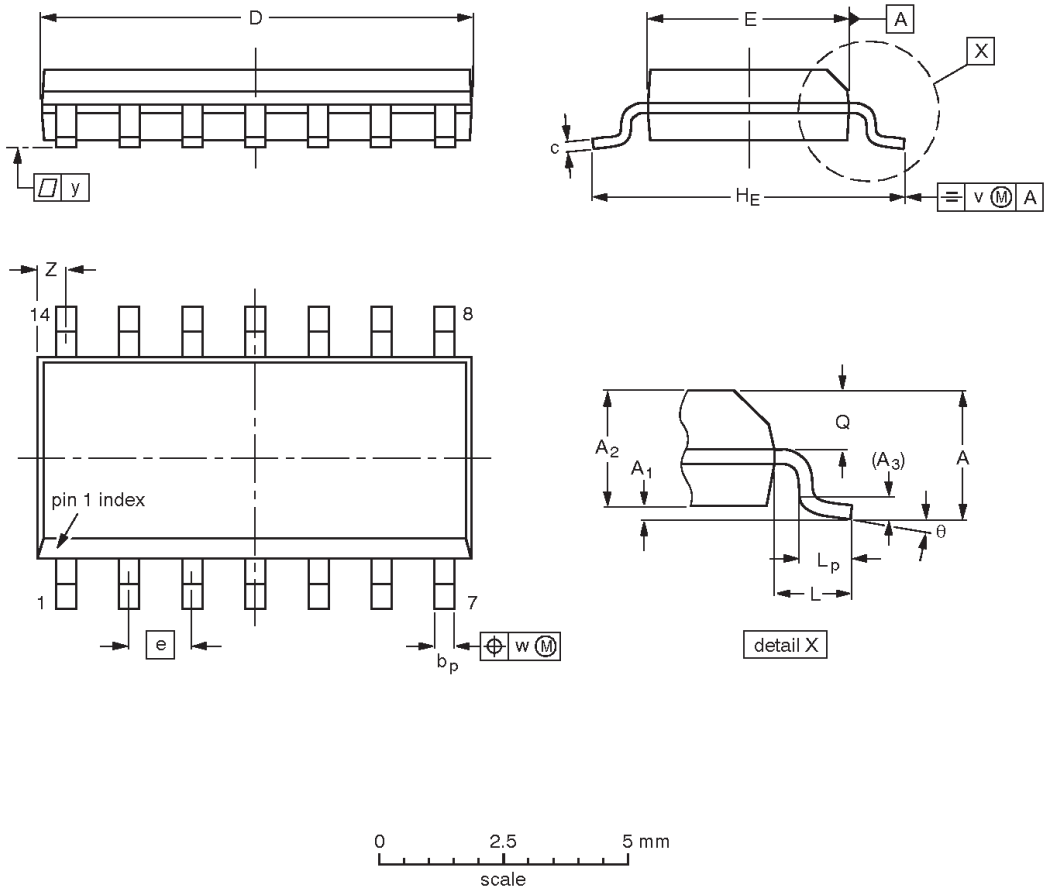
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT27-1	050G04	MO-001AA				92-11-17 95-03-11

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SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

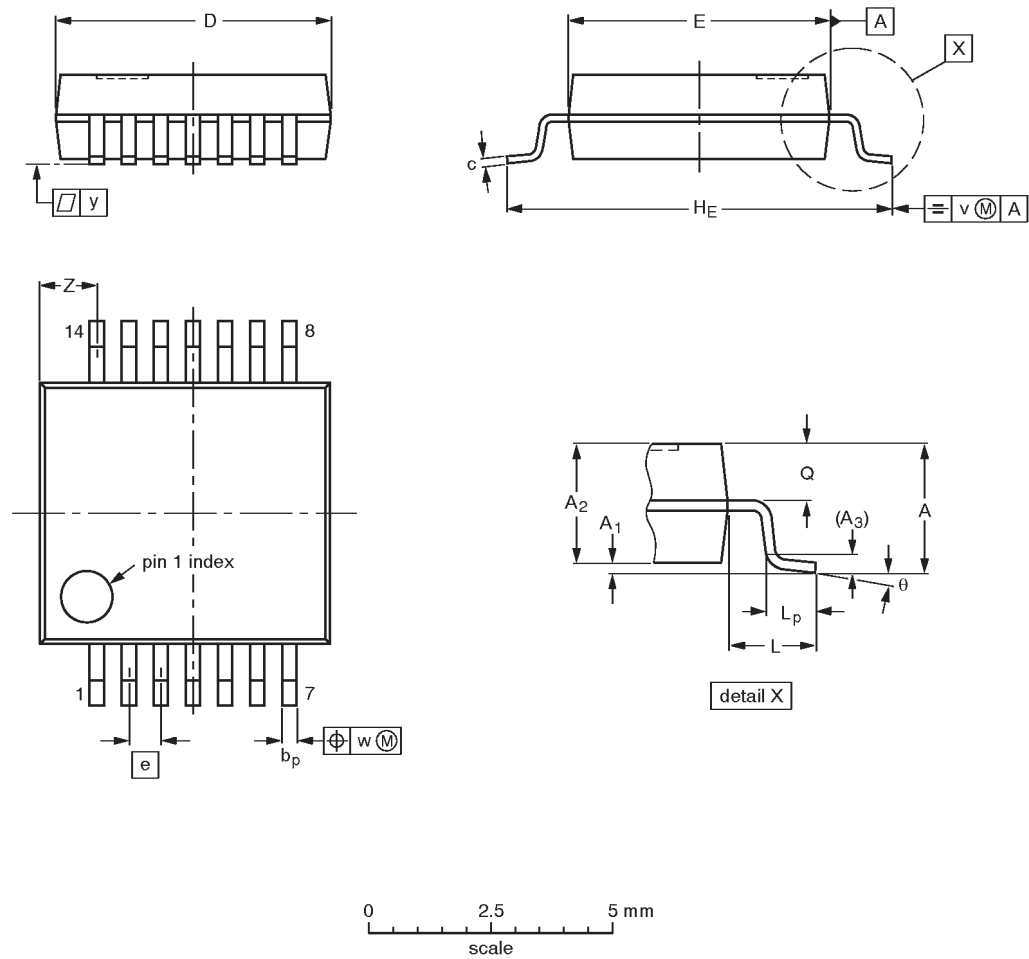
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06S	MS-012AB				95-01-23 97-05-22

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SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

Note
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

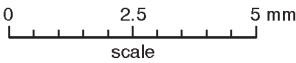
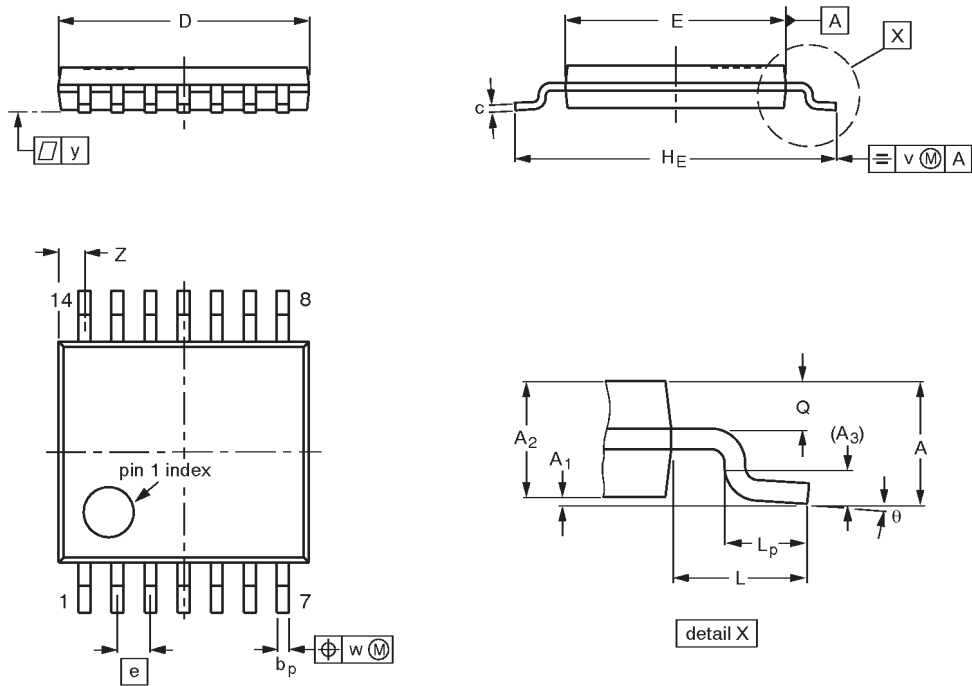
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT337-1		MO-150AB				95-02-04 96-01-18

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TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT402-1		MO-153				94-07-12 95-04-04

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NOTES

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DEFINITIONS		
Data Sheet Identification	Product Status	Definition
<i>Objective Specification</i>	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
<i>Preliminary Specification</i>	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
<i>Product Specification</i>	Full Production	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

LIFE SUPPORT APPLICATIONS

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