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National Semiconductor

CLC406
Wideband, Low Power Monolithic Op Amp

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General Description

The CLC406 is a wideband monolithic operational amplifier designed for low-gain applications where power and cost are of primary concern. Operating from ±5V supplies, the CLC406 consumes only 50mW of power yet maintains a 160MHz small signal bandwidth and a 1500V/μs slew rate. Benefitting from National's current feedback architecture, the CLC406 offers a gain range of ±1 to ±10 while providing stable, oscillation free operation without external compensation, even at unity gain.

With its exceptional differential gain and phase, typically 0.02% and 0.02° at 3.58MHz, the CLC406 is designed to meet the performance and cost requirements of high volume composite video applications. The CLC406's large signal bandwidth, high slew rate and high drive capability are features well suited for RGB video applications.

Providing a 12ns settling time to 0.05% (1/2 LSB in 10-bit systems) and −68/−75dBc 2nd/3rd harmonic distortion ($2V_{pp}$ at 10MHz, $R_L = 1k\Omega$), the CLC406 is an excellent choice as a buffer or driver for high speed A/D and D/A converter systems.

Commercial remote sensing applications and battery powered radio transceivers requiring a high performance, low power amplifier will find the CLC406 to be an attractive, cost-effective solution.

Constructed using an advanced, complementary bipolar process and National's proven current feedback architectures, the CLC406 is available in several versions to meet a variety of requirements.

CLC406AJP	-40°C to +85°C	8-pin plastic DIP
CLC406AJE	-40°C to +85°C	8-pin plastic SOIC
CLC406AJM5	-40°C to +85°C	5-pin SOT

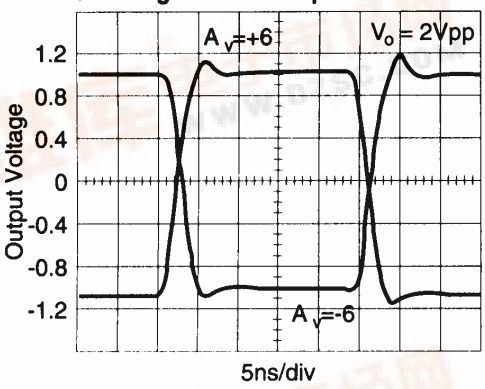
Features

- 160MHz small signal bandwidth
- 50mW power (±5Vsupplies)
- 0.02%/0.02° differential gain/phase
- 12ns settling to 0.05%
- 1500V/μs slew rate
- 2.2ns rise and fall time ($2V_{pp}$)
- 70mA output current

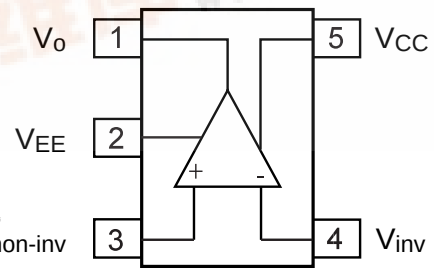
Applications

- Video distribution amp
- HDTV amplifier
- Flash A/D driver
- D/A transimpedance buffer
- Pulse amplifier
- Photodiode amp
- LAN amplifier

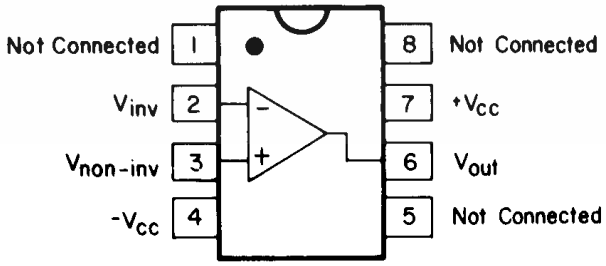
Small Signal Pulse Response



Pinout
SOT23-5



Pinout
DIP & SOIC



CLC406 Electrical Characteristics (A_V = +6, V_{cc} = ±5V, R_L = 100Ω, R_f = 500Ω; unless specified)

PARAMETERS	CONDITIONS	TYP	MAX & MIN RATINGS			UNITS	SYMBOL
Ambient Temperature	CLC406AJ	+25°C	−40°C	+25°C	+ 85°C		
FREQUENCY DOMAIN PERFORMANCE							
− 3db bandwidth	V_{out}<2V_{pp}	160	>110	>110	>90	MHz	SSBW
	V_{out}<5V_{pp}	130	>95	>95	>80	MHz	LSBW
gain flatness	V_{out}<2V_{pp}						
peaking	DC to 25MHz	0	<0.2	<0.2	<0.2	dB	GFPL
peaking	>25MHz	0	<0.5	<0.5	<0.5	dB	GFPH
rolloff	DC to 50MHz	0	<0.6	<0.6	<1.0	dB	GFR
linear phase deviation	DC to 75MHz	0.2	<0.8	<0.8	<1.2	°	LPD
differential gain	(A_V = +2) 150Ω load, 3.58MHz	0.02	<0.04	<0.04	<0.04	%	DG1
	4.43MHz	0.02	<0.04	<0.04	<0.04	%	DG2
differential phase	(A_V = +2) 150Ω load, 3.58MHz	0.02	<0.04	<0.04	<0.08	°	DP1
	4.43MHz	0.025	<0.05	<0.05	<0.10	°	DP2
TIME DOMAIN RESPONSE							
rise and fall time	2V step	2.2	<3.0	<3.0	<3.9	ns	TRS
	4V step	3.0	<3.6	<3.6	<5.0	ns	TRL
settling time to 0.05%	2Vstep	12	<18	<18	<20	ns	TS
overshoot	2V step	8	<15	<15	<15	%	OS
slew rate		1500	>1200	>1200	>1000	V/μs	SR
DISTORTION AND NOISE RESPONSE							
2nd harmonic distortion	2V_{pp},20MHz,R_L = 100Ω	−46	<−42	<−42	<−38	dBc	HD2
	2V_{pp},10MHz,R_L = 1kΩ	−68	<−62	<−62	<−60	dBc	HD2L
3rd harmonic distortion	2V_{pp},20MHz,R_L = 100Ω	−50	<−46	<−46	<−42	dBc	HD3
	2V_{pp},10MHz,R_L = 1kΩ	−75	<−70	<−70	<−65	dBc	HD3L
equivalent input noise							
non-inverting voltage	>1MHz	2.7	3.4	3.4	3.8	nV/√Hz	VN
inverting current	>1MHz	11.0	13.9	13.9	15.5	pA/√Hz	ICN
non-inverting current	>1MHz	2.1	2.6	2.6	3.0	pA/√Hz	NCN
total noise floor	>1MHz	−157	<−156	<−156	−155	dBm_{1Hz}	SNF
total integrated noise	1MHz to 100MHz	31	<38	<38	<42	μV	INV
STATIC, DC PERFORMANCE							
*input offset voltage		2	<10	<6	<12	mV	VIO
average temperature coefficient		30	<60	—	<60	μV/°C	DVIO
*input bias current	non-inverting	5	<24	<12	<12	μA	IBN
average temperature coefficient		30	<125	—	<50	nA/°C	DIBN
*input bias current	inverting	3	<23	<15	<20	μA	IBI
average temperature coefficient		20	<100	—	<50	nA/°C	DIBI
power supply rejection ratio		50	>46	>46	>44	dB	PSRR
common mode rejection ratio		50	>45	>45	>43	dB	CMRR
*supply current	no load	5.0	<7.0	<6.7	<6.7	mA	ICC
MISCELLANEOUS PERFORMANCE							
non-inverting input resistance		1000	>300	>500	>500	kΩ	RIN
non-inverting input capacitance		1.0	<2.0	<2.0	<2.0	pF	CIN
output impedance	DC	0.2	<0.6	<0.3	<0.2	Ω	RO
output voltage range	R_L = 100Ω	+3.1, −2.7	+1.6, −2.5	± 2.7	±2.7	V	VO
common mode input range		± 2.2	± 1.4	± 2.0	± 2.0	V	CMIR
output current		70	30	50	50	mA	IO

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Absolute Maximum Ratings

V_{cc}	±7V
I_{out} output is short circuit protected to ground, but maximum reliability will be maintained if I_{out} does not exceed...	70mA
common mode input voltage	±V_{cc}
differential input voltage	10V
junction temperature	+ 150°C
operating temperature range	
AJ:	− 40°C to + 85°C
storage temperature range	− 65°C to + 150°C
Lead solder duration (+ 300°C)	10 sec
EDS rating (human body model)	2000V

Reliability Information

Transistor count	34

Miscellaneous Ratings

recommended gain range: ±1 to ±10

NOTES:

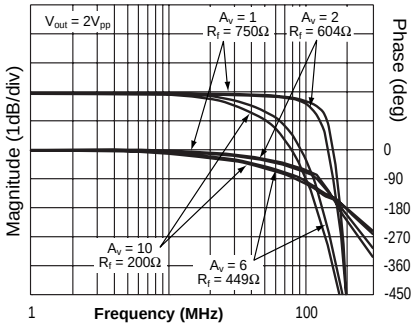
* AJ 100% tested at + 25°C.

Package Thermal Resistance

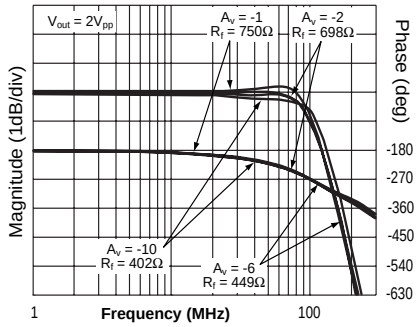
Package	θ_{JC}	θ_{JA}
AJP	70°C/W	125°C/W
AJE	65°C/W	145°C/W
AJM5	130°C/W	150°C/W

CLC406 Typical Performance Characteristics (T_A = 25°, A_V = +6, V_{CC} = ±5V, R_L = 100Ω, R_f = 500Ω)

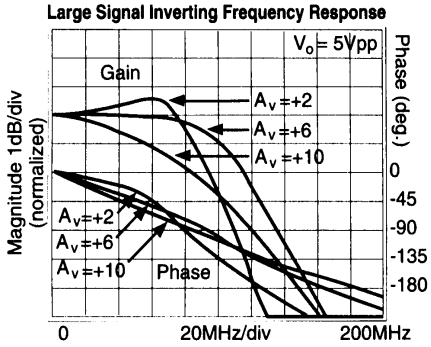
Non-Inverting Frequency Response



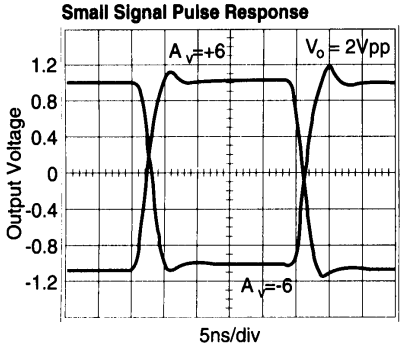
Inverting Frequency Response



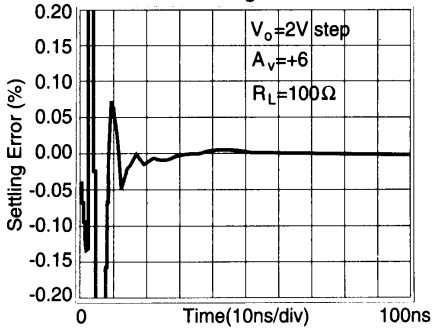
Large Signal Inverting Frequency Response



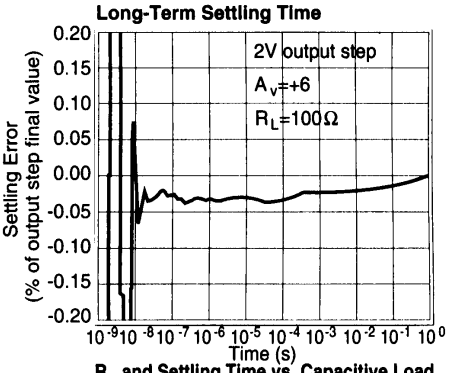
Small Signal Pulse Response



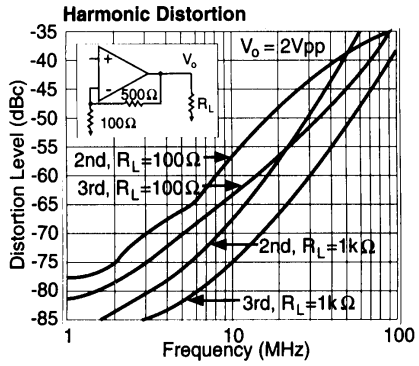
Short-Term Settling Time



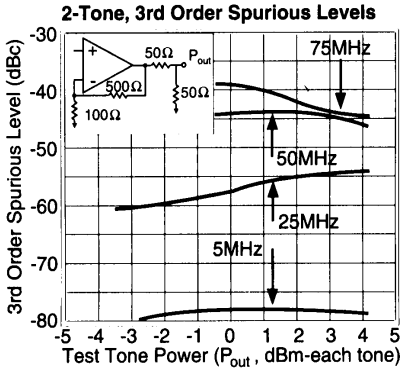
Long-Term Settling Time



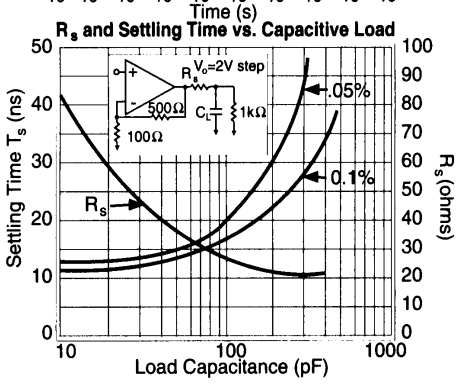
Harmonic Distortion



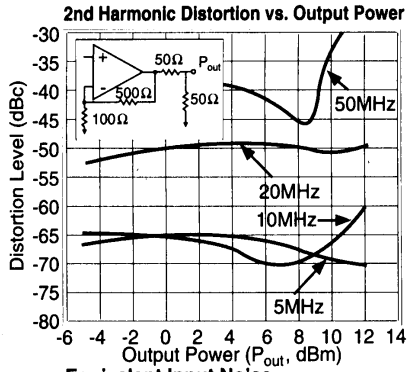
2-Tone, 3rd Order Spurious Levels



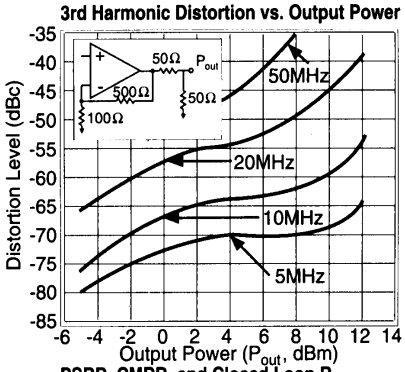
Rs and Settling Time vs. Capacitive Load



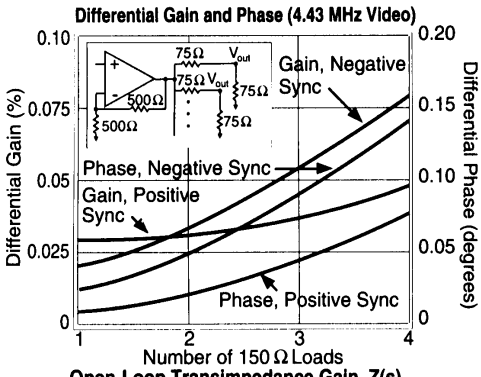
2nd Harmonic Distortion vs. Output Power



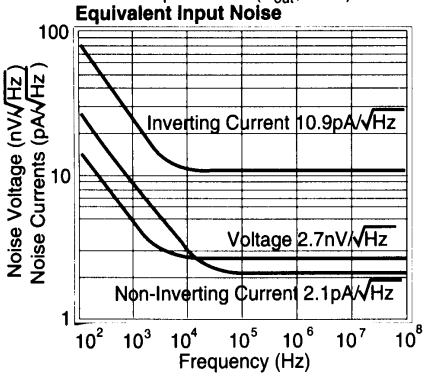
3rd Harmonic Distortion vs. Output Power



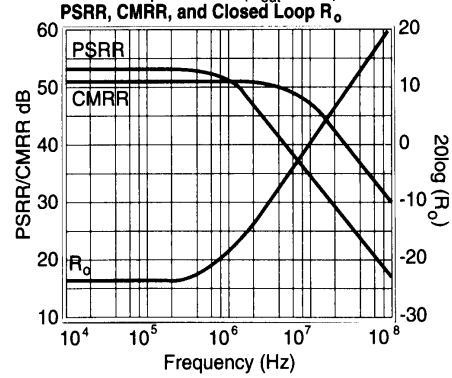
Differential Gain and Phase (4.43 MHz Video)



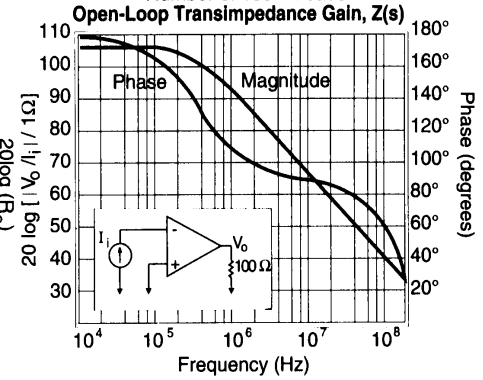
Equivalent Input Noise



PSRR, CMRR, and Closed Loop R_o



Open-Loop Transimpedance Gain, Z(s)



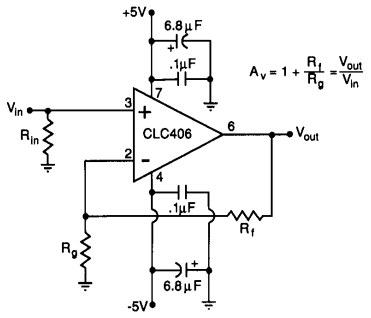
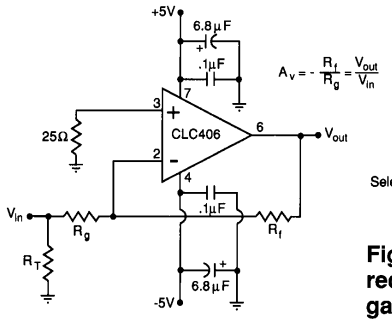


Figure 1: recommended non-inverting gain circuit



Select R_T to yield desired $R_{in} = R_T || R_g$

Figure 2: recommended inverting gain circuit

Feedback Resistor

The CLC406 achieves its exceptional AC performance while requiring very low quiescent power by using the current feedback topology and an internal slew rate enhancement circuit. The loop gain and frequency response for a current feedback op amp is predominantly set by the feedback resistor value. The CLC406 is optimized for a gain of +6 to use a 500Ω feedback resistor **(for maximally flat response at a gain of +2, use $R_f = 1k\Omega$).** Using lower values can lead to excessive ringing in the pulse response while a higher value will limit the bandwidth. Application Note OA-13 provides a more detailed discussion of choosing a feedback resistor. A plot found within the CLC415 data sheet entitled "Recommended R_f vs. Gain" is also applicable to the CLC406. The values of R_f found on this plot will optimize the performance of the CLC406 over its ±1 to ±10 gain range. The CLC406, like all current feedback op amps, can be operated at higher than recommended gains with an expected reduction in bandwidth.

Slew Rate and Harmonic Distortion

The current feedback topology yields an inherently high slew rate amplifier. For this reason the CLC406 shows little difference in bandwidth between $2V_{pp}$ and $5V_{pp}$ outputs. The dominant slew rate limiting mechanism is the unity gain buffer used internally from the non-inverting to the inverting inputs. Using a slew enhancement circuit to sense the onset of slew limiting, the buffer stage momentarily increases the quiescent current to handle high slew requirements. Slew rates will decrease when operating the CLC406 at lower non-inverting gains due to the increasing signal swing through the buffer stage which is necessary to maintain a fixed desired output swing. Conversely, slew rates are generally higher and relatively insensitive to gain setting for inverting gain operation. An additional discussion of slew rates can be found in the CLC404 data sheet.

As the output signal swing is increased, the slew enhancement circuit found in the buffer stage acts to suppress harmonic distortions. This is one reason the CLC406 does not exhibit a simple relationship between output power and distortion. For example, the 2-tone, 3rd order spurious plot shows the spurious level to remain nearly constant over test tone power. For this reason the CLC406 does not exhibit an intercept type performance where the relative spurious levels change at twice the rate of the test tone power.

Differential Gain and Phase

Differential gain and phase performance specifications are common to composite video distribution applications. These specifications refer to the change in small signal gain and phase of the color subcarrier frequency (4.43MHz for PAL composite video) as the amplifier output is swept over a range of DC voltages. For this test only, the CLC406 is specified at a gain of +2 while connected to one or more doubly terminated 75Ω loads. Application Note OA-08 provides an additional discussion of differential gain and phase measurements.

Non-inverting Source Impedance

For best operation, the DC source impedance looking out of the non-inverting input should be less than 3kΩ but greater than 20Ω. Parasitic self oscillations may occur in the input transistors if the DC source impedance is out of this range. This impedance also acts as the gain for the non-inverting input bias and noise currents and therefore can become troublesome for high values of DC source impedance. The inverting configuration of Figure 2 shows a 25Ω resistor to ground on the non-inverting input which insures stability but does not provide bias current cancellation. The input bias currents are unrelated for a current feedback amplifier which eliminates the need for source impedance matching to achieve bias current cancellation.

DC Accuracy and Noise

Figure 3 shows an example of the output offset voltage computation. The calculation is developed using typical bias current and offset voltage specifications at 25°C, a gain (Av) of +6 and a non-inverting source impedance (R_s) of 25Ω.

Figure 3: Output Offset Voltage Calculation

Output Offset Voltage $V_o = (\pm I_{bn}R_{in} \pm V_{io})(1 + R_f/R_g) \pm I_{bi}R_f$

$V_o = (\pm 5\mu A(25\Omega) \pm 2mV)(6) \pm 3\mu A(500\Omega) = \pm 14.25mV$

Improved output offset voltage is possible using the composite circuits shown in Application Note OA-07.

The total output spot noise is computed in a similar fashion to the output offset voltage. Using the input spot noise voltage and the two input spot noise currents, the total output spot noise is developed through the same gain equations for each term but combined as the square root of the sum of squared contributing elements. Application Note OA-12 provides a more detailed discussion of noise calculations for current feedback amplifiers.

Printed Circuit Layout

As with any high speed component, a careful attention to the board layout is necessary for optimum performance. Of particular importance is the careful control of parasitic capacitances on the output pin. As the output impedance plot shows, the closed loop output for the CLC406 eventually becomes inductive as the loop gain rolls off with increasing frequency. Direct capacitive loading on the output pin can quickly lead to peaking in the frequency response, overshoot in the pulse response, ringing or even sustained oscillations. The "Suggested Series R_s vs. C" plot should be used as a starting point when a capacitive load must be driven.

Evaluation boards (CLC730013 – DIP, CLC730027 – SOIC, and CLC730068 – SOT) for the CLC406 are available. Further layout suggestions can be found in Application Note OA-15.

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