FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-13513-1E

Linear IC Converter

CMOS

D/A Converter for Digital Tuning

(12-channel, 8-bit, on-chip OP amp., low-voltage)

MB88146A

■ DESCRIPTION

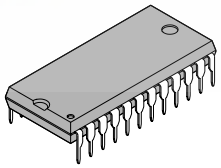
The MB88146A is an 8-bit D/A converter with twelve built-in channels. The 12 analog outputs each have a built-in OP amplifier with large current drive-capability.
The data input/output format is CS (chip select) with serial bus connection available.
A built-in 12-bit I/O expander enables serial ↔ parallel conversion (8 of the 12 bits can also be used for analog output).
This product can be used for microcontroller port expansion, electronic level adjustment, replacement of semi-fixed resistance for tuning, etc.

■ FEATURES

- Ultra low power consumption (1.2 mW/chl: typical)
- Ultra compact package
- Built-in 12-channel R-2R type 8-bit D/A converter
- Built-in 12-bit I/O expander (8 bits also function as analog output)
- Built-in analog output amplifier (sink current 1.0 mA maximum, source current 1.0 mA maximum)
- Built-in power-on detection circuit (initialized at detection of VccD power-on)
- MCU interface compatible with 3 V to 5 V systems
- Power divided into MCU interface power supply (VccD) and OP amplifier power supply (VccA), D/A converter power supply (VccD)
- Analog output capability from 0 V to VccA
- Serial data I/O operates to maximum of 2.5 MHz (in cascade connection, up to 2.5 MHz when VccD = 5 V, up to 1.5 MHz when VccD = 3 V)
- CMOS process
- Choice of two packages: SDIP-24 pin and SSOP-24 pin.

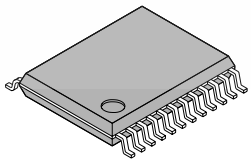
■ PACKAGES

24-pin Plastic DIP



(DIP-24P-M02)

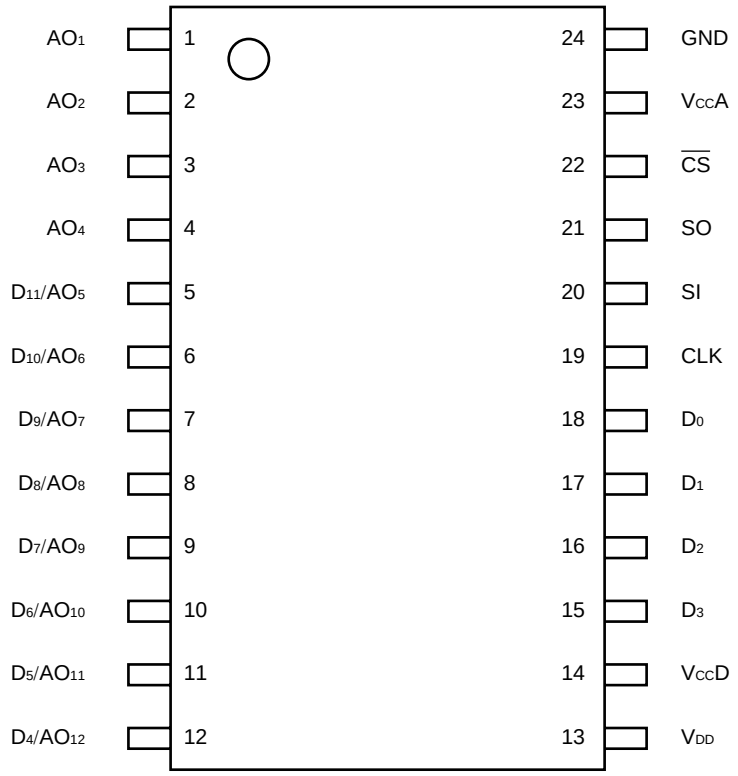
24-pin Plastic SSOP



(FPT-24P-M03)

■ PIN ASSIGNMENT

(TOP VIEW)



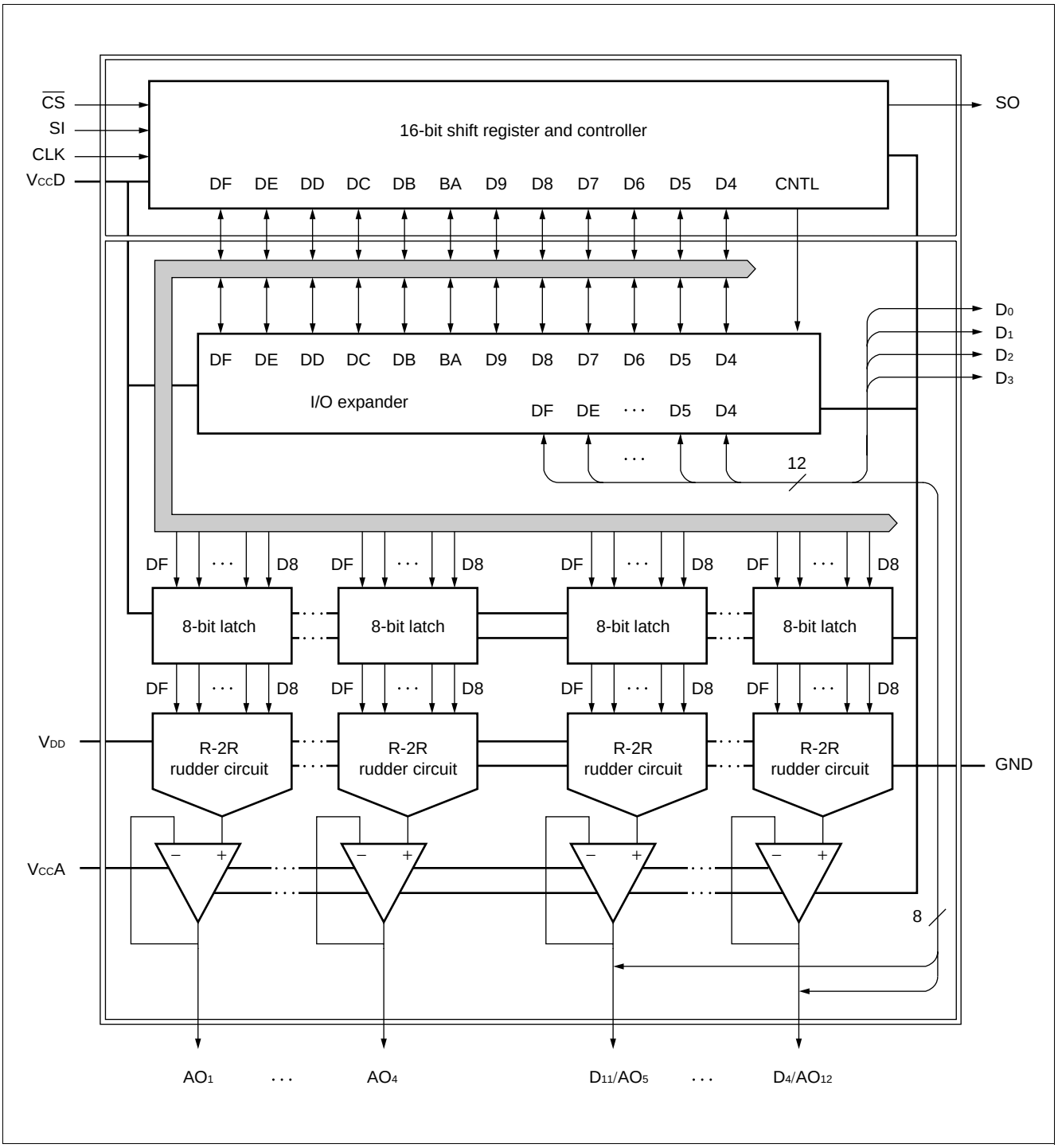
DIP-24, SSOP-24

■ PIN DESCRIPTION

Pin no.	Pin name	Description
1 to 4	AO_1 to AO_4	D/A converter analog output pins (V_{DD} to GND output). (Default: output #00 setting level)
5 to 12	D_{11}/AO_5 to D_4/AO_{12}	These pins may be used either as I/O expander parallel input/output ($V_{CC}A$/GND output 0.5 $V_{CC}A$/0.2 $V_{CC}A$ input) or D/A converter analog output (V_{DD} to GND output). Pin status is controlled by input data. See "■Data Configuration". (Default: Input mode, Hi-Z state)
13	V_{DD}*1	D/A converter reference power pin.
14	$V_{CC}D$*1	MCU interface power supply pin (power supply for I/O expander).
15 to 18	D_3 to D_0	I/O expander parallel input/output pins. ($V_{CC}D$/GND output: When $V_{CC}D \geqq 4.0$ V, 0.5 $V_{CC}D$/0.2 $V_{CC}D$ input, When $V_{CC}D < 4.0$ V, 2 V/0.2 $V_{CC}D$ input) Pin status is controlled by input data. See "■Data Configuration." (Default: Input mode, Hi-Z state)
19	CLK*2	Shift clock signal input pin. When $\overline{CS}$ = "L," SI data is loaded into the shift register at the rising edge of the shift clock.
20	SI*2	Data input pin (serial input pin). Used for 16-bit serial data input.
21	SO	Data output pin (serial output pin). The first bit (LSB) data of the 16-bit shift register is output simultaneously with the falling edge of the shift clock. When $\overline{CS}$ output = "H," this pin goes to high impedance state.
22	$\overline{CS}$*2	Chip select signal input pin. Input to shift registers is enabled when the $\overline{CS}$ signal falling edges. Shift register contents can be executed when the $\overline{CS}$ signal rising edges.
23	$V_{CC}A$*1	Analog unit power supply pin (OP amplifier power supply).
24	GND	Common GND pin.

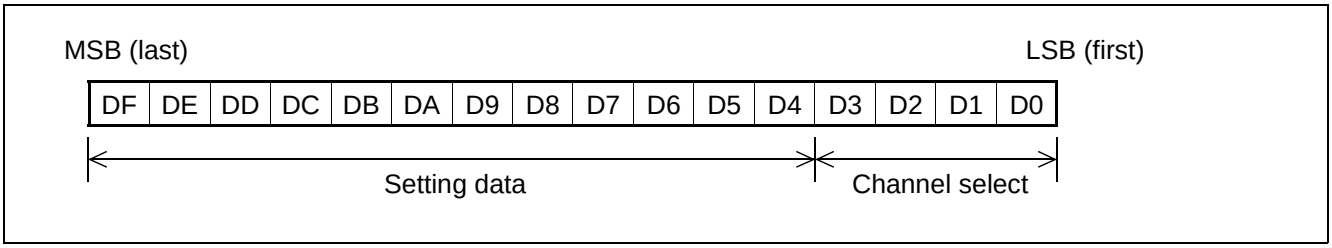
*1: Be sure that $V_{CC}A \geqq V_{CC}D$, and that $V_{CC}A \geqq V_{DD}$.
*2: Do not leave this pin in floating state.

■ BLOCK DIAGRAM



■ DATA CONFIGURATION

1. Data Configuration



2. Channel Select

D3	D2	D1	D0	Function
0	0	0	0	Don't Care/special function
0	0	0	1	AO_1 selected
0	0	1	0	AO_2 selected
to	to	to	to	to
1	0	1	1	AO_{11} selected
1	1	0	0	AO_{12} selected
1	1	0	1	I/O expander (serial → parallel)
1	1	1	0	I/O expander (parallel → serial)
1	1	1	1	Expander status register (ESR)

3. Setting Data

- Don't Care/special function (Channel select = "0000")

DF	DE	DD	DC	DB	DA	D9	D8	D7	D6	D5	D4	Analog output voltage level
×	×	×	×	×	×	×	×	0	0	0	0	Don't Care
to	to	to	to	to	to	to	to	to	to	to	to	Don't Care
×	×	×	×	×	×	×	×	1	0	1	1	Don't Care
0	0	0	0	0	0	0	0	1	1	0	0	GND (all channels)
0	0	0	0	0	0	0	1	1	1	0	0	$V_{DD}/256 \times 1$ (all channels)
0	0	0	0	0	0	1	0	1	1	0	0	$V_{DD}/256 \times 2$ (all channels)
to	to	to	to	to	to	to	to	to	to	to	to	to
1	1	1	1	1	1	1	0	1	1	0	0	$V_{DD}/256 \times 254$ (all channels)
1	1	1	1	1	1	1	1	1	1	0	0	$V_{DD}/256 \times 255$ (all channels)
×	×	×	×	×	×	×	×	1	1	0	1	Hi-Z (I/O expander state)*
×	×	×	×	×	×	×	×	1	1	1	0	Reset (state when power is ON)
×	×	×	×	×	×	×	×	1	1	1	1	Don't Care

×: Don't care *: Hi-Z output on all channels of AO_5 through AO_{12}

- D/A Converter (Channel select = "0001" to "1100")

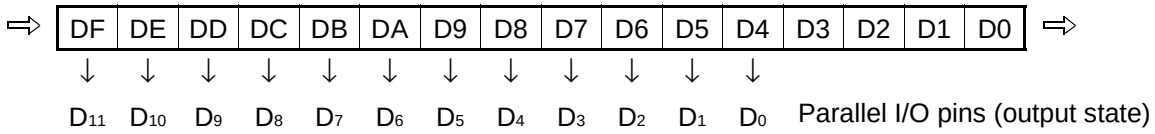
DF	DE	DD	DC	DB	DA	D9	D8	D7	D6	D5	D4	Analog output voltage level
0	0	0	0	0	0	0	0	0	0	0	0	GND
0	0	0	0	0	0	0	1	0	0	0	0	$V_{DD}/256 \times 1$
0	0	0	0	0	0	1	0	0	0	0	0	$V_{DD}/256 \times 2$
0	0	0	0	0	0	1	1	0	0	0	0	$V_{DD}/256 \times 3$
to	to	to	to	to	to	to	to	to	to	to	to	to
1	1	1	1	1	1	0	1	0	0	0	0	$V_{DD}/256 \times 253$
1	1	1	1	1	1	1	0	0	0	0	0	$V_{DD}/256 \times 254$
1	1	1	1	1	1	1	1	0	0	0	0	$V_{DD}/256 \times 255$
×	×	×	×	×	×	×	×	0	0	0	1	Hi-Z (I/O expander state)*
×	×	×	×	×	×	×	×	0	0	1	0	Don't Care
to	to	to	to	to	to	to	to	to	to	to	to	Don't Care
×	×	×	×	×	×	×	×	1	1	1	1	Don't Care

×: Don't care *: Only AO_5 through AO_{12} output is valid

- I/O Expander [Channel select = “1101”]: Serial → Parallel Conversion

  Performs parallel conversion of data bits D4 to DF for output on pins D_0 to D_{11}.
  Note that only those pins designated for output in the ESR (expander status register) are output.

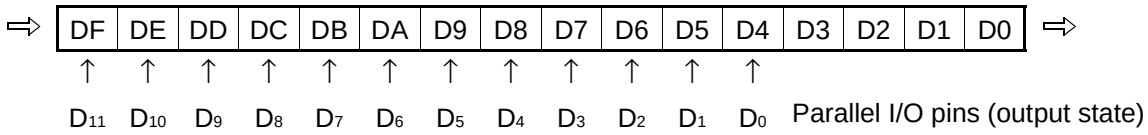
  Shift register



- I/O Expander [Channel select = “1110”]: Parallel → Serial Conversion

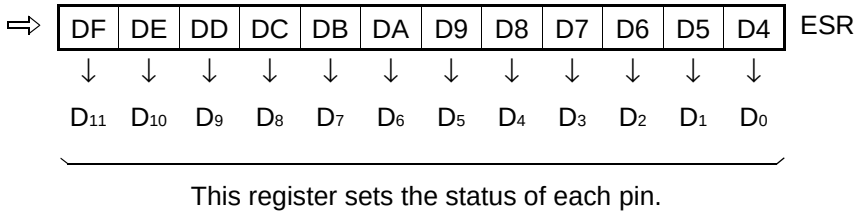
  Writes data from D_0 to D_{11} pins to bits D4 to DF in the shift register.
  Data is output to the SO pin on the shift clock (CLK) signal (The first 4 bits output data D0 to D3, so the converted output should be read as data bits 5 through 16.).
  Note that the data value is “0” for pins designated for output in the ESR (expander status register) as well as analog output pins.

  Shift register



- Expander Status Register [Channel select = “1111”]

  Shift register



Setting	Pin status
“0”	• Input standby status (Hi-Z output) • D_{11} to D_4 pins used for analog output should be set to “0.”
“1”	• Output state

Note: After power $V_{CC}D$ is turned on, the state of pins and registers is as follows.

Pin	State
AO_1 to AO_4	"L" output
D_{11}/AO_5 to D_4/AO_{12}	Hi-Z state (input state)
D_3 to D_0	Hi-Z state (input state)

Register	State
Shift register	Bits DF to D8 are "0," and D7 to D0 are not defined (retain prior state).
D/A register	All reset to "0."
Parallel output register	Not defined (retain prior state).
Expander status register (ESR)	All reset to "0."

- ESR settings have priority in determining pin states. Switching between input standby state and analog output state is enabled even when the ESR value is "1." When the ESR value returns to "0", the pin returns to its previously defined state.
- In input standby state with AO set for Hi-Z output, the AO output setting can be used for transition to AO output state.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Rating		Unit
			Min.	Max.	
Power supply voltage	$V_{CC}A$	Based on GND (Ta = +25°C)	–0.3	+7.0	V
	$V_{CC}D$		–0.3	$V_{CC}A$*	V
	V_{DD}		–0.3	$V_{CC}A$*	V
Input voltage 1	$V_{in}1$	SI, CLK, $\overline{CS}$, SO, D_0 to D_3	–0.3	$V_{CC}D$ + 0.3	V
Output voltage 1	$V_{out}1$		–0.3	$V_{CC}D$ + 0.3	V
Input voltage 2	$V_{in}2$	D_4 to D_{11}	–0.3	$V_{CC}A$ + 0.3	V
Output voltage 2	$V_{out}2$		–0.3	$V_{CC}A$ + 0.3	V
Power consumption	P_D	—	—	250	mW
Operating temperature	Ta	—	–20	+85	°C
Storage temperature	T_{stg}	—	–55	+150	°C

* : $V_{CC}A \geqq V_{CC}D$, $V_{CC}A \geqq V_{DD}$

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Power supply voltage	$V_{CC}A$	—	4.5	5.0	5.5	V
	$V_{CC}D$	$V_{CC}A \geqq V_{CC}D$	2.7	—	$V_{CC}A$	V
	V_{DD}	$V_{CC}A \geqq V_{DD}$	2.0	—	$V_{CC}A$	V
	GND	—	—	0	—	V
Analog output current	I_{AL}	Source current	—	—	1.0	mA
	I_{AH}	Sink current	—	—	1.0	mA
Oscillation limit output capacity	C_{OL}	—	—	—	1.0	µF
Operation temperature	Ta	—	–20	—	+85	°C

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

■ ELECTRICAL CHARACTERISTIC

1. DC Characteristics

(1) Digital section

($V_{CC}D \leqq V_{CC}A$, Ta = –20°C to +85°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit
				Min.	Typ.	Max.	
Power supply voltage	$V_{CC}D$	$V_{CC}D$	—	2.7	5.0	5.5	V
Power supply current	$I_{CC}D$		CLK =1 MHz, (Unloaded)	—	0.2	0.5	mA
Standby current	$I_{CC}S$		CLK, SI, $\overline{CS}$ Stop $V_{in} = V_{CC}D$ or GND	–10	—	+10	µA
Input leak current	I_{ILK1}	CLK, SI, $\overline{CS}$, D_0 to D_3	V_{in} = 0 to $V_{CC}D$	–10	—	+10	µA
"H" level input voltage	V_{IH1}		$V_{CC}D \geqq 4.0$ V	0.5 × $V_{CC}D$	—	—	V
			$V_{CC}D < 4.0$ V	2.0	—	—	V
"L" level input voltage	V_{IL1}		—	—	—	0.2 × $V_{CC}D$	V
High-impedance leak current	I_{OLK}	SO	V_{in} = 0 to $V_{CC}D$	–10	—	+10	µA
"H" level output voltage	V_{OH1}	SO, D_0 to D_3	I_{OH} = –0.4 mA	$V_{CC}D$ – 0.4	—	—	V
"L" level output voltage	V_{OL1}		I_{OL} = 2.5 mA	—	—	0.4	V

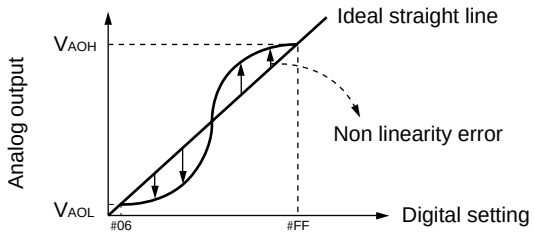
(2) D/A converter section

($V_{CC}A$ = 5 V ± 10%, Ta = –20°C to +85°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit
				Min.	Typ.	Max.	
Power supply voltage	V_{DD}	V_{DD}	$V_{DD} \leqq V_{CC}A$	2.0	5.0	5.5	V
Power supply current	I_{DD}		$V_{DD} \leqq V_{CC}A$	—	1.2	2.5	mA
Resolution	Res	AO_1 to AO_{12}	Unload $V_{DD} = V_{CC}A$ – 0.1 V Digital value: #06 to #FF	—	8	—	bits
Monotonic increase	Rem			—	8	—	bits
Nonlinearity error	LE			–1.5	—	+1.5	LSB
Differential linearity error	DLE			–1.0	—	+1.0	LSB

Nonlinearity error: Deviation (error) in input/output curves with respect to an ideal straight line connecting output voltage at "06" and output voltage at "FF."

Differential linearity error: Deviation (error) in amplification with respect to theoretical increase in amplification per 1-bit increase in digital value.



Note: The value of V_{AOH} and V_{DD}, and the value of V_{AOL} and GND are not necessarily equivalent.

(3) Operational Amplifier/Analog output section

(V_{DD} = $V_{CC}A$ = 5.0 V, Ta = –20°C to +85°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit
				Min.	Typ.	Max.	
Power supply voltage	V_{CCA}	$V_{CC}A$	—	4.5	5.0	5.5	V
Power supply current	I_{CCA}		#80 setting (Unloaded)	—	1.0	3.7	mA
Input leak current	I_{ILK2}	D_4 to D_{11}	V_{in} = 0 to $V_{CC}A$	–10	—	+10	µA
"H" level digital input voltage	V_{IH2}		—	0.5 × $V_{CC}A$	—	—	V
"L" level digital input voltage	V_{IL2}		—	—	—	0.2 × $V_{CC}A$	V
"H" level digital output voltage	V_{OH2}		I_{OH} = –0.4 mA	$V_{CC}A$ – 0.4	—	—	V
"L" level digital output voltage	V_{OL2}		I_{OL} = 2.5 mA	—	—	0.4	V
Analog output minimum voltage 1	V_{AOL1}	AO_1 to AO_{12}	I_{AL} = 0 A #00 setting	GND	—	0.1	V
Analog output minimum voltage 2	V_{AOL2}		I_{AL} = 0.5 mA #00 setting	–0.2	GND	0.2	V
Analog output minimum voltage 3	V_{AOL3}		I_{AH} = 0.5 mA #00 setting	GND	—	0.2	V
Analog output minimum voltage 4	V_{AOL4}		I_{AL} = 1.0 mA #00 setting	–0.3	GND	0.3	V
Analog output minimum voltage 5	V_{AOL5}		I_{AH} = 1.0 mA #00 setting	GND	—	0.3	V
Analog output maximum voltage 1	V_{AOH1}	AO_1 to AO_{12}	I_{AL} = 0 A #FF setting	$V_{CC}A$ – 0.1	—	$V_{CC}A$	V
Analog output maximum voltage 2	V_{AOH2}		I_{AL} = 0.5 mA #FF setting	$V_{CC}A$ – 0.2	—	$V_{CC}A$	V
Analog output maximum voltage 3	V_{AOH3}		I_{AH} = 0.5 mA #FF setting	$V_{CC}A$ – 0.2	$V_{CC}A$	$V_{CC}A$ + 0.2	V
Analog output maximum voltage 4	V_{AOH4}		I_{AL} = 1.0 mA #FF setting	$V_{CC}A$ – 0.3	—	$V_{CC}A$	V
Analog output maximum voltage 5	V_{AOH5}		I_{AH} = 1.0 mA #FF setting	$V_{CC}A$ – 0.3	$V_{CC}A$	$V_{CC}A$ + 0.3	V

Note: I_{AH}: Analog output sink current I_{AL}: Analog output source current

2. AC Characteristics

- For operation at $V_{CC}D$ = 5.0 V

(V_{DD} = $V_{CC}A$ = 5.0 V, Ta = –20°C to +85°C)

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Clock “L” level pulse width	t_{CKL}	—	200	—	—	ns
Clock “H” level pulse width	t_{CKH}	—	200	—	—	ns
Clock rise time	t_{Cr}	—	—	—	200	ns
Clock fall time	t_{Cf}	—	—	—	200	ns
Serial input setup time	t_{SSU}	—	30	—	—	ns
Serial input hold time	t_{SHD}	—	60	—	—	ns
Serial output delay time	t_{SOD}	See “Load condition 1”	0	80	170	ns
$\overline{CS}$ input setup time	t_{CSU}	—	100	—	—	ns
$\overline{CS}$ hold time	t_{CCH}	—	200	—	—	ns
$\overline{CS}$ “H” level hold time	t_{CSH}	—	100	—	—	ns
Data output enable time	t_{SO}	—	—	—	200	ns
Data output float time	t_{SOZ}	—	—	—	200	ns
Parallel input setup time	t_{PSU}	—	30	—	—	ns
Parallel input hold time	t_{PHD}	—	60	—	—	ns
Parallel output delay time	t_{POD}	See “Load condition 1”	—	100	170	ns
Analog output delay time	t_{AOD}	See “Load condition 2”	—	30	100	µs
Power supply rise time	t_R	—	—	—	50	ms
Power-on reset non-startup power supply variation	ΔV_R	—	–10	—	10	V/µs

- For operation at $V_{CC}D$ = 3.0 V *1

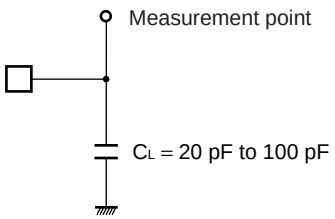
($V_{CC}D$ = 3.0 V, Ta = –20°C to +85°C)

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Serial output delay time	t_{SOD}	See “Load condition 1”*2	0	120	300	ns
Parallel output delay time	t_{POD}	See “Load condition 2”*3	—	120	300	ns

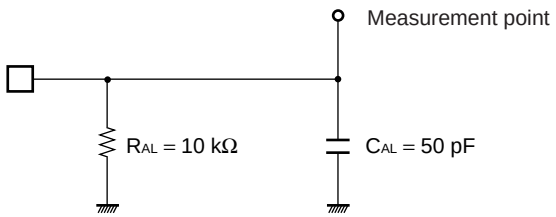
*1: Items not listed are identical to characteristics for $V_{CC}D$ = 5.0 V.
*2: Cascade connection enabled at 1.5 MHz.
*3: Applied to D0 to D3 operating at $V_{CC}D$.

Load Conditions

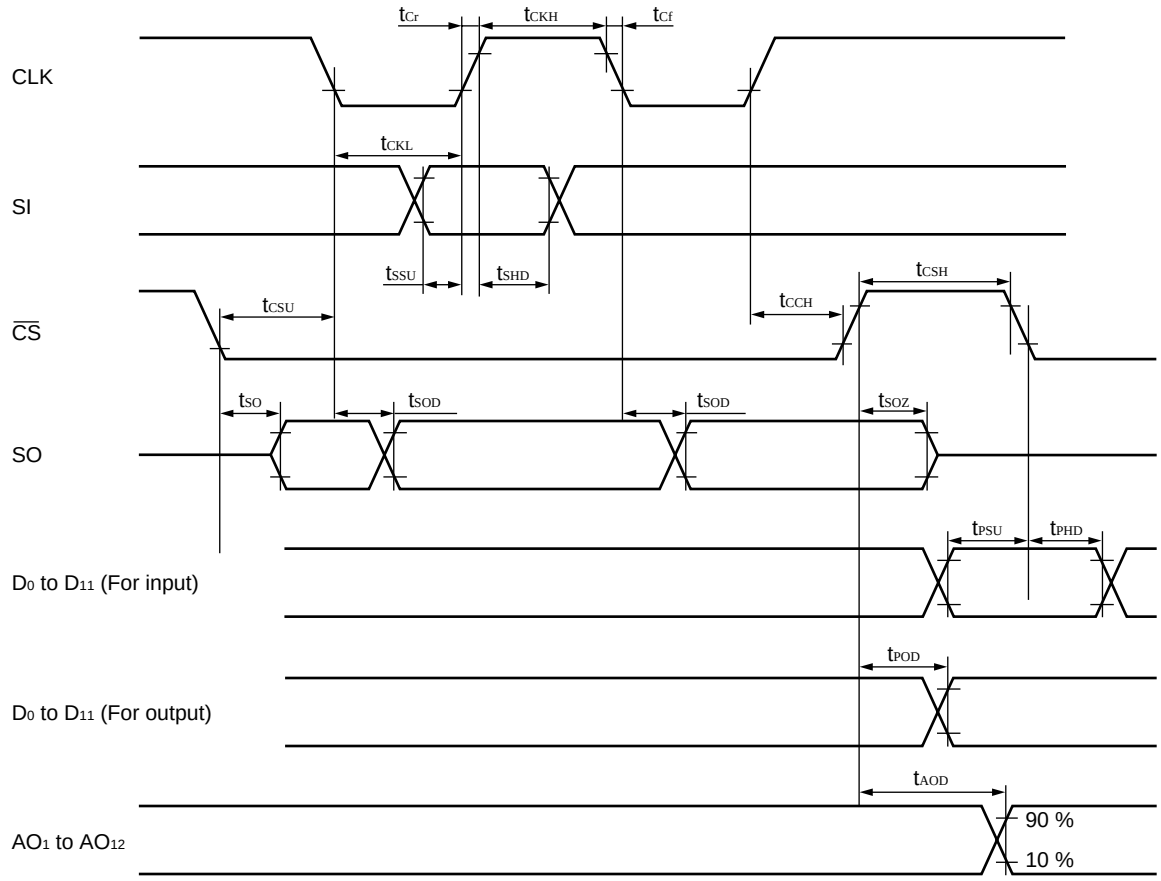
• Load condition 1



• Load condition 2



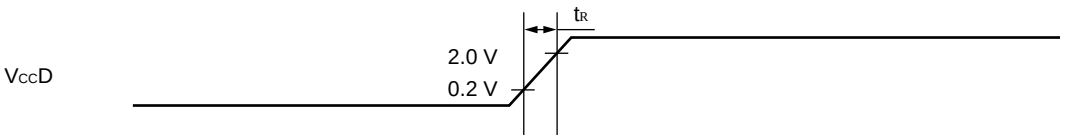
- Input/Output Timing ($\overline{CS}$ method)



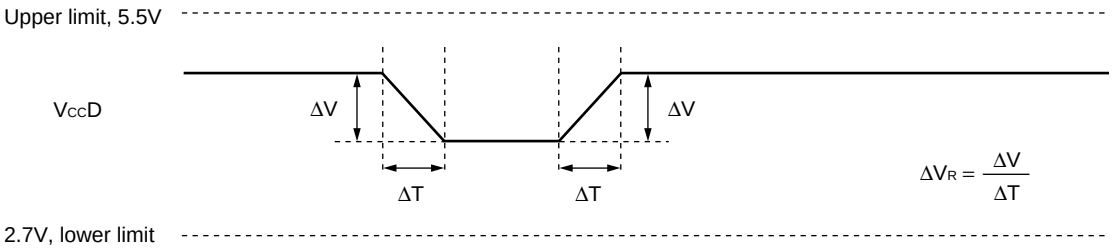
The decision level for CLK, SI, $\overline{CS}$, SO, and D_0 to D_3 is 80% and 20% of $V_{CC}D$. The decision level for D_4 to D_{11} is 80% and 20% of $V_{CC}A$, and for AO_1 to AO_{12} is 90% and 10% of $V_{CC}A$.

- Power Supply Timing

- Power-On Timing



- Power-On Reset Non-Startup Supply Variation

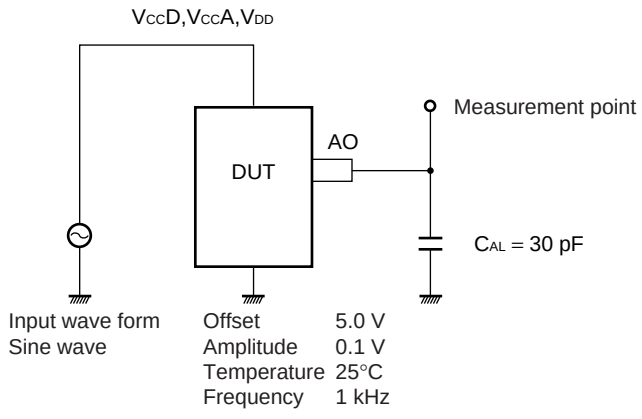


3. Analog Output Noise Characteristic

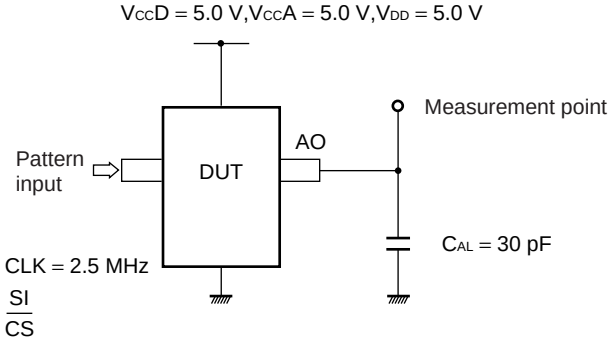
(V_{DD} = $V_{CC}D$ = $V_{CC}A$ = 5.0 V, Ta = +25°C)

Parameter	Symbol	Conditions	Measurement condition	Value			Unit
				Min.	Typ.	Max.	
Digital supply noise reduction ratio	P_{SRD}	f_{NOISE} = 1 kHz	1	—	—	20	dB
Analog supply noise reduction ratio	P_{SRA}	f_{NOISE} = 1 kHz	1	—	—	20	dB
D/A supply noise reduction ratio	P_{SRDA}	f_{NOISE} = 1 kHz	1	—	—	0	dB
Operating noise	V_{N1}	• During serial transfer • During analog operation • During Hi-Z commands. See “Operating Noise V_{N1}.”	2	–30	—	30	mV
I/O expander operating noise 1	V_{N2}	• Serial → parallel conversion See “I/O Expander Operating Noise 1 V_{N2}.” During digital-only pin operation • During parallel → serial conversion • ESR setting During digital input/digital output switching	2	–30	—	30	mV
I/O expander operating noise 2	V_{N3}	• During serial → parallel conversion See “I/O Expander Operating Noise 2 V_{N3}.” During digital/analog capable pin operation • ESR setting During digital output/digital output switching	2	–0.1	—	0.1	V

• Measurement condition 1



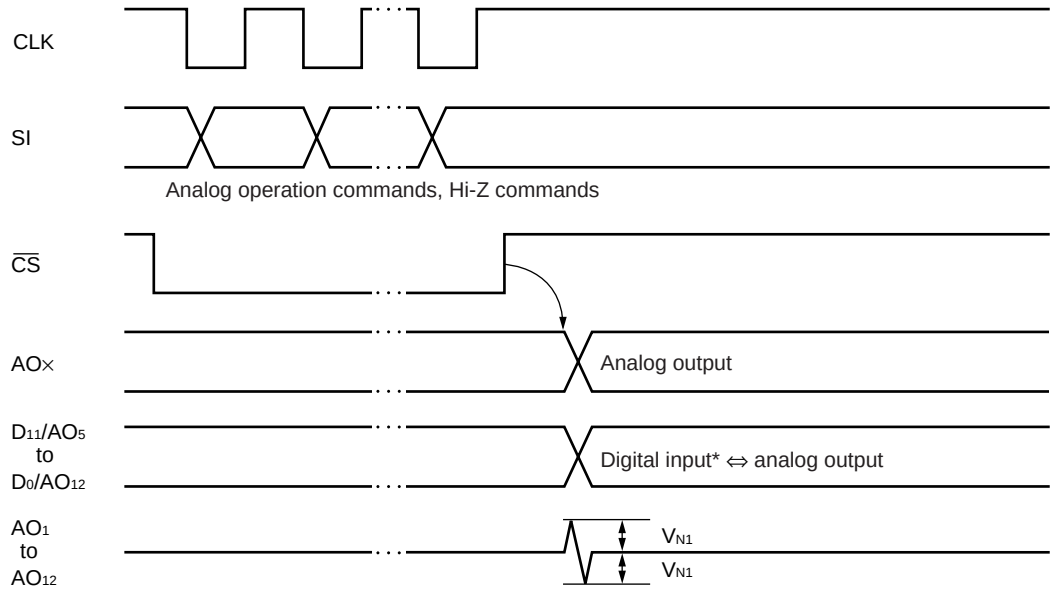
• Measurement condition 2



- Analog Output Noise Description

- Output Noise V_{N1}

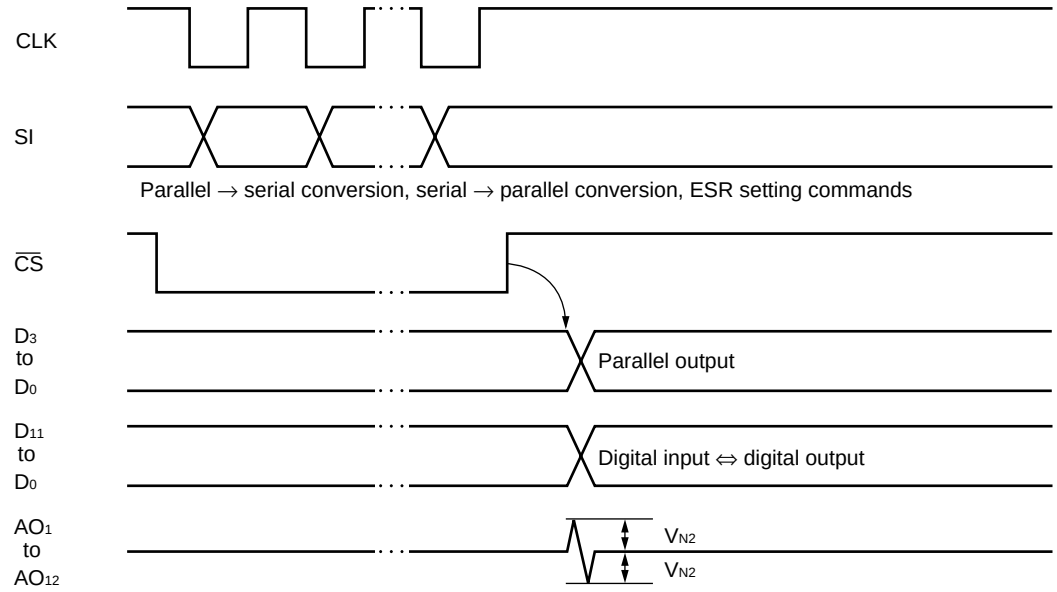
Noise to analog output during serial data transfer, analog operation, Hi-Z commands.



* Hi-Z state = digital input state.

- I/O Expander Operation Noise 1 V_{N2}

Noise to analog output during parallel → serial conversion commands, serial → parallel conversion command for digital-only pins, or ESR setting commands for switching between digital input and digital output.

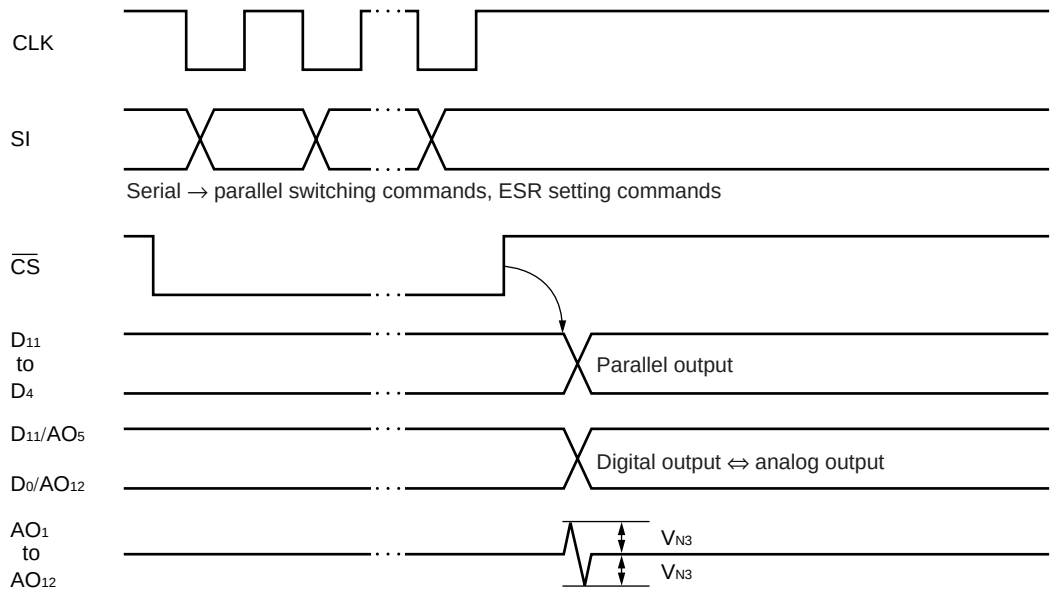


(Continued)

(Continued)

- I/O Expander Operation Noise 2 V_{N3}

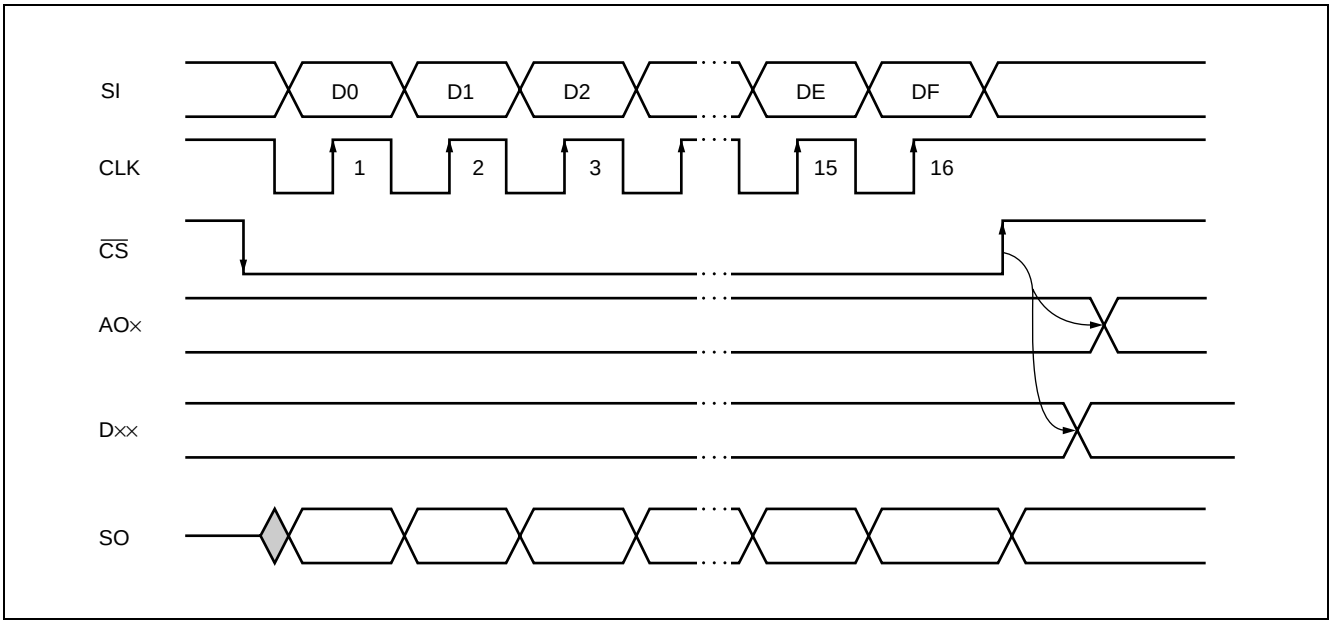
Noise to analog output during serial → parallel switching commands for digital-only pins, or ESR setting commands for switching between digital output and analog output.



■ DATA INPUT/OUTPUT TIMING

MB88146A Data Input/Output Timing (Serial Bus Format)

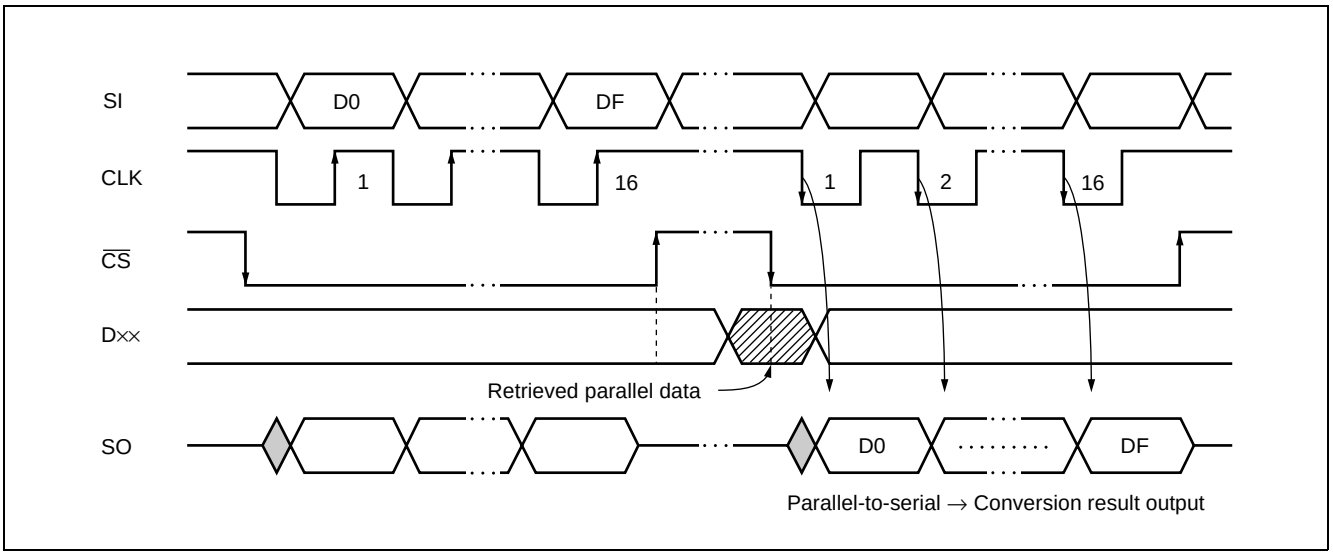
- D/A converter operation, and I/O expander (serial → parallel conversion) operation, and ESR writing operation.



Data input is enabled at the falling edge of the $\overline{CS}$ signal. 16-bit data is input, and the shift register command is executed at the rising edge of $\overline{CS}$.

In D/A converter operation, the analog output selected at the rising edge of $\overline{CS}$ is the conversion result. In serial → parallel conversion, the digital output selected at the rising edge of $\overline{CS}$ is the conversion result. In ESR write operation, ESR data is set and pin status determined at the rising edge of $\overline{CS}$.

- I/O expander (parallel → serial conversion) operation



Data input is enabled at the falling edge of the $\overline{CS}$ signal. 16-bit data (parallel → serial conversion commands) is input and commands accepted at the rising edge of $\overline{CS}$. At the falling edge of $\overline{CS}$, data from the parallel input is loaded into bits D4 to DF of the shift register, and output from the SO pin timed to the falling edge of the CLK signal.

■ USAGE PRECAUTIONS

1. Preventing Latch-Up

A condition known as “latch-up” may occur when the input or output pins of a CMOS IC device are exposed to voltages higher then $V_{CC}D$ or $V_{CC}A$ or lower than GND voltage, or when voltages are applied to the device in excess of rated values for $V_{CC}D$, VccA, or V_{DD} to GND voltages. Latchup produces a rapid increase in power supply current, and may result in thermal destruction of elements. Users should take sufficient precautions to ensure that absolute maximum ratings are not exceeded at any time during use.

2. Power Supply Pins

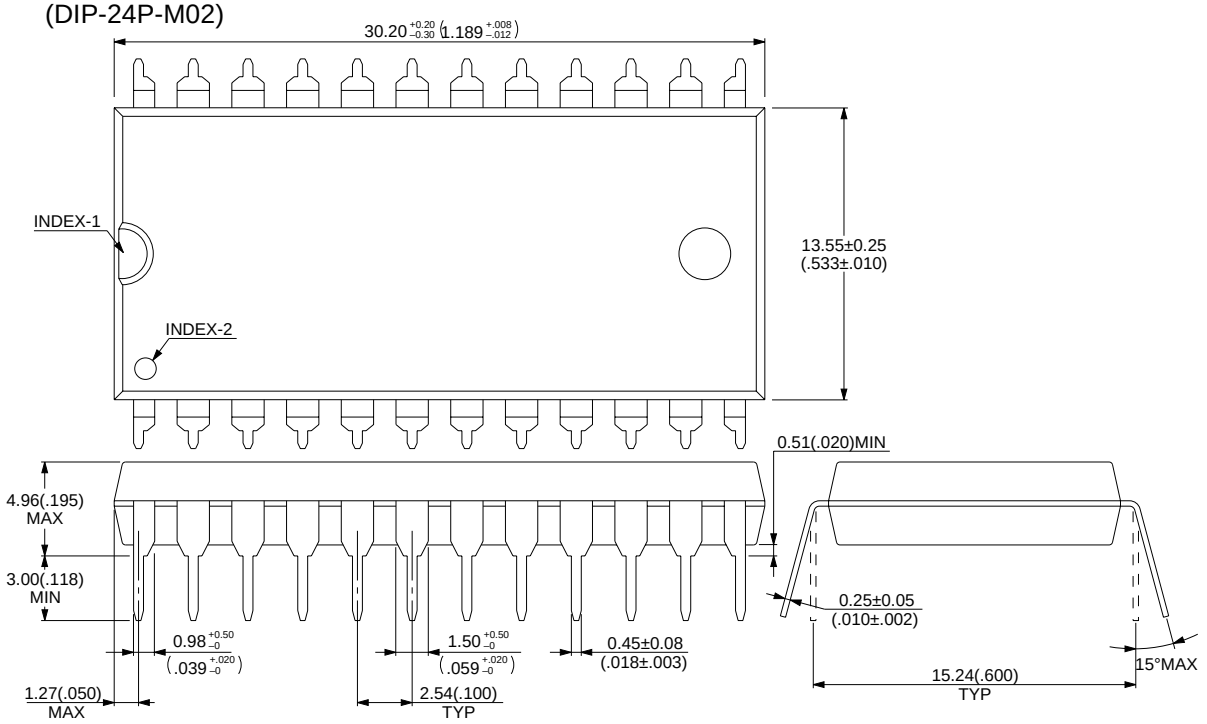
The power supply should be connected to the $V_{CC}D$, $V_{CC}A$, V_{DD}, and GND terminals of the MB88146A with as low an impedance as possible.
In addition, it is recommended that ceramic capacitors or approximately 0.1 μF be connected as bypass capacitors between the $V_{CC}D$, $V_{CC}A$, and V_{DD} terminals and the GND terminals.

■ ORDERING INFORMATION

Part number	Package	Remarks
MB88146AP	24-pin Plastic DIP (DIP-24P-M02)	
MB88146APFV	24-pin Plastic SSOP (FPT-24P-M03)	

■ PACKAGE DIMENSIONS

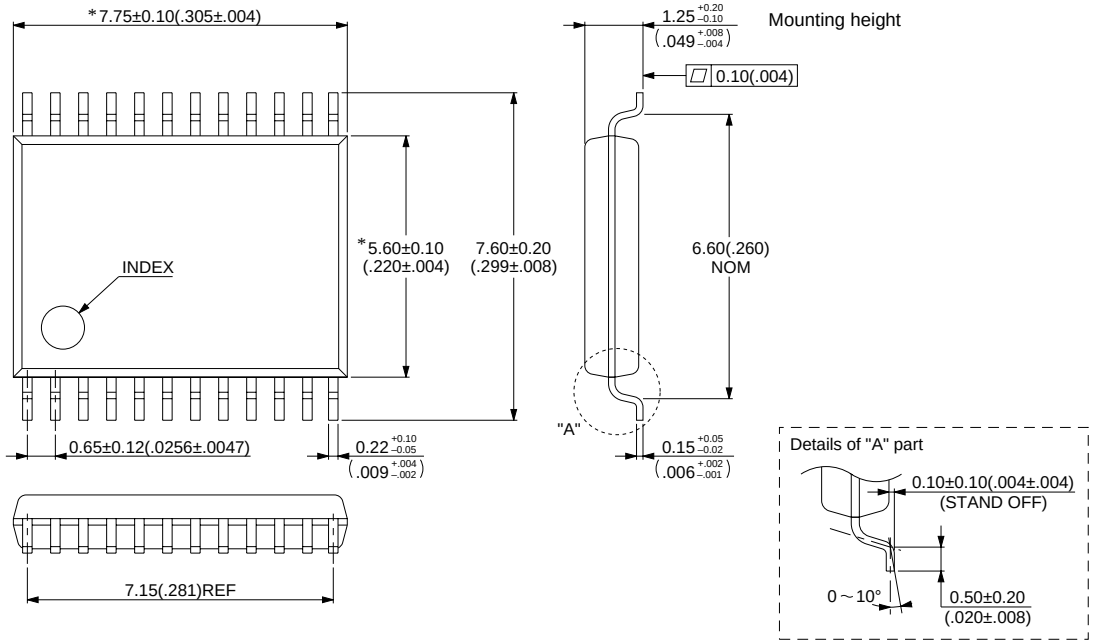
24-pin Plastic DIP
(DIP-24P-M02)



Dimensions in mm (inches)

24-pin Plastic SSOP
(FPT-24P-M03)

* : These dimensions do not include resin protrusion.



Dimensions in mm (inches)

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