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TENTATIVE TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

# 16 MBIT (2 M × 8 BITS) CMOS NAND FLASH $E^2$PROM

## DESCRIPTION

The TC5816 device is a single 5.0-volt 16 Mbit NAND Electrically Erasable and Programmable Read Only Memory (NAND Flash EEPROM) with spare 64 K × 8 bits. The device is organized as 264 bytes × 16 pages × 512 blocks. The device has a 264-byte, static register which allows the program and read data to be transferred between the register and the memory cell array in 264-byte increments. The Erase operation is implemented in a single block unit (4 Kbytes + 128 bytes: 264 bytes × 16 pages).

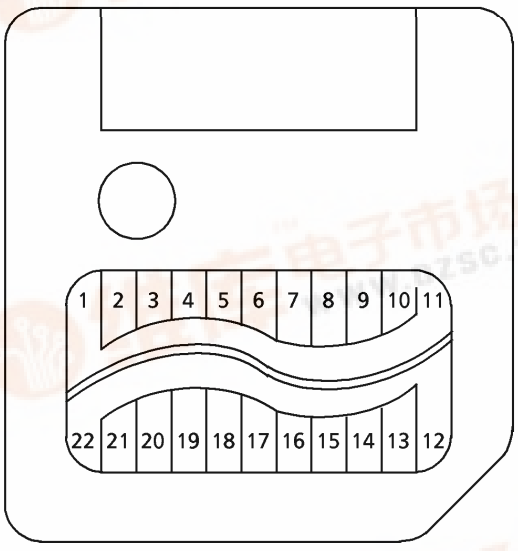
The TC5816 is a serial type of memory device which utilizes the I/O pins for both address and data input/output as well as command inputs. The Erase and Program operations are automatically executed, making the device most suitable for applications such as solid state file storage, voice recording, image file memory for still cameras and other systems which require high-density, and non-volatile memory data storage.

## FEATURES

- Organization
  - Memory cell array 264 × 8 K × 8
  - Register 264 × 8
  - Page size 264 bytes
  - Block size (4 K + 128) bytes
- Mode
  - Read, Reset, Auto Page Program
  - Auto Block Erase, Suspend / Resume, Status Read
- Mode control
  - Serial input/output
  - Command control
- Power supply
  - $V_{CC}$ = 5.0 V ± 0.5 V
- Operating temperature
  - 0° to 55°C
- Access time
  - Cell array-Register 25 μs max
  - Serial Read Cycle 80 ns min
- Operating current
  - Read (80 ns cycle) 15 mA typ
  - Program (ave.) 40 mA typ
  - Erase (ave.) 20 mA typ
  - Standby 100 μA
- Package
  - TC5816BDC : FDC-22
    (Weight: 1.8 g typ)

## PIN ASSIGNMENT (TOP VIEW)

TC5816BDC




## PIN NAMES

| | | |
|---|---|---|
| 1, 10, 11 | $V_{SS}$ | Ground |
| 2 | CLE | Command Latch Enable |
| 3 | ALE | Address Latch Enable |
| 4 | $\overline{WE}$ | Write Enable |
| 5 | $\overline{WP}$ | Write Protect |
| 6 to 9 | I/O1 to 4 | I/O Port |
| 13 to 16 | I/O5 to 8 | I/O Port |
| 17 | LVD | Low Voltage Detect |
| 18 | GND | Ground Input |
| 19 | R/$\overline{B}$ | Ready/Busy |
| 20 | $\overline{RE}$ | Read Enable |
| 21 | $\overline{CE}$ | Chip Enable |
| 22, 12 | $V_{CC}$ | Power Supply (5.0 V) |

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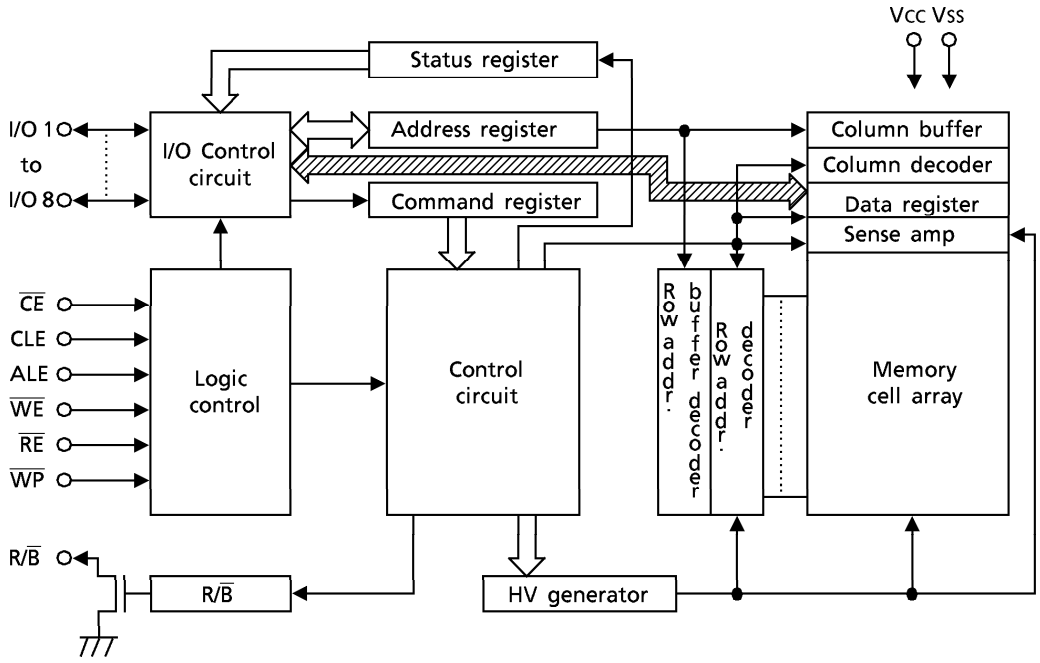
## BLOCK DIAGRAM




## ABSOLUTE MAXIMUM RATINGS

| SYMBOL | RATING | VALUE | UNIT |
|---|---|---|---|
| $V_{CC}$ | Power Supply | − 0.6 to 7.0 | V |
| $V_{IN}$ | Input Voltage | − 0.6 to 7.0 | V |
| $V_{I/O}$ | Input/Output Voltage | − 0.6 V to Vcc + 0.5 V (≦ 7.0 V) | V |
| $P_D$ | Power Dissipation | 0.5 | W |
| $T_{STG}$ | Storage Temperature | − 20 to 65 | °C |
| $T_{OPR}$ | Operating Temperature | 0 to 55 | °C |

## CAPACITANCE *(Ta = 25°C, f = 1 MHz)

| SYMBOL | PARAMETER | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input | $V_{IN}$ = 0 V | − | 5 | 10 | pF |
| $C_{OUT}$ | Output | $V_{OUT}$ = 0 V | − | 5 | 10 | pF |

* This parameter is periodically sampled and is not tested for every component.

## VALID BLOCK (1)

| SYMBOL | PARAMETER | TC5816 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $N_{VB}$ | Valid Block Number | 502 | 508 | 512 | Blocks |

(1) The TC5816 occasionally contains unusable blocks. Refer to Application Note (17) toward the end of this document.

## DC RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Power Supply | 4.5 | 5.0 | 5.5 | V |
| $V_{IH}$ | High Level Input Voltage | 2.2 | – | $V_{CC}$ + 0.5 | V |
| $V_{IL}$ | Low Level Input Voltage | – 0.3* | – | 0.8 | V |

* – 2 V (pulse width ≦ 20 ns)

## DC CHARACTERISTICS (Ta = 0° to 55°C, $V_{CC}$ = 5.0 V ± 0.5 V)

| SYMBOL | PARAMETER | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{IL}$ | Input Leak Current | $V_{IN}$ = 0 V to $V_{CC}$ | – | – | ± 10 | μA |
| $I_{LO}$ | Output Leak Current | $V_{OUT}$ = 0.4 V to $V_{CC}$ | – | – | ± 10 | μA |
| $I_{CCO1}$ | Operating Current (Serial Read) | $\overline{CE}$ = $V_{IL}$, Iout = 0 mA, $t_{cycle}$ = 80 ns | – | 15 | 30 | mA |
| $I_{CCO2}$ | Operating Current (Command Input) | $t_{cycle}$ = 80 ns | – | 15 | 30 | mA |
| $I_{CCO3}$ | Operating Current (Data Input) | $t_{cycle}$ = 80 ns | – | 40 | 60 | mA |
| $I_{CCO4}$ | Operating Current (Address Input) | $t_{cycle}$ = 80 ns | – | 15 | 30 | mA |
| $I_{CCO5}$ | Programming Current | – | – | 40 | 60 | mA |
| $I_{CCO6}$ | Erasing Current | – | – | 20 | 40 | mA |
| $I_{CCS1}$ | Standby Current | $\overline{CE}$ = $V_{IH}$ | – | – | 1 | mA |
| $I_{CCS2}$ | Standby Current | $\overline{CE}$ = $V_{CC}$ – 0.2 V | – | – | 100 | μA |
| $V_{OH}$ | High Level Output Voltage | $I_{OH}$ = – 400 μA | 2.4 | – | – | V |
| $V_{OL}$ | Low Level Output Voltage | $I_{OL}$ = 2.1 mA | – | – | 0.4 | V |
| $I_{OL}$ (R/$\overline{B}$) | Output Current of (R/$\overline{B}$) Pin | $V_{OL}$ = 0.4 V | – | 8 | – | mA |

## AC CHARACTERISTICS AND OPERATING CONDITIONS (Ta = 0° to 55°C, $V_{CC}$ = 5.0 V ± 0.5 V) (1)

| SYMBOL | PARAMETER | MIN | MAX | UNIT | NOTE |
|---|---|---|---|---|---|
| $t_{CLS}$ | CLE Set-Up Time | 20 | – | ns | |
| $t_{CLH}$ | CLE Hold Time | 40 | – | ns | |
| $t_{CS}$ | $\overline{CE}$ Set-Up Time | 20 | – | ns | |
| $t_{CH}$ | $\overline{CE}$ Hold Time | 40 | – | ns | |
| $t_{WP}$ | Write Pulse Width | 40 | – | ns | |
| $t_{ALS}$ | ALE Set-Up Time | 20 | – | ns | |
| $t_{ALH}$ | ALE Hold Time | 40 | – | ns | |
| $t_{DS}$ | Data Set-Up Time | 30 | – | ns | |
| $t_{DH}$ | Data Hold Time | 20 | – | ns | |
| $t_{WC}$ | Write Cycle Time | 80 | – | ns | (2) |
| $t_{WH}$ | $\overline{WE}$ High Hold Time | 20 | – | ns | |
| $t_{WW}$ | $\overline{WP}$ High to $\overline{WE}$ Falling Edge | 100 | – | ns | |
| $t_{RR}$ | Ready to $\overline{RE}$ Falling Edge | 20 | – | ns | |
| $t_{RC}$ | Read Cycle Time | 80 | – | ns | |
| $t_{REA}$ | $\overline{RE}$ Access Time (Serial Data Access) | – | 45 | ns | |
| $t_{CEH}$ | $\overline{CE}$ High Time for the Last Address in Serial Read Cycle | 250 | – | ns | (4) |
| $t_{REAID}$ | $\overline{RE}$ Access Time (ID Read) | – | 45 | ns | |
| $t_{RHZ}$ | $\overline{RE}$ High to Output High Impedance | – | 30 | ns | |
| $t_{CHZ}$ | $\overline{CE}$ High to Output High Impedance | – | 20 | ns | |
| $t_{REH}$ | $\overline{RE}$ High Hold Time | 20 | – | ns | |
| $t_{IR}$ | Output High Impedance to $\overline{RE}$ Rising Edge (Status Read) | 0 | – | ns | |
| $t_{RSTO}$ | $\overline{RE}$ Access Time (Status Read) | – | 45 | ns | |
| $t_{CSTO}$ | $\overline{CE}$ Access Time (Status Read) | – | 55 | ns | |
| $t_{RHW}$ | $\overline{RE}$ High to $\overline{WE}$ Low | 0 | – | ns | |
| $t_{WHC}$ | $\overline{WE}$ High to $\overline{CE}$ Low (Status Read) | 50 | – | ns | |
| $t_{WHR}$ | $\overline{WE}$ High to $\overline{RE}$ Low (Status Read) | 50 | – | ns | |
| $t_{AR1}$ | ALE Low to $\overline{RE}$ Low (ID Read) | 200 | – | ns | |
| $t_{CR}$ | $\overline{CE}$ Low to $\overline{RE}$ Low (ID Read) | 200 | – | ns | |
| $t_R$ | Memory Cell Array to Starting Address | – | 25 | μs | |
| $t_{WB}$ | $\overline{WE}$ High to Busy | – | 200 | ns | |
| $t_{AR2}$ | ALE Low to $\overline{RE}$ Low (Read Cycle) | 150 | – | ns | |
| $t_{RB}$ | $\overline{RE}$ Last Clock Rising Edge to Busy (in Sequential Read) | – | 200 | ns | |
| $t_{CRY}$ | $\overline{CE}$ High to Ready (in Case of Interception by $\overline{CE}$ in Read Mode) | – | 600 + tr(R/$\overline{B}$) | ns | (3) |
| $t_{RST}$ | Device Reset Time (Read/Program/Erase/after Suspend) | – | 10/20/500/10 | μs | |

## AC TEST CONDITIONS

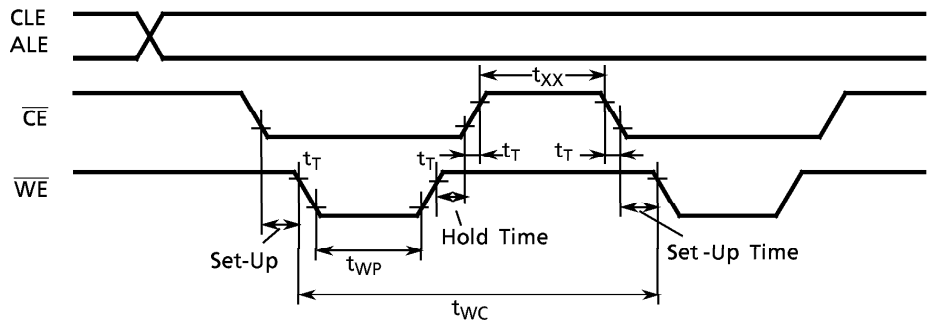
| | | |
|---|---|---|
| Input level | : | 2.4 V / 0.6 V |
| Input comparison level | : | 2.2 V / 0.8 V |
| Output data comparison level | : | 2.0 V / 0.8 V |
| Output load | : | 1 TTL & CL (100 pF) |

(1) Transition time ($t_T$) = 5 ns

(2) When CLE, ALE and $\overline{CE}$ are input at the clock pulse, $t_{WC}$ will exceed 80 ns

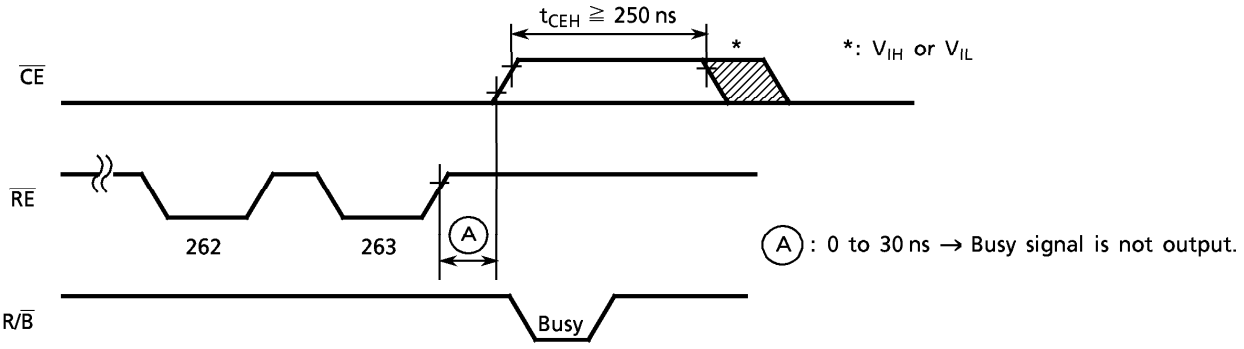
$$\underset{20\text{ ns}}{\text{Set-Up Time}} + \underset{40\text{ ns}}{\text{Hold Time}} + \underset{40\text{ ns}}{t_{WP}} + t_{XX} + \underset{20\text{ ns}}{4t_T}$$

(ex.)




(3) The $\overline{CE}$ High to Ready time depends on the pull-up resistor tied to the R/$\overline{B}$ pin. (Refer to Application Note (10) toward the end of this document.)

(4) If the delay between $\overline{RE}$ and $\overline{CE}$ is less than 200 ns and $t_{CEH}$ is greater than or equal to 250 ns, reading will stop.
If the $\overline{RE}$-to-$\overline{CE}$ delay is less than 30 ns, the device will not return to the Busy state.




## PROGRAMMING AND ERASING CHARACTERISTICS (Ta = 0° to 55°C, $V_{CC}$ = 5.0 V ± 0.5 V)

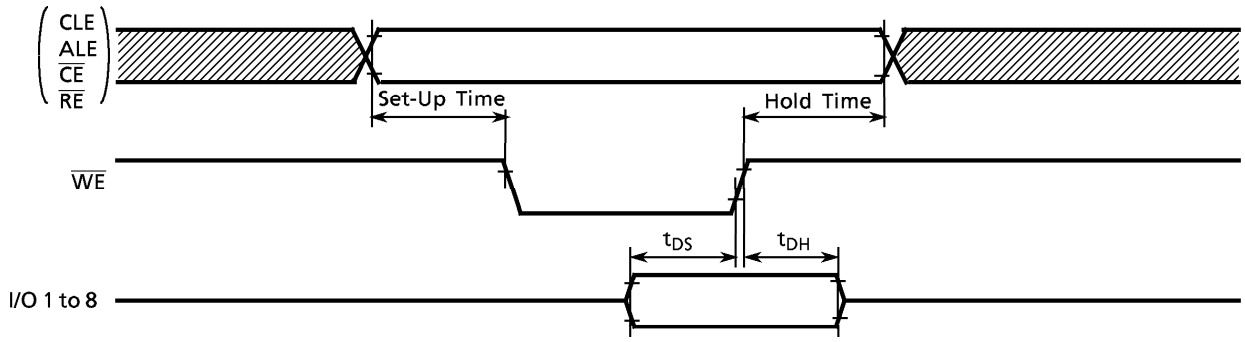
| SYMBOL | PARAMETER | MIN | TYP | MAX | UNIT | NOTE |
|---|---|---|---|---|---|---|
| $t_{PROG}$ | Average Programming Time | | 200 to 500 | 3000 | μs | |
| N | Number of Programming Cycles on Same Page | | | 10 | | (1) |
| $t_{BERASE}$ | Block Erasing Time | | 4.5 | 100 | ms | |
| $t_{SR}$ | Suspend Input to Ready | | | 500 | μs | |
| $N_{W/E}$ | Number of Write/Erase Cycles | | | $1 \times 10^6$ | cycles | (2) |

(1) Refer to Application Note (15) toward the end of this document.

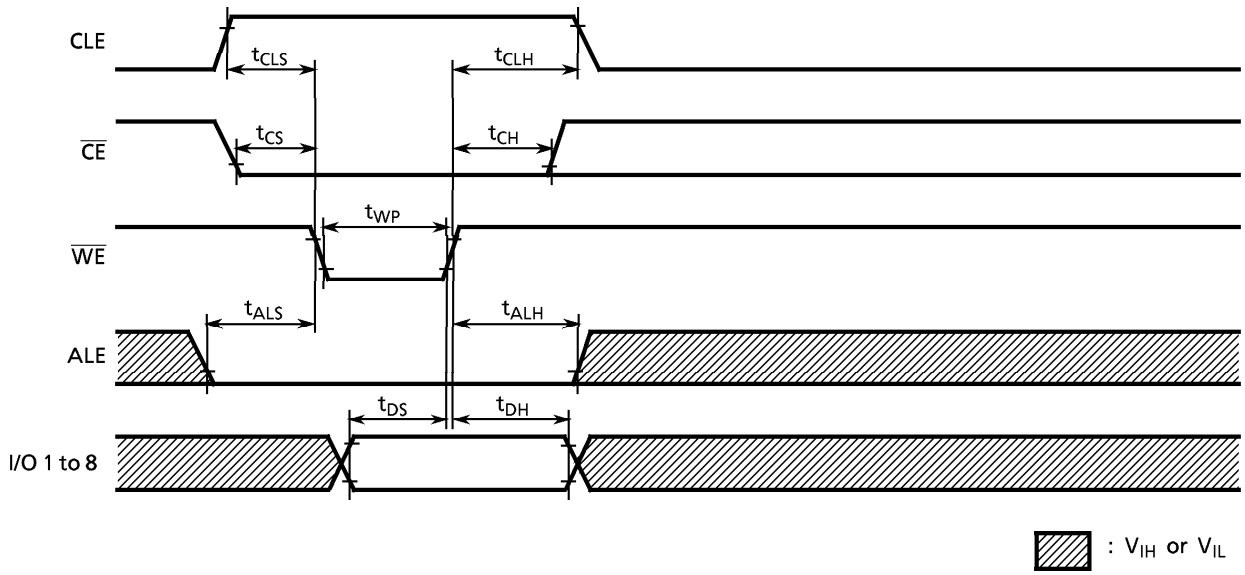
(2) Refer to Application Note (18) toward the end of this document.

## TIMING DIAGRAMS

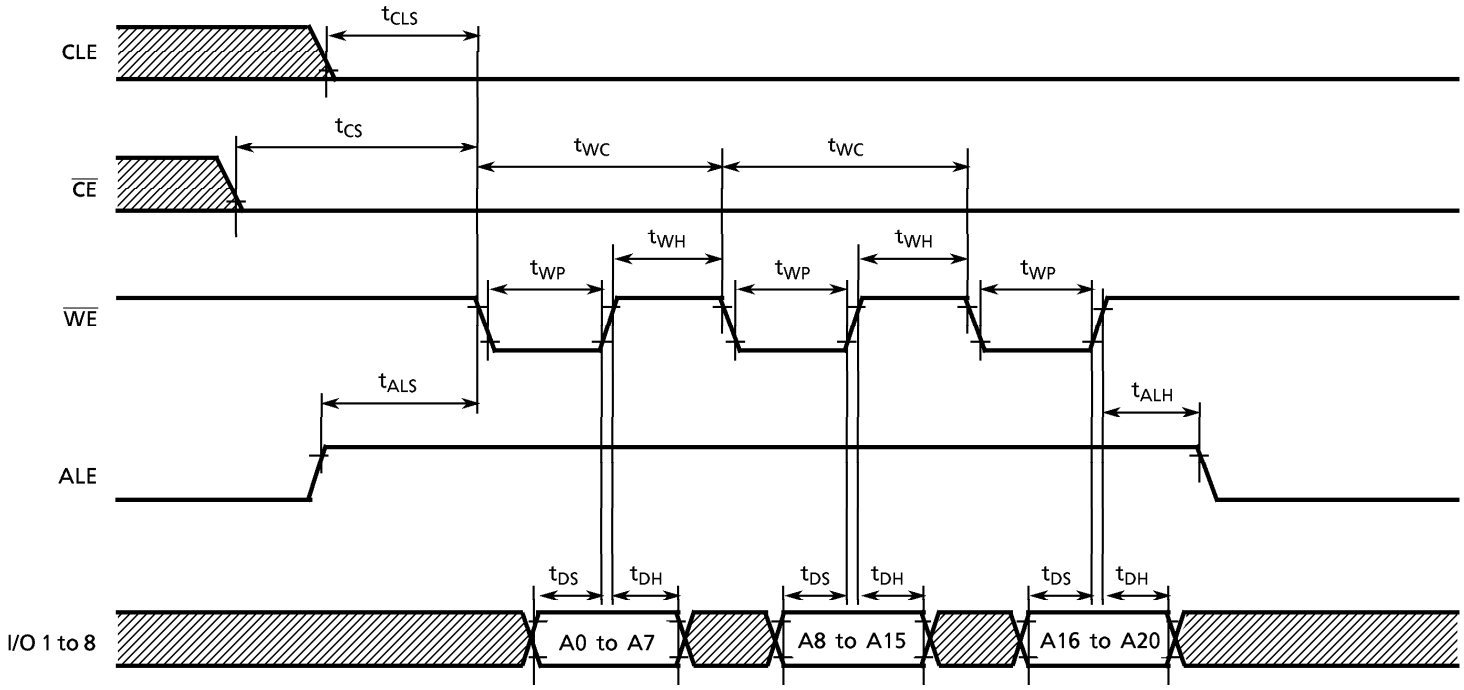
### Latch Timing Diagram for Command/Address /Data



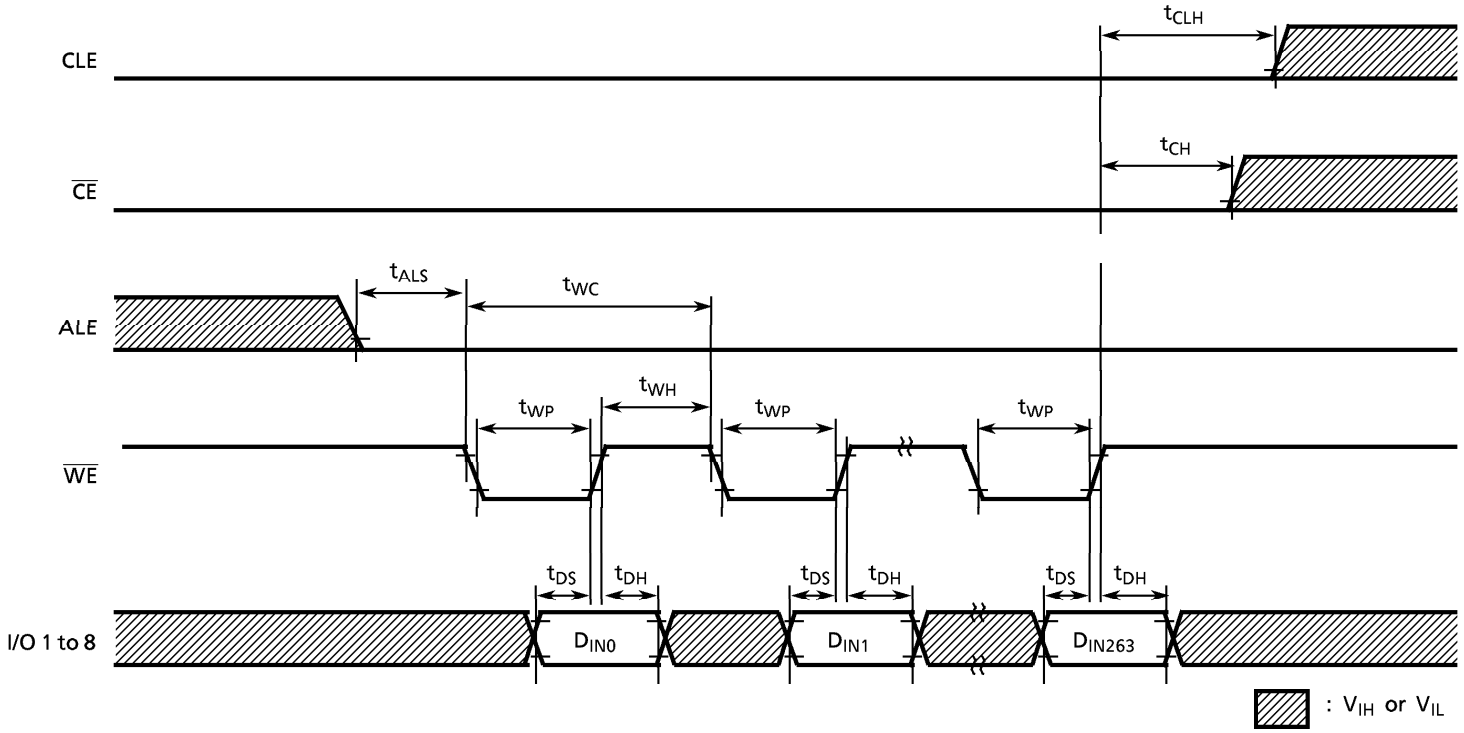

### Command Input Cycle Timing Diagram



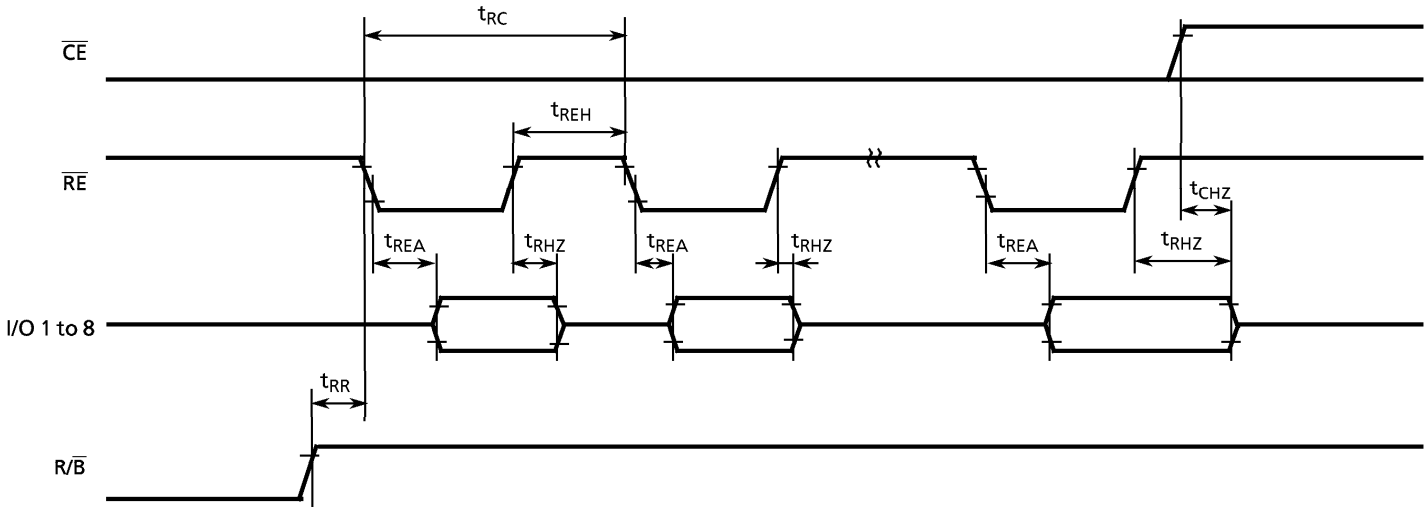
## Address Input Cycle Timing Diagram



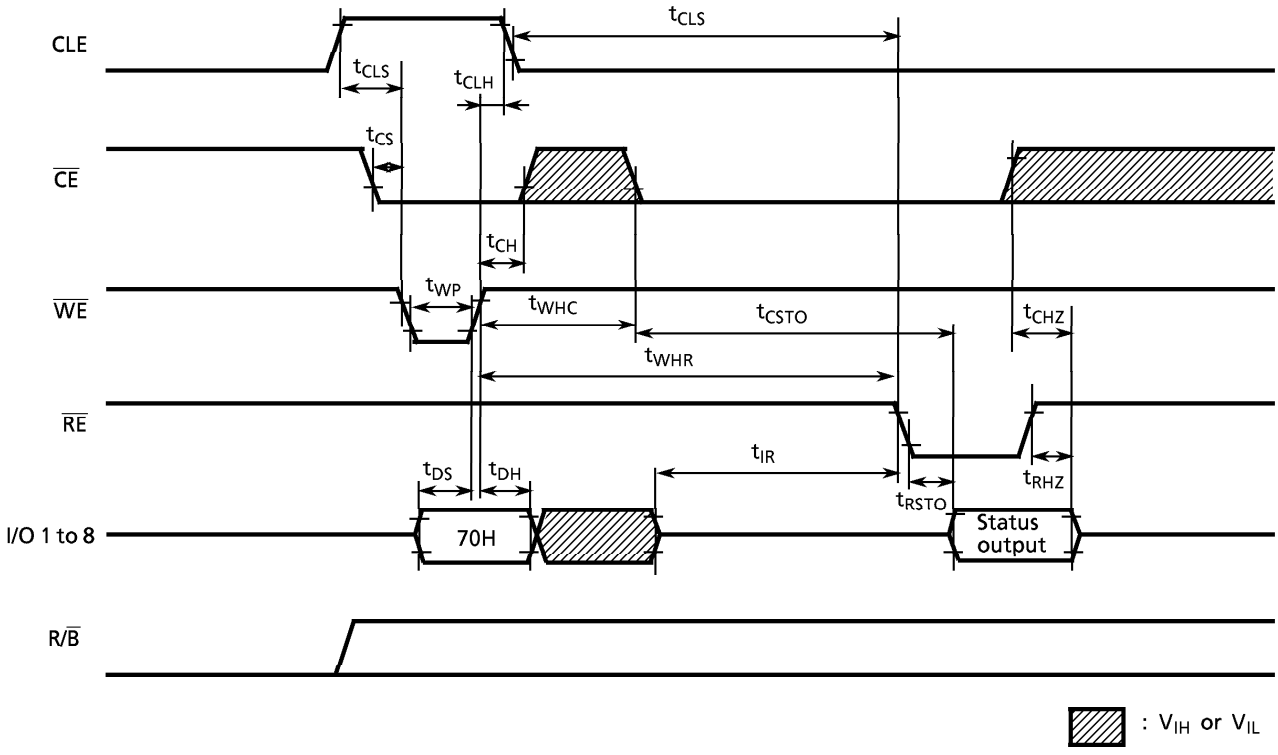

## Data Input Cycle Timing Diagram



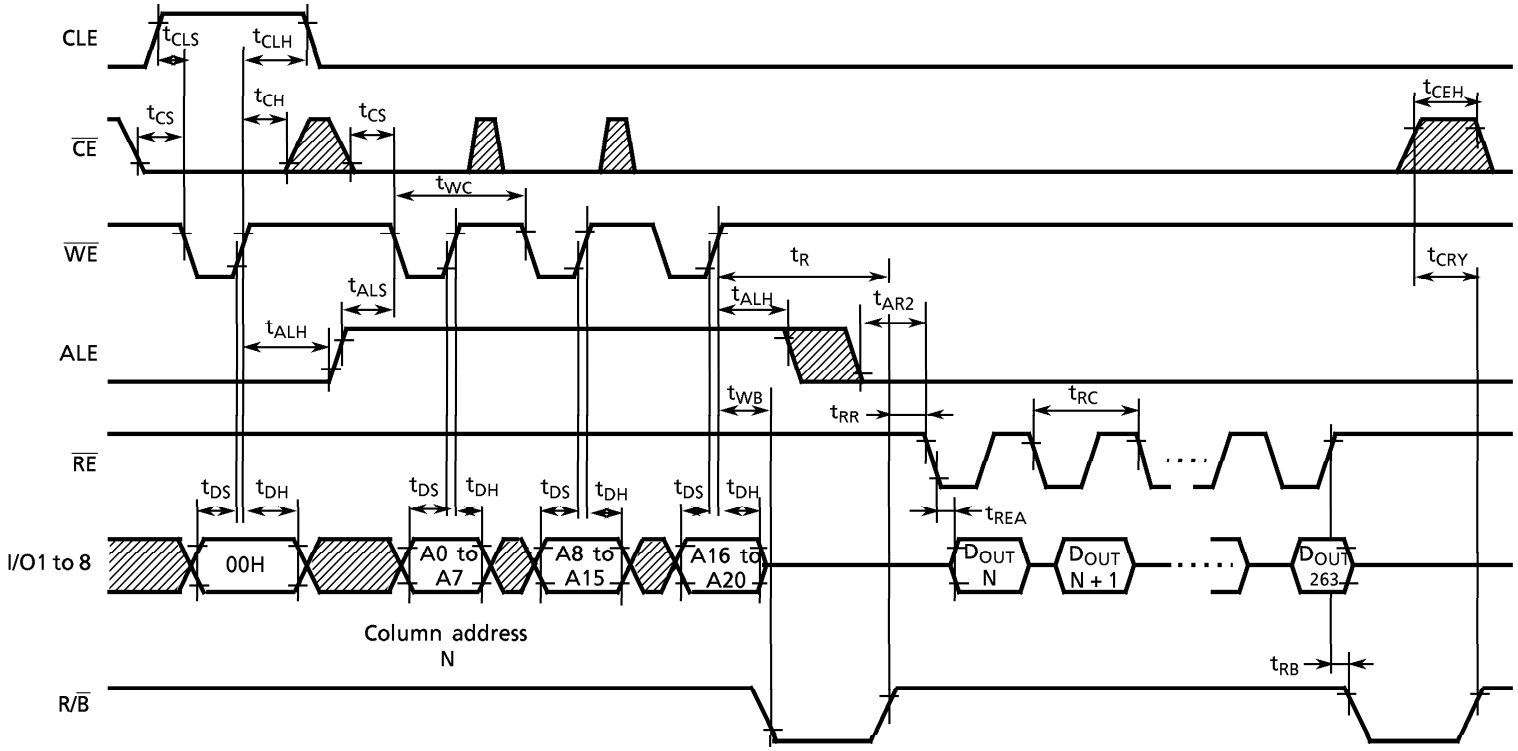
Serial Read Cycle Timing Diagram



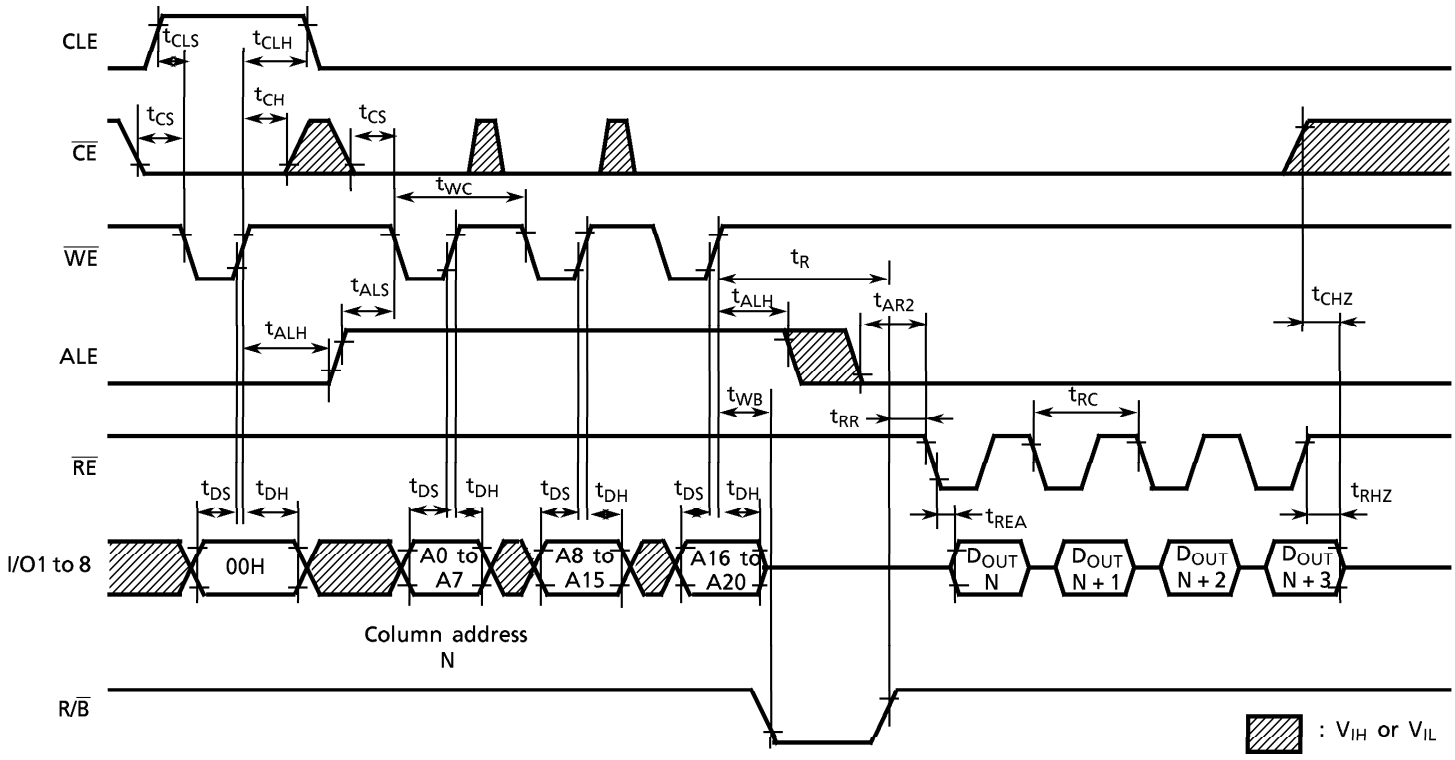

Status Read Cycle Timing Diagram



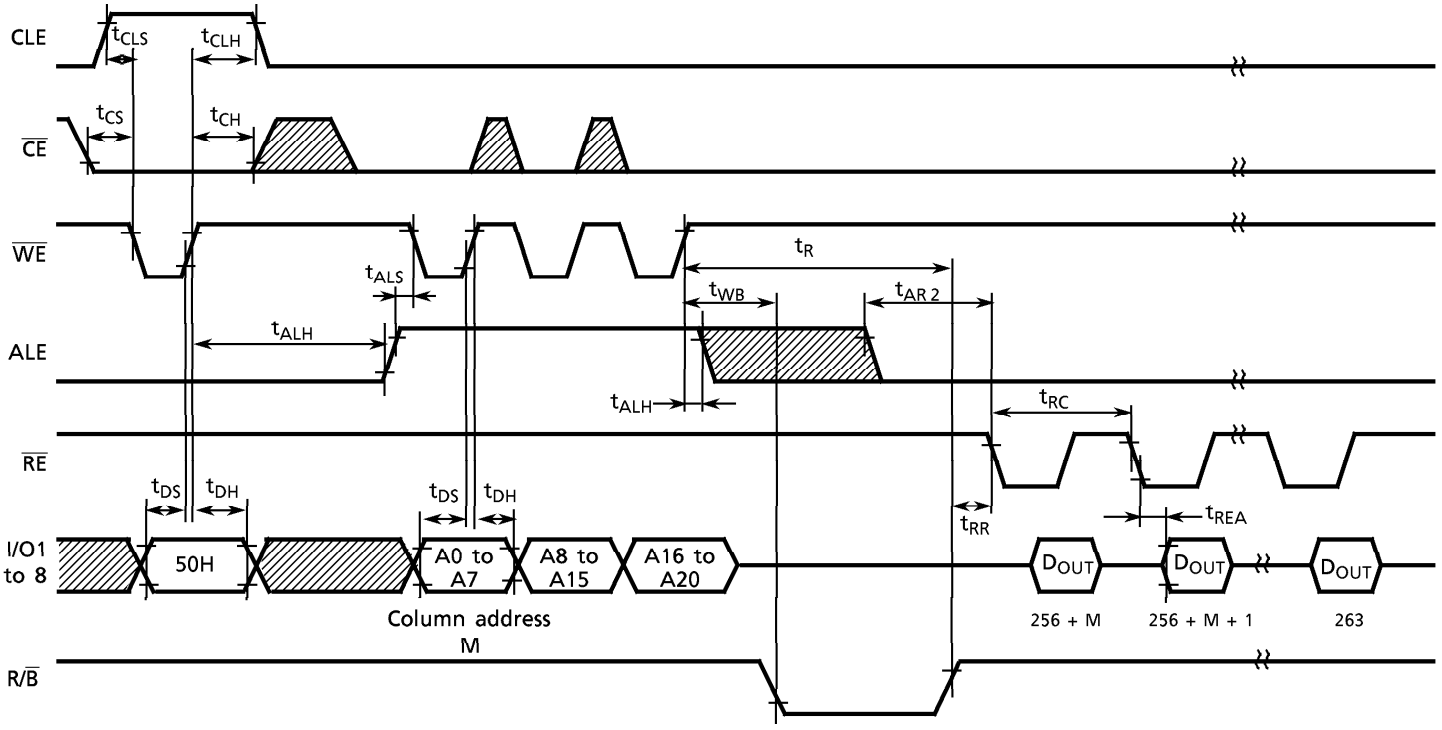
Read Cycle (1) Timing Diagram



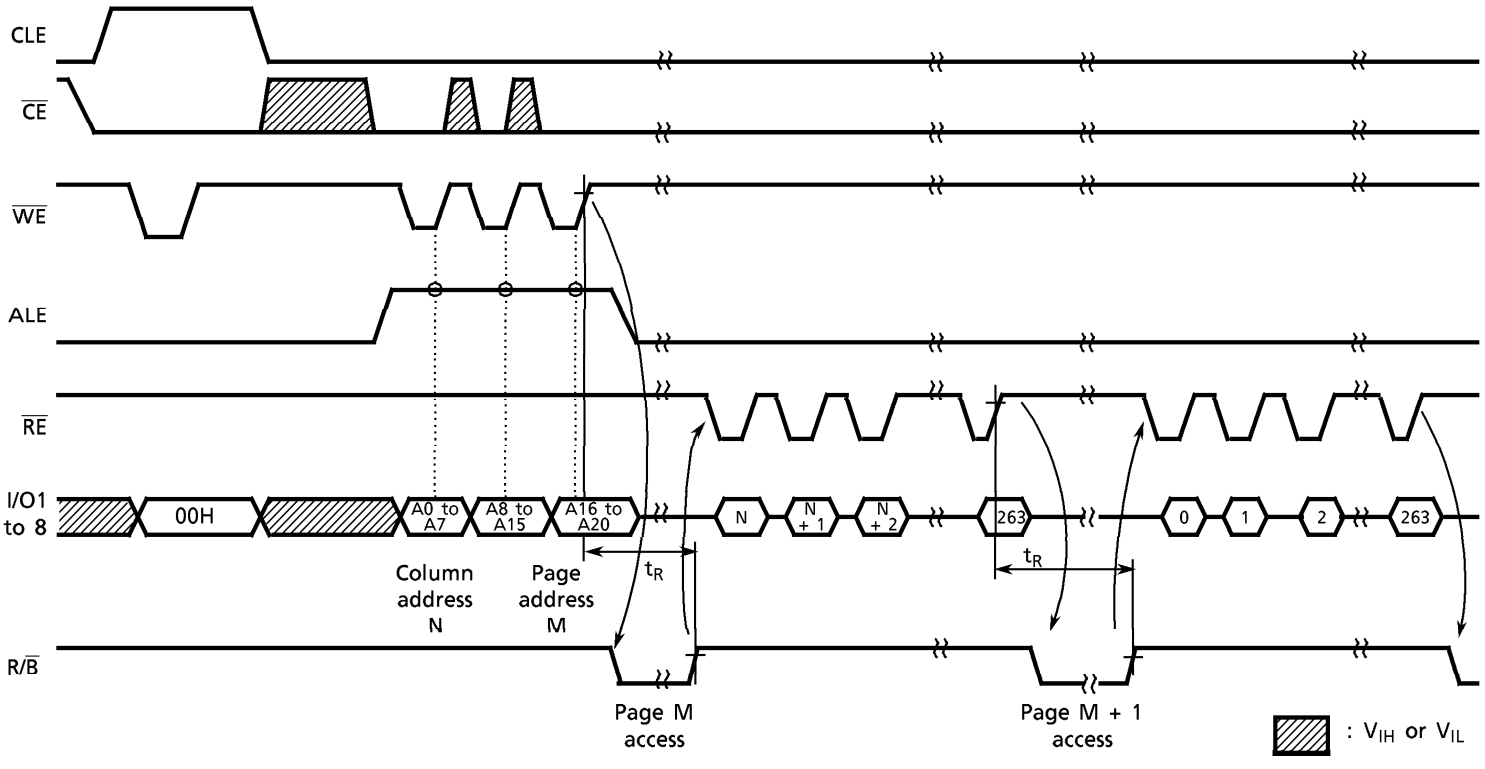

Read Cycle (1) Timing Diagram : Interrupted by $\overline{CE}$



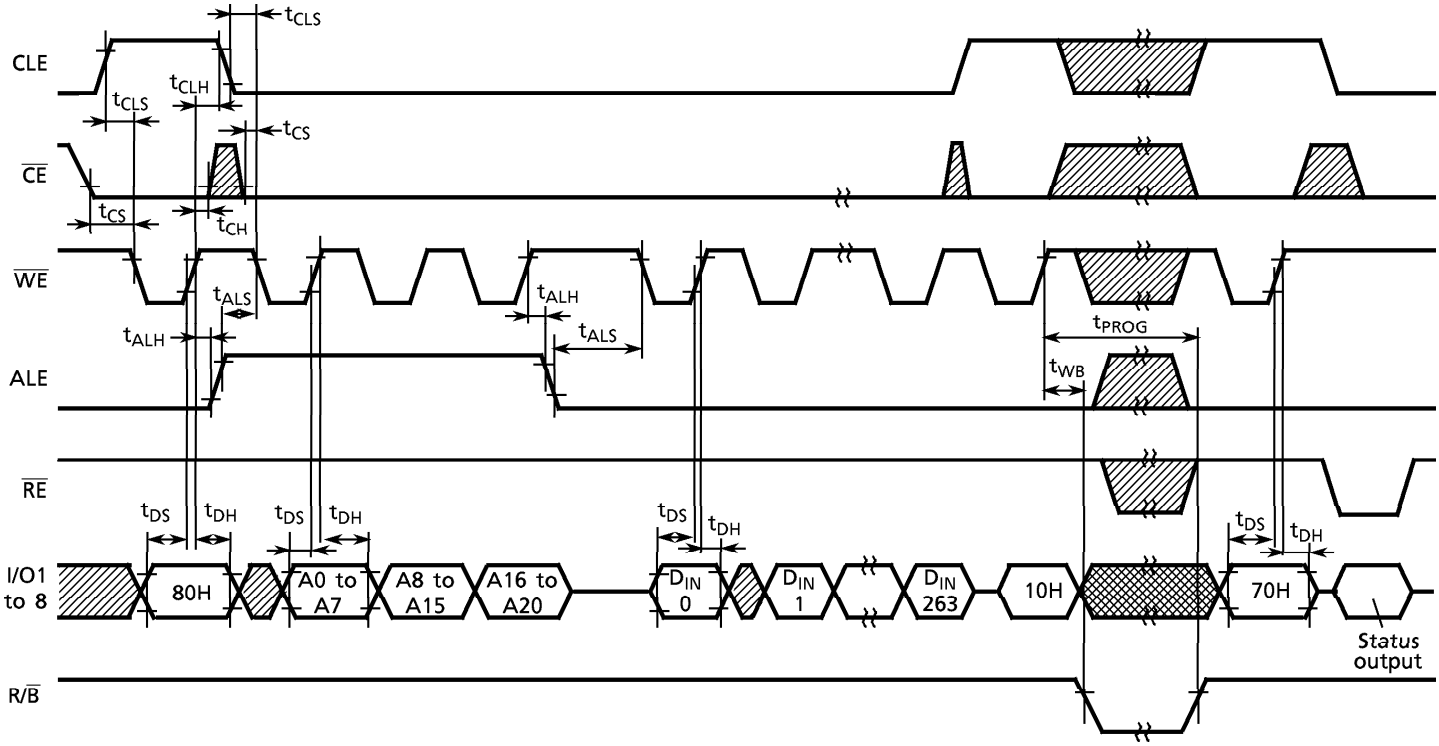
Read Cycle (2) Timing Diagram




Sequential Read Timing Diagram

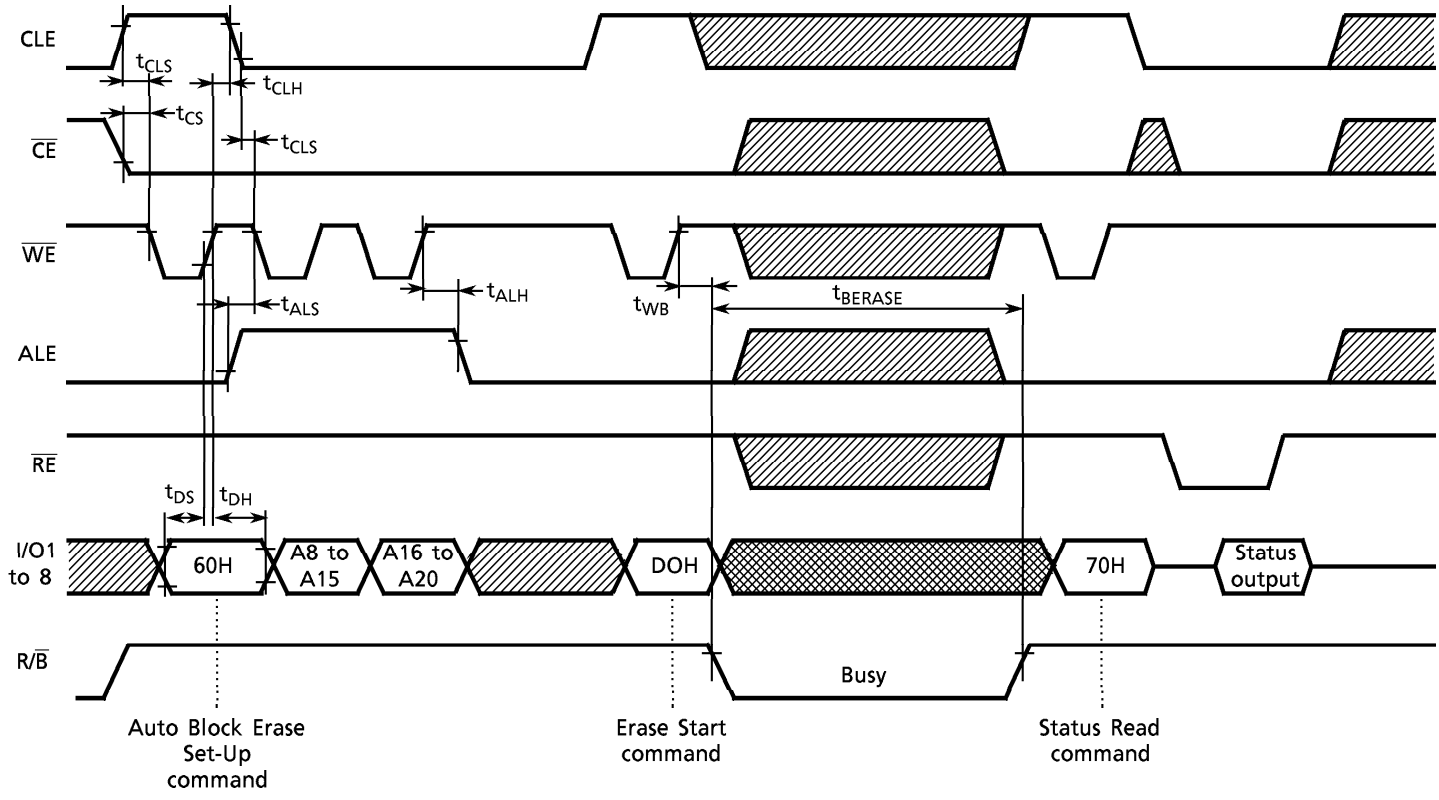


## Auto Program Operation Timing Diagram



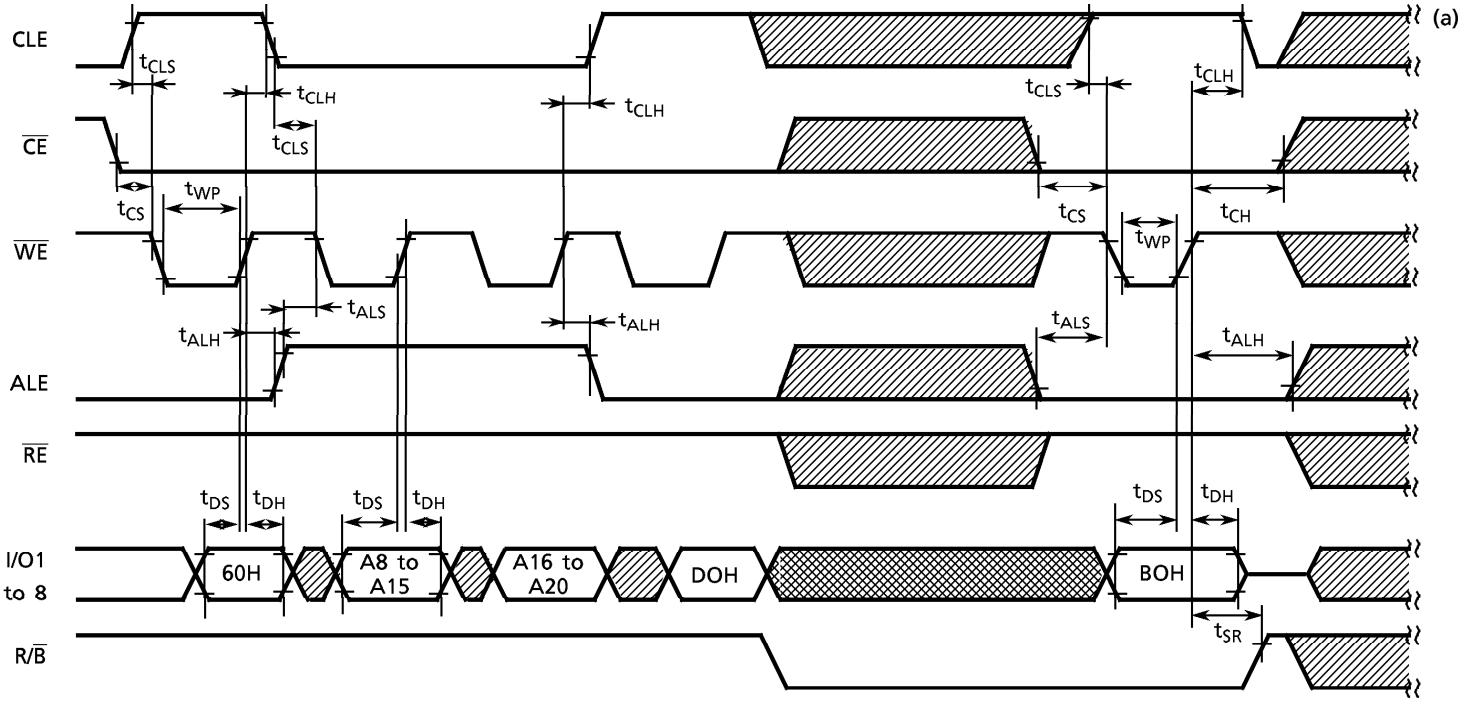

: $V_{IH}$ or $V_{IL}$ : If data is being output, do not allow any input.

## Auto Block Erase Timing Diagram

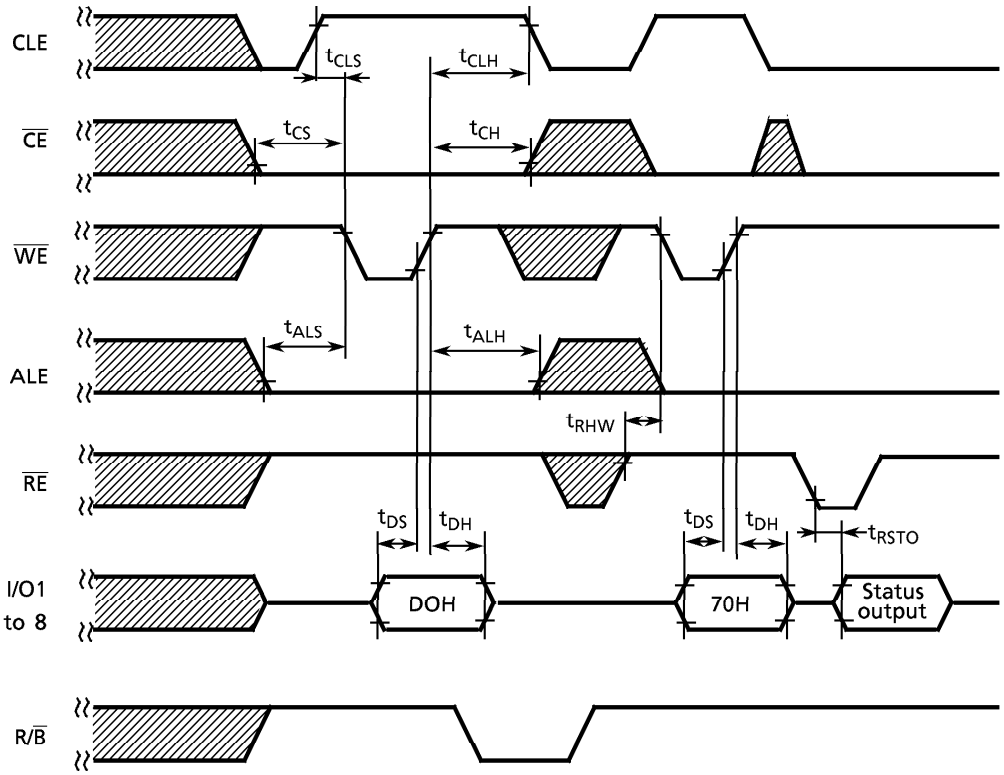



: $V_{IH}$ or $V_{IL}$ : If data is being output, do not allow any input.

Suspend/Resume on Block Erase Operation Timing Diagram




(a) :

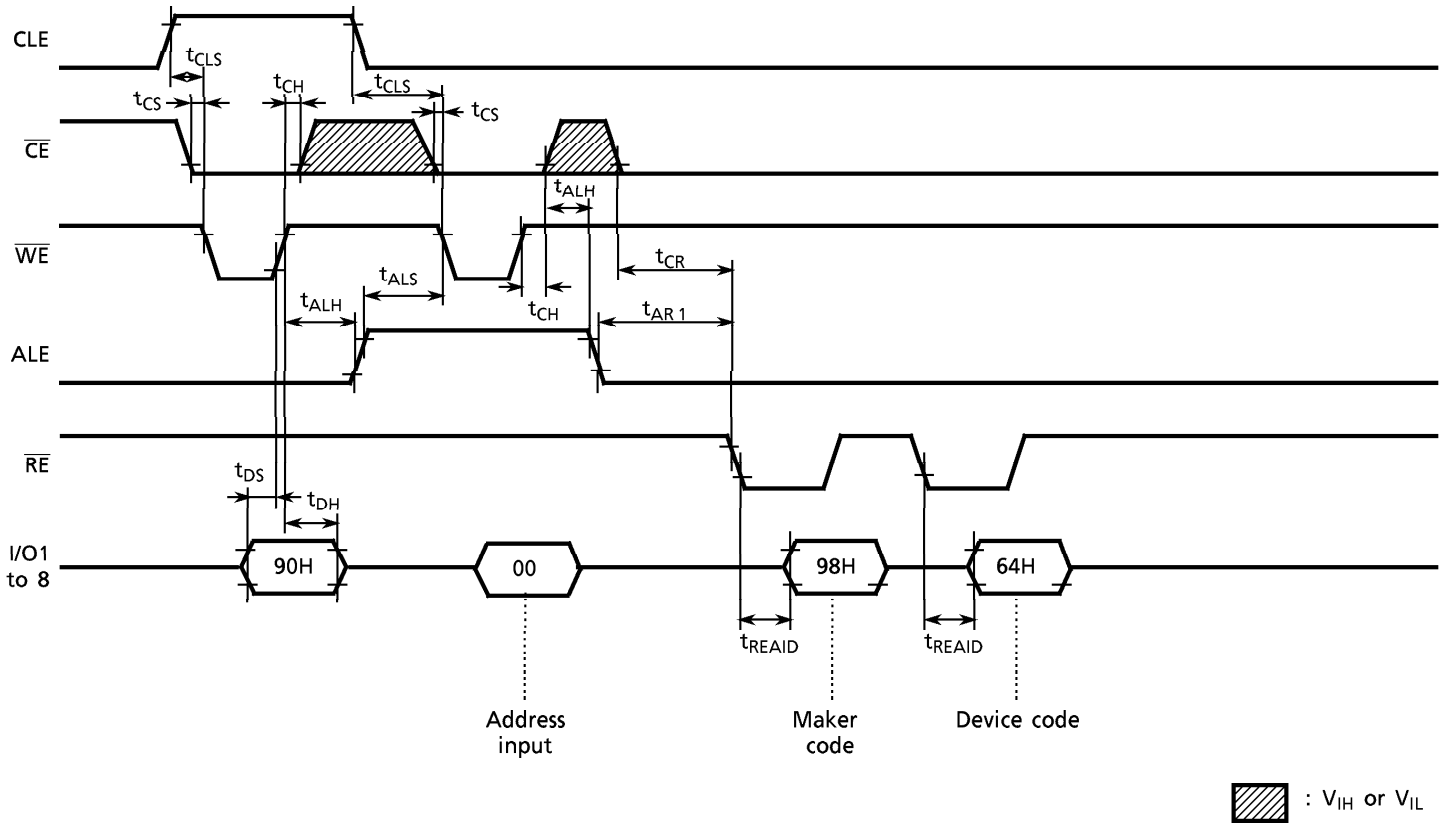



(a): Continued

: $V_{IH}$ or $V_{IL}$

: If data is being output, do not allow any input.

ID Read Operation Timing Diagram



## PIN FUNCTIONS

The TC5816 is a serial access memory which utilizes time-sharing input of address information. The device pin-outs are configured as shown in Figure 1.

Command Latch Enable: CLE (Figure 1. Pin No.2)

The CLE input signal is used to control the acquisition of the operation mode command into the internal command register. The command is latched into the command register from the I/O port on the rising edge of the $\overline{WE}$ signal while CLE is high.

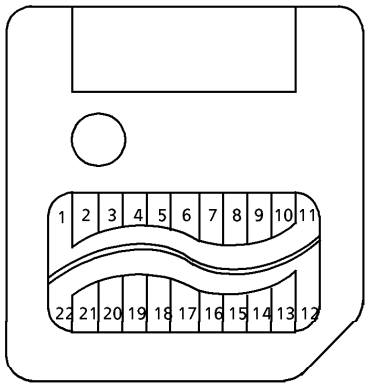



Figure 1. TC5816 Pinout

Address Latch Enable: ALE (Figure 1. Pin No.3)

The ALE signal is used to control the acquisition of either address information or input data into the internal address/data register.
Address information is latched on the rising edge of $\overline{WE}$ if ALE is high.
Input data is latched if ALE is low.

Chip Enable: $\overline{CE}$ (Figure 1. Pin No.21)

The device goes into a low power standby mode during a Read operation when $\overline{CE}$ goes high. The $\overline{CE}$ signal is ignored when the device is in the Busy state ($R/\overline{B}$ = L), such as during a Program or Erase operation, and will not go into Standby mode even if a $\overline{CE}$ high signal is input.

Write Enable: $\overline{WE}$ (Figure 1. Pin No.4)

The $\overline{WE}$ signal is used to control the acquisition of data from the I/O port.

Read Enable: $\overline{RE}$ (Figure 1. Pin No.20)

The $\overline{RE}$ signal controls serial data output. Data is available $t_{REA}$ after the falling edge of $\overline{RE}$.
The internal column address counter is also incremented (Address + 1) on this falling edge.

I/O Port: I/O 1 to 8 (Figure 1. Pin No.6 to 9, 13 to 16)

The I/O 1 to 8 pins are used as the port for transferring address, command and input/output data information to or from the device.

Write Protect: $\overline{WP}$ (Figure 1. Pin No.5)

The $\overline{WP}$ signal is used to protect the device from accidental programming or erasing. The internal voltage regulator is reset when $\overline{WP}$ is low. This signal is usually used for protecting the data during the power on/off sequence when input signals are invalid.

Ready/Busy: $R/\overline{B}$ (Figure 1. Pin No.19)

The $R/\overline{B}$ output signal is used to indicate the operating condition of the device. The $R/\overline{B}$ signal is in a busy state ($R/\overline{B}$ = L) during the Program, Erase and Read operations and will return to a ready state ($R/\overline{B}$ = H) afrer completion of the operation. The output buffer for this signal is an open drain.

Low Voltage Detect: LVD (Figure 1. Pin No.17)

The LVD is used to detect the proper supply voltage. By connecting this pin to $V_{SS}$ through a pull-down resistor, it is possible to distinguish 3.3 V product from 5 V product. When 3.3 V is applied as $V_{CC}$ to pins 12 and 22, a "H" level can be detected on the system side if the device is a 3.3 V product, and "L" level for a 5 V product.

Schematic Cell Layout and Address Assignment

The program operation is implemented in page units while the erase operation is carried out in block units.

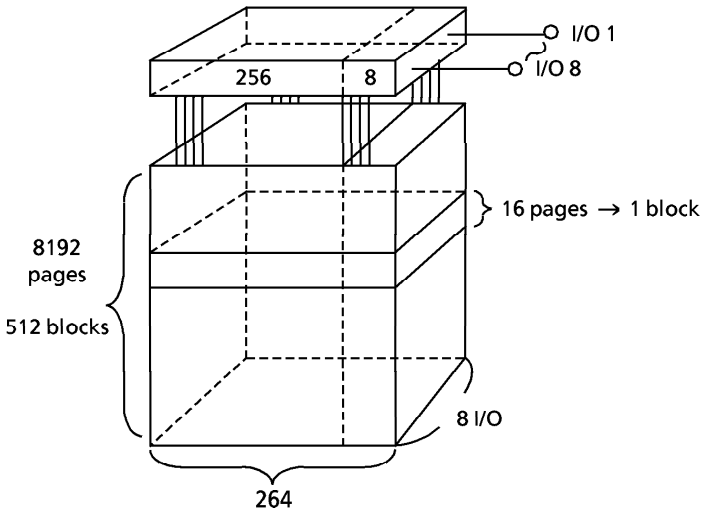



Figure 2. TC58V16 Schematic Cell Layout

A page consists of 264 bytes in which 256 bytes are for main memory and 8 bytes are for redundancy or other uses.

1 Page = 264 bytes
1 Block = 264 bytes × 16 pages = (4 K + 128) bytes
Total Device Density = 264 bytes × 16 pages × 512 blocks
= 16.5 Mbits (2.0625 Mbytes)

The address is acquired through the I/O port over three consecutive clock cycles as shown in Table 1.

Table 1. Addressing

| | I/O 1 | I/O 2 | I/O 3 | I/O 4 | I/O 5 | I/O 6 | I/O 7 | I/O 8 |
|---|---|---|---|---|---|---|---|---|
| First cycle | A0 | A1 | A2 | A3 | A4 | A5 | A6 | A7 |
| Second cycle | A8 | A9 | A10 | A11 | A12 | A13 | A14 | A15 |
| Third cycle | A16 | A17 | A18 | A19 | A20 | * L | * L | * L |

A0 to A7 : column address
A8 to A20 : page address
( A12 to A20: block address
A8 to A11 : NAND address in block )

*: I/O 6 to 8 must be set low in the third cycle.

Operation Mode: Logic and Command Tables

The operation modes such as Program, Erase, Read, Erase Suspend and Reset are controlled by the eleven different command operations shown in Table 2. The address, command input and data input/output are controlled by the CLE, ALE, $\overline{CE}$, $\overline{WE}$, $\overline{RE}$ and $\overline{WP}$ signals, as shown in Table 2.

Table 2. Logic Table

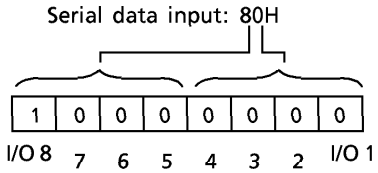
| | CLE | ALE | $\overline{CE}$ | $\overline{WE}$ | $\overline{RE}$ | $\overline{WP}$ |
|---|---|---|---|---|---|---|
| Command Input | H | L | L | ⌐└↗ | H | * |
| Data Input | L | L | L | ⌐└↗ | H | * |
| Address Input | L | H | L | ⌐└↗ | H | * |
| Serial Data Output | L | L | L | H | ↘⌐ | * |
| During Programming (Busy) | * | * | * | * | * | H |
| During Erasing (Busy) | * | * | * | * | * | H |
| Program, Erase Inhibit | * | * | * | * | * | L |

H: $V_{IH}$, L: $V_{IL}$, *: $V_{IH}$ or $V_{IL}$

Table 3. Command table (HEX data)

| | FIRST CYCLE | SECOND CYCLE | ACCEPTABLE COMMAND WHILE BUSY |
|---|---|---|---|
| Serial Data Input | 80 | – | |
| Read Mode (1) | 00 | – | |
| Read Mode (2) | 50 | – | |
| Reset | FF | – | ○ |
| Auto Program | 10 | – | |
| Auto Block Erase | 60 | D0 | |
| Suspend in Erasing | B0 | – | ○ |
| Resume | D0 | – | |
| Status Read | 70 | – | ○ |
| ID Read | 90 | – | |

Bit assignment of HEX data (Example)




Once the device is set into Read mode by the "00H" or "50H" command, additional Read commands are not needed for sequential page read operations. Table 4 shows the operation states for Read Mode.

Table 4. Read mode operation states

| | CLE | ALE | $\overline{CE}$ | $\overline{WE}$ | $\overline{RE}$ | I/O 1 to I/O 8 | POWER |
|---|---|---|---|---|---|---|---|
| Output Select | L | L | L | H | L | Data output | Active |
| Output Deselect | L | L | L | H | H | High impedance | Active |
| Standby | L | L | H | H | * | High impedance | Standby |

## DEVICE OPERATION

### Read Mode (1)

Read mode (1) is set by issuing a "00H" command to the command register. Refer to Figure 3 below for timing details and a block diagram.

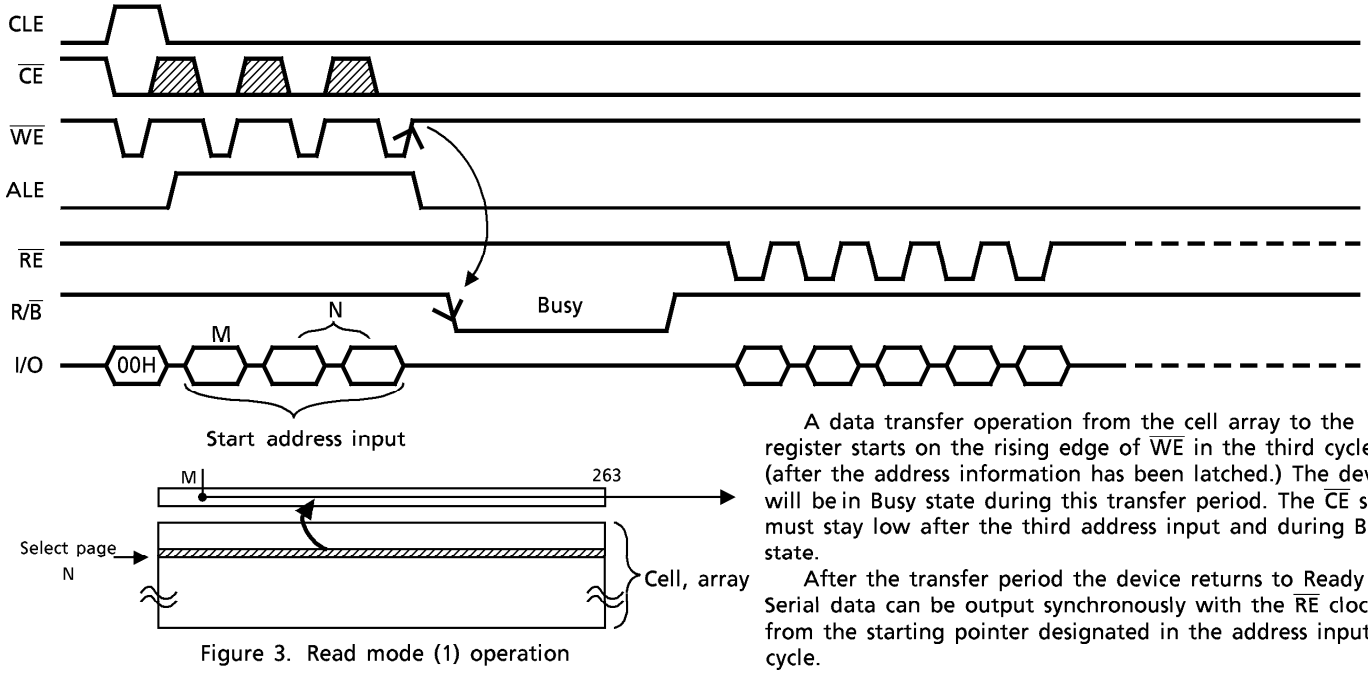



Figure 3. Read mode (1) operation

A data transfer operation from the cell array to the register starts on the rising edge of $\overline{WE}$ in the third cycle (after the address information has been latched.) The device will be in Busy state during this transfer period. The $\overline{CE}$ signal must stay low after the third address input and during Busy state.

After the transfer period the device returns to Ready state. Serial data can be output synchronously with the $\overline{RE}$ clock from the starting pointer designated in the address input cycle.

Read Mode (2)

Read mode (2) has the same timing as Read mode (1) but is used to access information in the extra 8-byte redundancy area of the page. The starting pointer is therefore assigned between bytes 256 and 263.

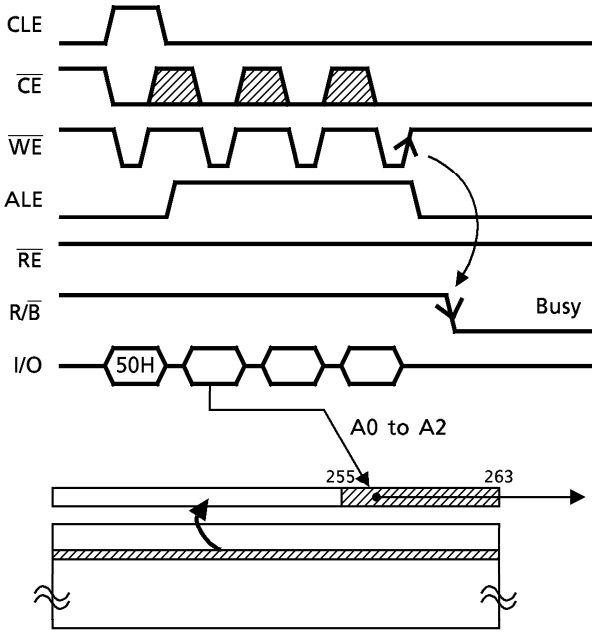



Figure 4. Output Select (2) operation

Addresses A0 to A2 are used to set the starting pointer for the redundant memory cell, while A3 to A7 are ignored. Once the "50H" command is set, the pointer moves to the redundant cell locations and only those 8 cells can be addressed, regardless of the A3 to A7 address. (The "00H" command is necessary to move the pointer back to the 0 to 255 the main memory cell locations.)

Sequential Read (1) (2)

This mode allows sequential reading without the additional address input.

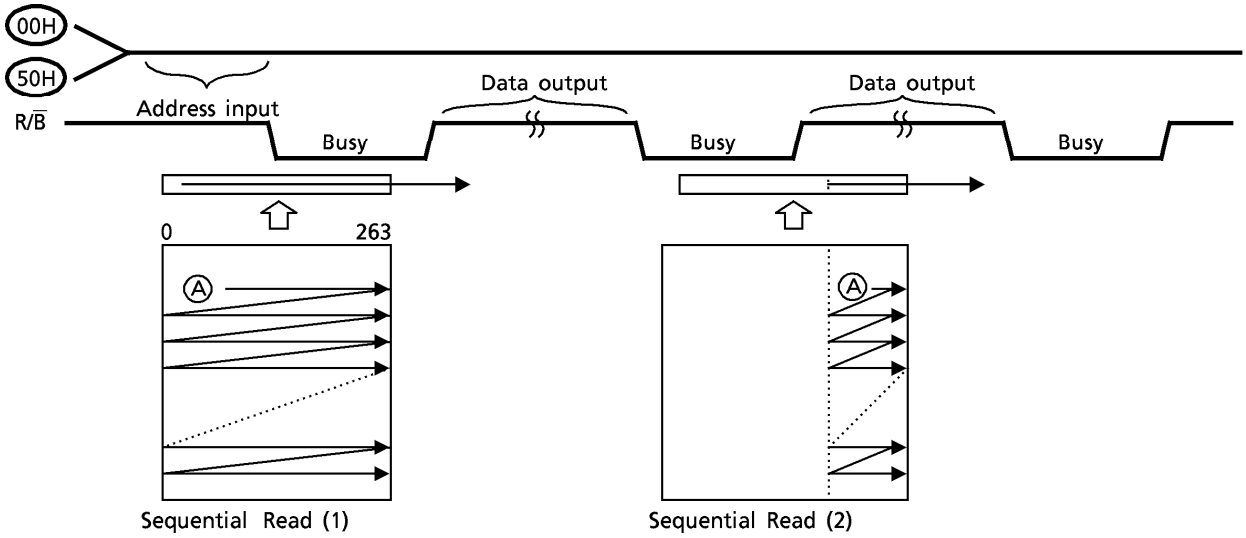



Figure 5. Sequential Read operation

Sequential Read mode (1) outputs addresses 0 to 263 while Sequential Read mode (2) outputs the redundant address locations only. When the pointer reaches the last address, the device continues to output the last data from this address on each $\overline{RE}$ clock signal.

Status Read

The TC5816 automatically implements the execution and verification of the Program and Erase operations. The Status Read function is used to monitor the Ready/Busy status of the device, determine the pass/fail result of a Program or Erase operation, and determine if the device is in Suspend or Protect mode. The device status is output through the I/O port using the $\overline{RE}$ clock after a "70H" command input. The resulting information is outlined in Table 5.

Table 5. Status output table

| | STATUS | OUTPUT | |
|---|---|---|---|
| I/O 1 | Pass/Fail | Pass: "0" | Fail: "1" |
| I/O 2 | Not used | "0" | |
| I/O 3 | Not used | "0" | |
| I/O 4 | Not used | "0" | |
| I/O 5 | Not used | "0" | |
| I/O 6 | Suspend | Suspended: "1" | Not Suspended: "0" |
| I/O 7 | Ready/Busy | Ready: "1" | Busy: "0" |
| I/O 8 | Write Protect | Protect: "0" | Not Protect: "1" |

The Pass / Fail status on I/O 1 is only valid when the device is in the Ready state.

The device will always indicate Fail Status while in the Busy state in the Program and Erase operations.

An application example with multiple devices is shown in Figure 6.

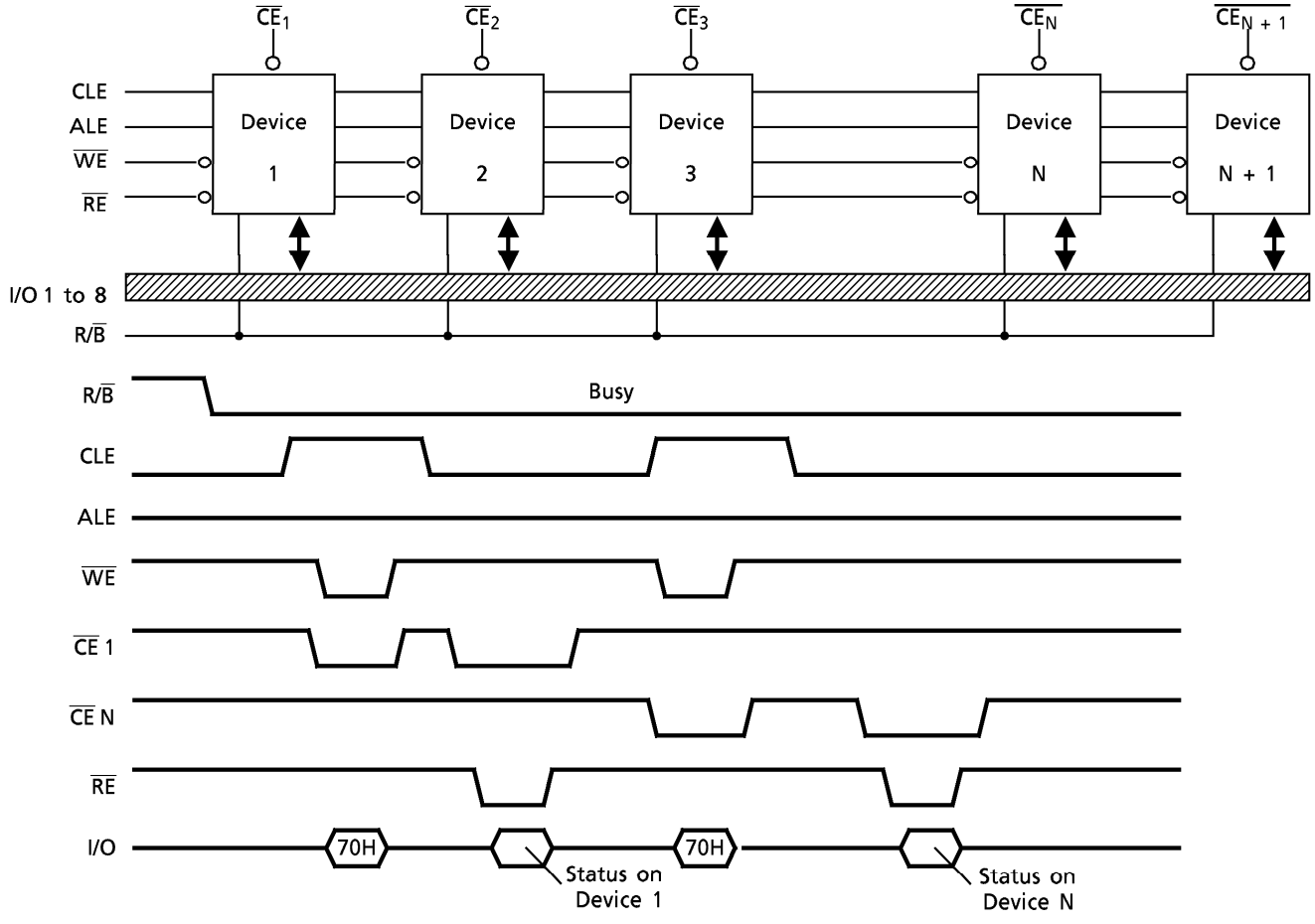
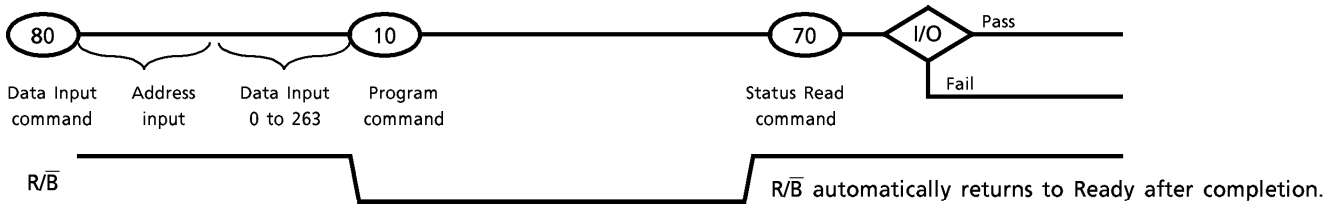



Figure 6. Status Read Timing Application Example

SYSTEM DESIGN NOTE: If the R/$\overline{B}$ pin signals of multiple devices are common-wired, as shown in the diagram, the Status Read Function can be used to determine the status of each individually selected device.

## Auto Page Program

The TC5816 implements the Automatic Page Program operation by receiving a "10H" program command after the address and data have been input. The sequence of command, address and data input is shown below. (Refer to the detailed timing chart.)



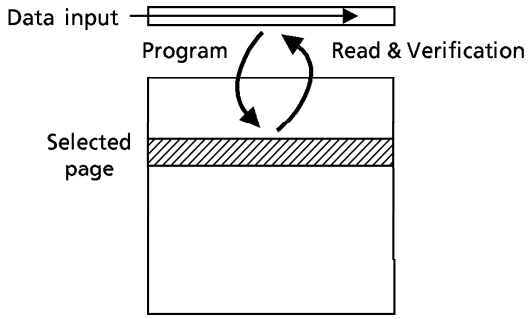




Figure 7. Auto Page Program Operation

The data is transferred (programmed) from the register to the selected page on the rising edge of WE following the "10H" command input. After programming the programmed data is transferred back to the register to be automatically verified by the device. If the program does not succeed, the above Program/Verify operation is repeated by the device until success is achieved or until the maximum loop number set in the device is reached.

## Auto Block Erase

The Auto Block Erase operation starts on the rising edge of $\overline{WE}$ after the Erase start command "D0H" which follows the Erase Set-Up command "60H". This two-cycle process for Erase operations acts as an extra layer of protection from accidental erasure of data due to external noise. The device automatically executes the Erase and Verify operations.

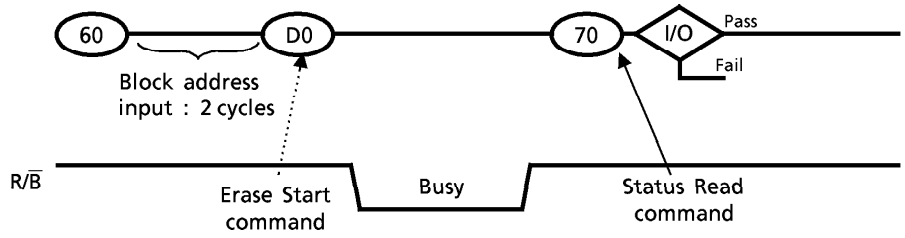



Figure 8. Auto Block Erase

Suspend / Resume

Because a Block Erase operation can keep the device in the Busy state for an extended period of time, the TC5816 has the ability to suspend the Erase operation in order to allow Program or Read operations to be performed on the device. The block diagram and command sequence for this operation are shown as below. (Refer to the detailed timing chart)

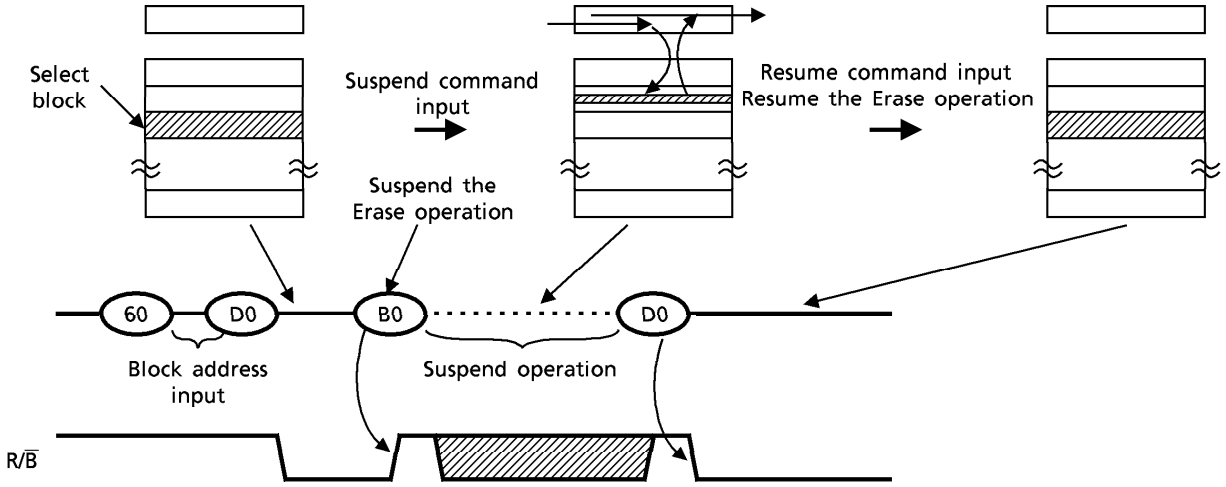



Figure 9. Suspend/Resume Operation

The B0 ····· D0 Suspend/Resume cycle can be repeated up to 20 times during a Block Erase operation. After the Resume command has been input, the Erase operation continues from the point at which it left off and does not have to be restarted.

Reset

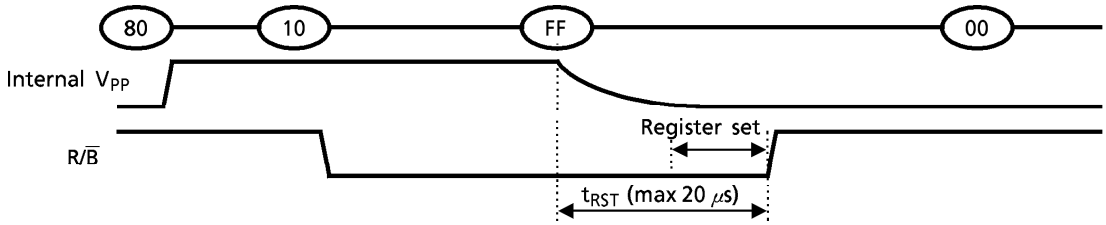
The Reset mode stops all operations. For example, in the case of a Program or Erase operation, the regulated voltage is discharged to 0 volts and the device will go into Wait state.
The address and data register are set as follows after a Reset:

- Address Register : All "0"
- Data Register : All "1"
- Operation Mode : Wait State

The response after an "FFH" Reset command input during each operation is as follows:

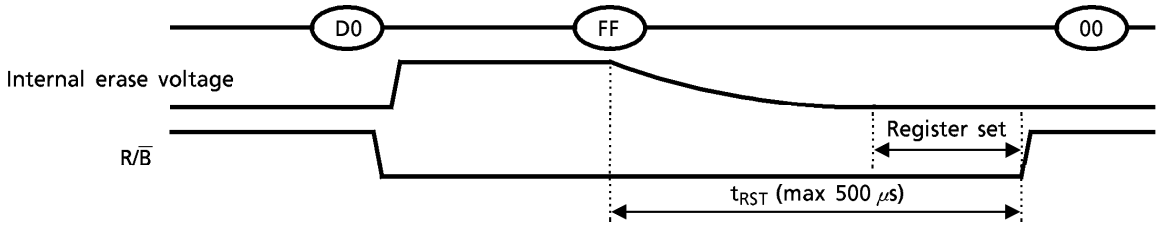
- When a Reset (FFH) command is input during programming.

Figure 10.



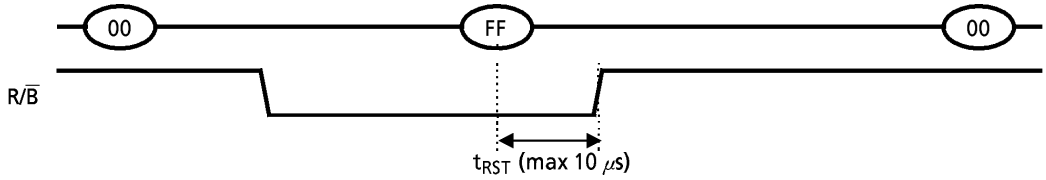

- When a Reset (FFH) command is input during erasing.

Figure 11.



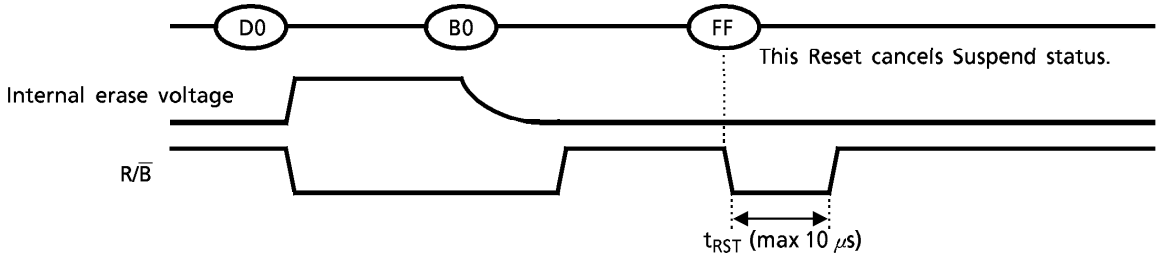

- When a Reset (FFH) command is input during a Read operation.

Figure 12.

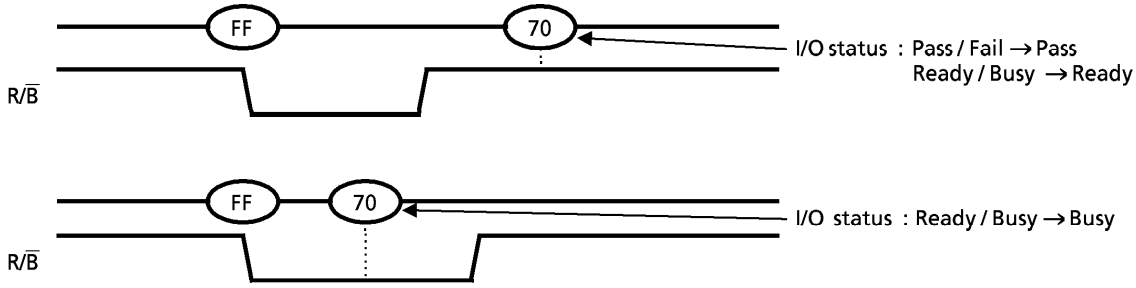



- When a Reset (FFH) command is input after Suspend.

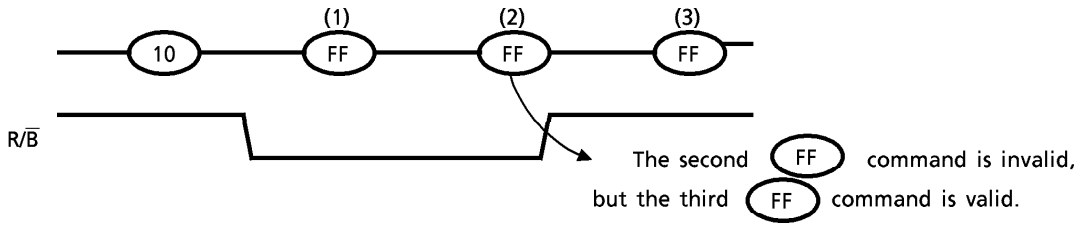
Figure 13.



· When a Status Read command (70H) is input after a Reset. Figure 14.




· When more than one Reset commands are input in succession. Figure 15.




## ID READ

The TC5816 contains an ID code to identify the device type and the manufacturer. The ID codes are read out using the following timing conditions:

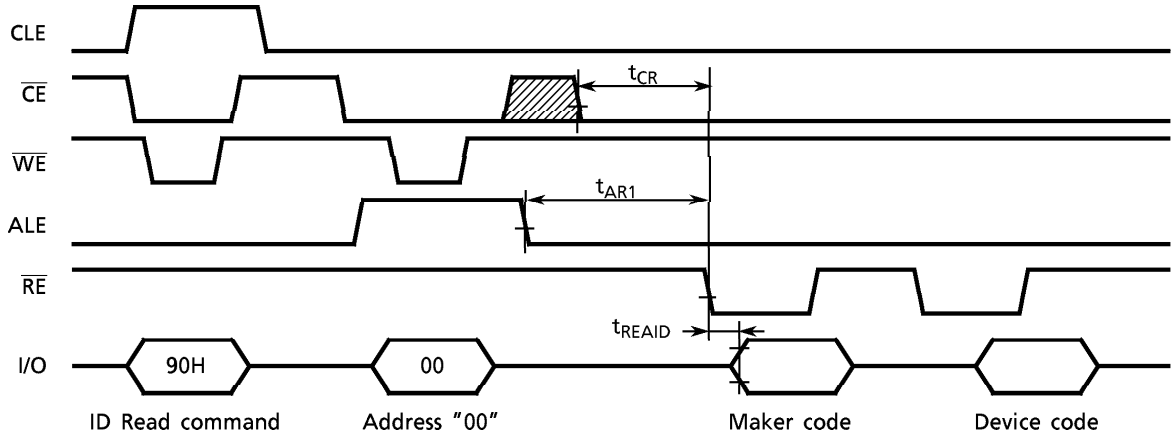



Figure 16. ID Read timing

Table 6. Code table

| | I/O 8 | I/O 7 | I/O 6 | I/O 5 | I/O 4 | I/O 3 | I/O 2 | I/O 1 | HEX DATA |
|---|---|---|---|---|---|---|---|---|---|
| Maker code | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 98H |
| Device code | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 64H |

Refer to the specifications for the $t_{REAID}$, $t_{CR}$ and $t_{AR1}$ access timings.

## DEVICE PHYSICS:

### Program Operation

Figure 17 shows the NAND memory cell level details of the programming mechanism. The Program operation is used to write "0" data into an erased memory cell ("1" data cell) using a tunneling mechanism. An example Program operation to program "0" data into TR1 and "1" data into TR2 is as follows:

(1) A high level is applied to Select line 1 and a low level is applied to Select line 2 so that the device is connected to the Bit line and disconnected from the ground line.

(2) Vpp (≈ 20 V) is applied to the selected word line and an inhibit voltage of VPI (≈ 10 V) is applied to the unselected word lines.

(3) 0 volts is applied to the bit line tied to cell transistor TR1 and the inhibit voltage VDPI (≈ 10 V) is applied to the bit line tied to TR2.

(4) Vpp is applied between the control gate and the channel in TR1, as shown in Figure 18, which causes electrons to be injected from the channel to the floating gate by a tunneling mechanism.

(5) The injected electrons are captured in the floating gate surrounded by an oxide layer and will remain, even after power is cut off, until they are removed by an Erase operation.

(6) Although 20 volts is applied to the control gate of TR2, the voltage difference between the control gate and the channel is only 10 V because the voltage of the channel is 10 V. Therefore, tunneling does not take place (i.e. the electron is not injected into the floating gate.)

(7) Tunneling does not take place in the unselected pages because of the 10 V (VPI) applied to the unselected word lines which makes the voltage difference between the control gate and channel only 10 volts.

Thus the floating gate of the "0" cell is charged to "Minus" and that of the "1" cell is charged to "Plus".

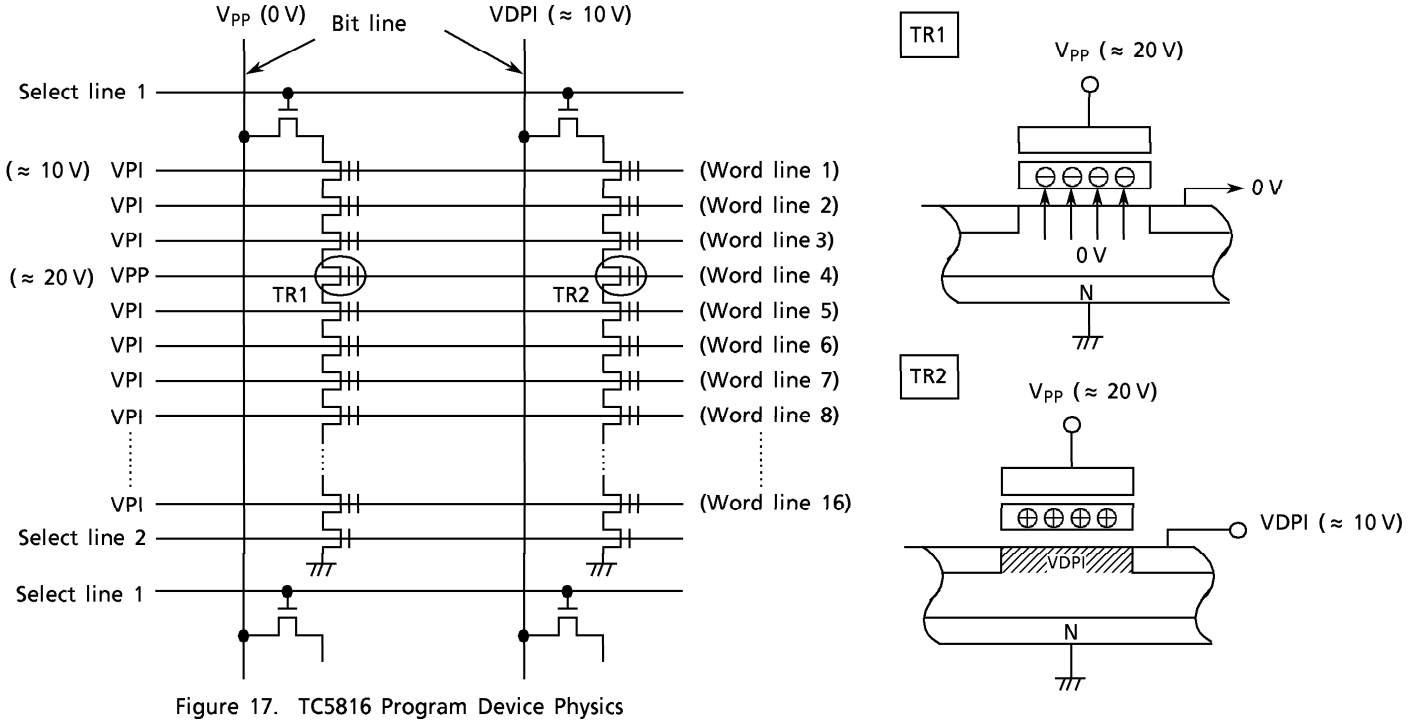



Figure 17. TC5816 Program Device Physics

Erase Operation

Figure 18 shows the NAND memory cell level details of the Erase mechanism. The Erase operation is used to turn the "0" (programmed) cells back to "1" in a block. The captured electrons are pulled out from the floating gate to the substrate by a tunneling mechanism.
0 volts is applied to the control gate and Vpp (≈ 20 V) is applied to the substrate so that a 20-volt potential is created and the electrons in the floating gate are pulled out by the tunneling mechanism.

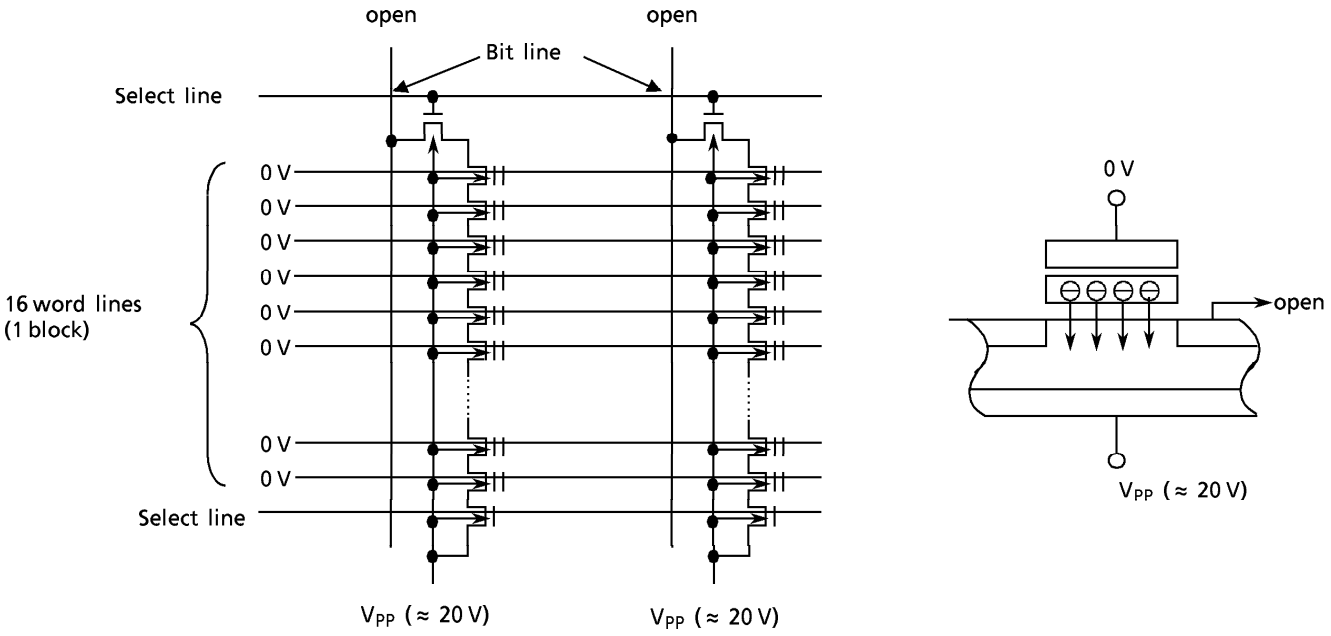



Figure 18. TC5816 Erase Device Physics

Read Operation

After programming the state of the memory cell is either "0" (minus charge on the floating gate) or "1" (plus charge on the floating gate). Each state is indicated as the "threshold voltage (Vth)" which is a characterization parameter of the MOS transistor as shown in Figure 19. The threshold voltage of a transistor with data "0" is distributed in the "plus" region while a transistor with data "1" is distributed in the "minus" region. The distribution band depends on the fluctuation of the transistor.

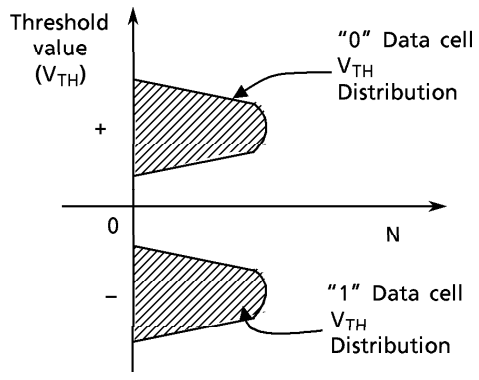



Figure 19. $V_{TH}$ Distribution for "0" and "1" data cells

Figure 20 shows memory cell level details of the Read operation mechanism:

(1) A high voltage is applied to Select lines 1 and 2 in the block which includes the selected page, so that the 16 NAND memory cells are connected to the Bit line and ground.

(2) 0 volts is applied to the control gates of the selected page and a high level voltage is applied to the control gates of the unselected pages.

(3) In Figure 20, transistor TR2 with data "1" turns on, transistor TR1 with data "0" turns off, and all other unselected transistors turn on.

(4) The precharged bit line tied to TR2 is discharged through TR2 as cell current flows to ground, while the precharged bit line tied to TR1 remains high because current does not flow. The sense amplifiers tied to the bit lines thus sense the voltage levels as "1" and "0" respectively.

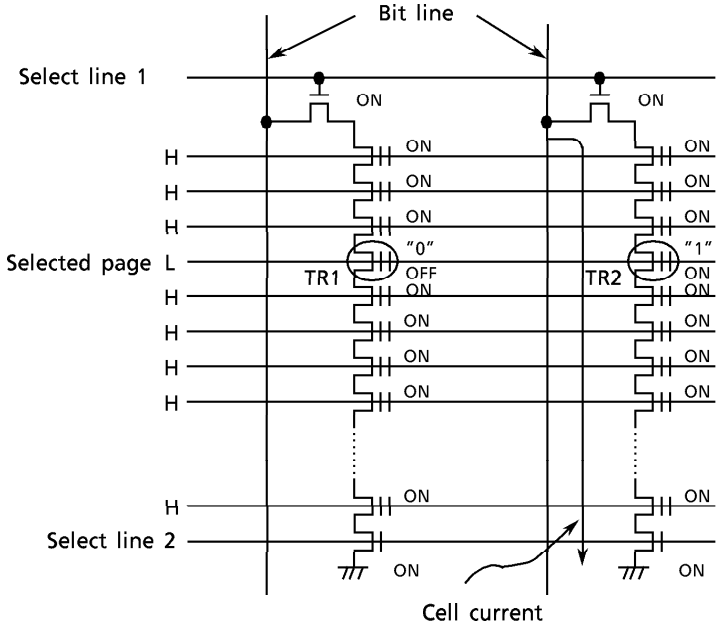



Figure 20. TC5816 Read Device Physics

## APPLICATION NOTES AND COMMENTS

(1) Prohibition of unspecified commands

The operation commands are listed in Table 3. Data input as a command other than the specified commands in Table 3 is prohibited. Stored data may be corrupted if an unspecified command is entered during the command cycle.

(2) Pointer control for "00H", "50H"

The TC5816 has two Read modes to set the destination of the pointer in either the main memory area of a page or the redundancy area. The pointer can be designated at any location from 0 to 255 in Read mode (1) and from 256 to 263 in Read mode (2). Figure 21 shows a block diagram of the modes' operations.

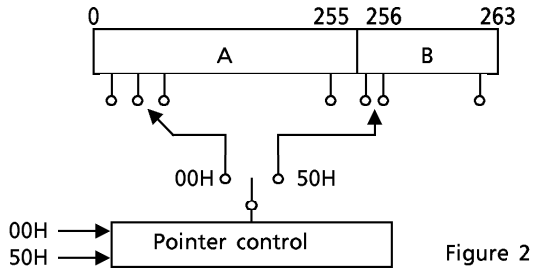



Figure 21. Pointer control

The pointer is set to region "A" by the "00H" command and to region "B" by the "50H" command.

(Example)

The "00H" command needs to be input to set the pointer back to region "A" when the pointer is in region "B".

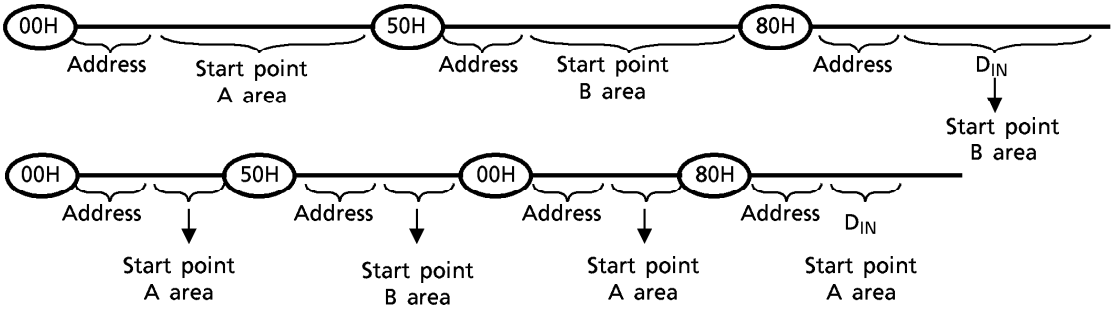
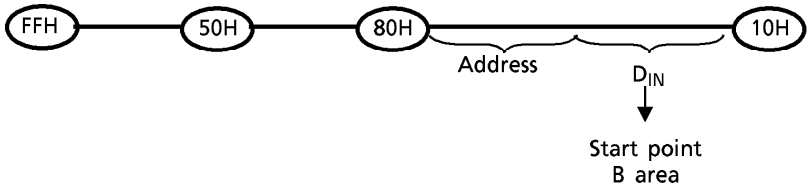



Figure 22. Example for Pointer Set

If the start point is set in region "B" using the "50H" command, so as to program region "B" only, the contents of the data resister must be set to "1" in advance using the "FFH" command.



(3) Acceptable commands after Serial Input command "80H"

Once the Serial Input command ("80H") has been input, do not input any command other than the Program Execution command ("10H") or the Reset command ("FFH") during programming.

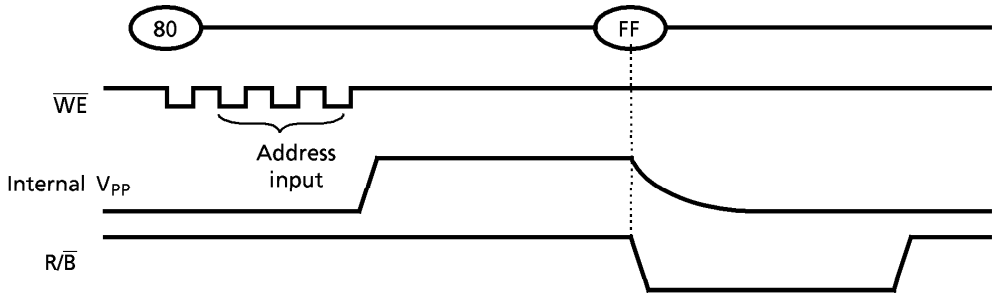
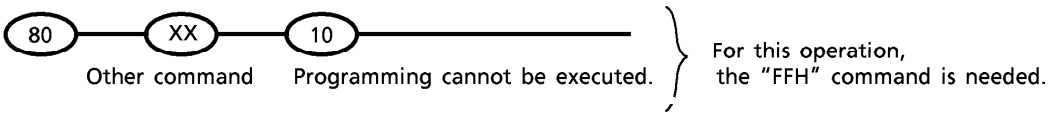



Figure 23.

If a command other than "10H" or "FFH" is input, the Program operation is not performed.




(4) Status Read during a Read operation

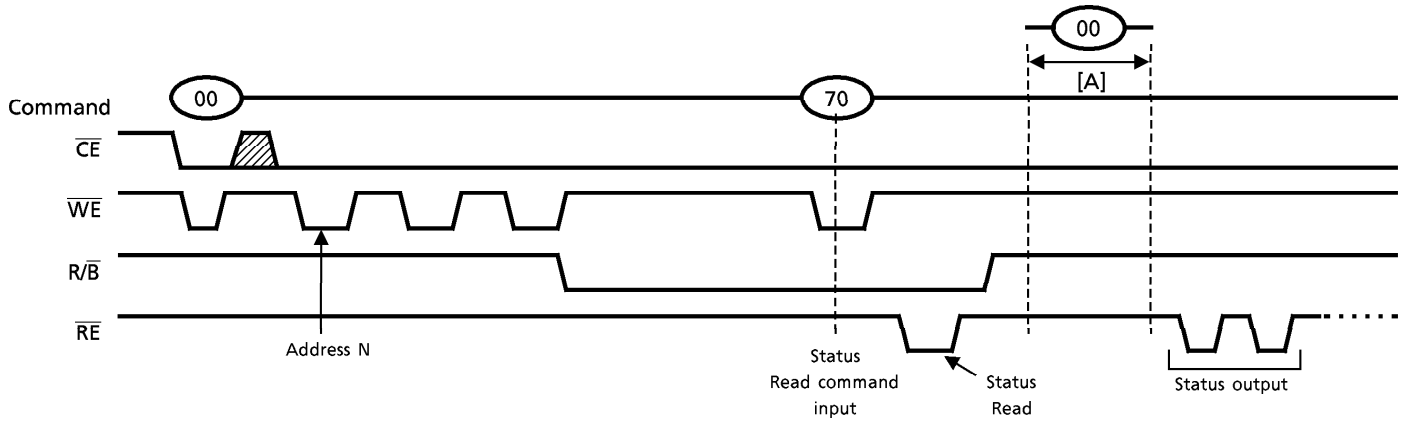



Figure 24.

The device status can be read out by inputting the Status Read command "70H" in Read mode. Once the device has been set to Status Read mode by a "70H" command, the device will not return to Read mode.

Therefore, Status Read during a Read operation is prohibited.

However, when the Read command "00H" is input during [A], Status mode is reset and then the device returns to Read mode. In this case, data output starts from address N without the need for address input.

(5) Suspend command "B0H"

The following issues need to be observed when the device is interrupted by a "B0H" command during block erasing.

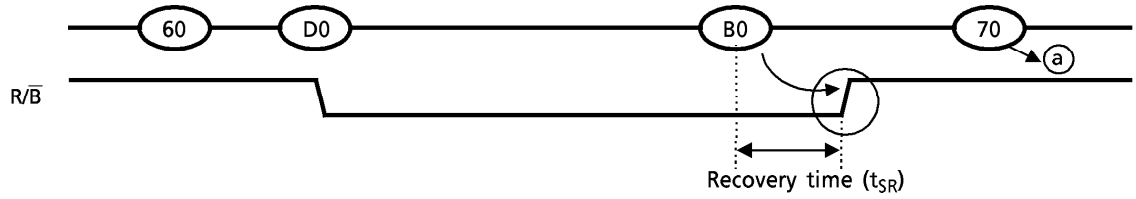



Figure 25.

The device status changes from Busy to Ready when "B0H" is input. However, the following two cases cannot be distinguished from one another.

- After a "B0H" command input, Busy → Ready
- After an Erase operation is completed with a "D0H" command, Busy → Ready

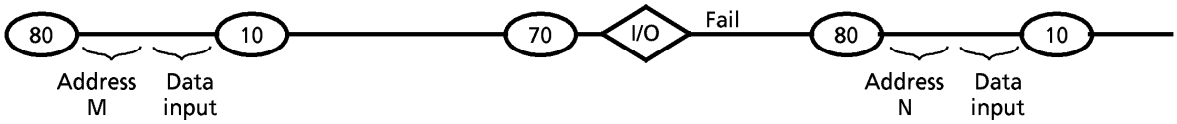
Therefore, the device status needs to be checked to see whether or not the "B0H" command has been accepted by issuing a "70H" command after the device goes to Ready.

The device responds as follows when a "D0H" command (Resume) is input instead of "70H".

- "B0H" has been accepted
  : Erase operation is executed. (The device is Busy.)
- "B0H" has not been accepted. (Erase operation has been completed)
  : "D0H" command cannot be accepted. (The device is Ready.)

The two cases above can be checked by monitoring the R/$\overline{B}$ signal.

(6) When auto programming fails.



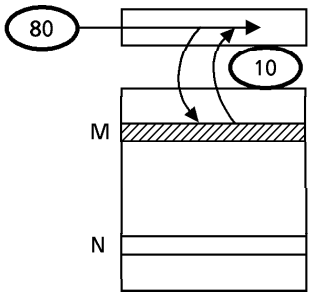




Figure 26.

If the programming result for page address M is "Fail", do not try to program the page to address N in another block. Because the previous input data is lost, the same sequence of "80H" command, address and data input is necessary.

(7) Data transfer

The data in page address M cannot be automatically tranferred to page address N. If the following sequence is executed, the data will be inverted. (i.e. "1" data will become "0" and "0" will become "1".)

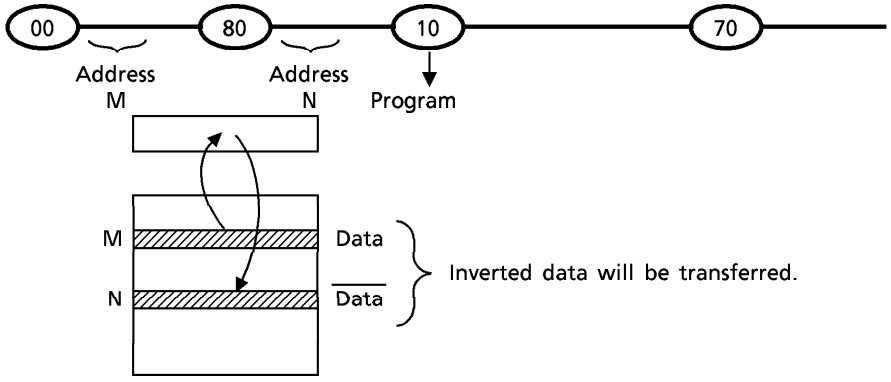
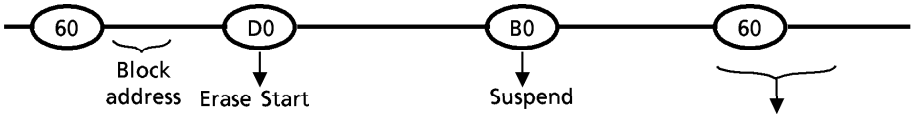



Figure 27.

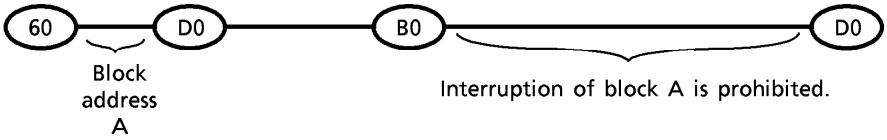
(8) Block Erase After Suspend command "B0H"




A Block Erase command is prohibited when the device has been suspended by the input of a "B0H" command during a Block Erase operation. Only a Program or Read operation is allowed during this Erase Suspend interruption.

(9) Interruption of block erasure

After the input of a "B0H" command, neither a Program nor a Read operation is allowed for the block which is currently being erased.



(10) R/$\overline{B}$: Termination for the Ready/Busy pin (R/$\overline{B}$)

A pull-up resistor must be used for termination because the R/$\overline{B}$ buffer consists of an open drain circuit.

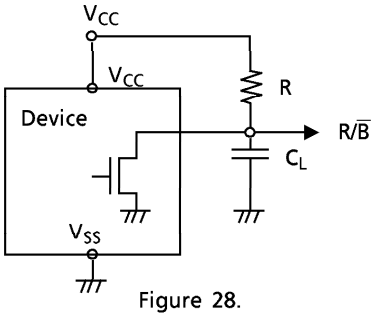
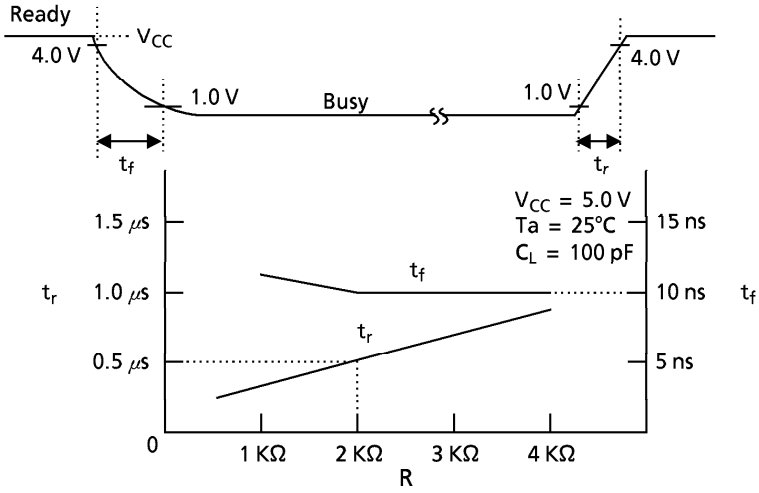



Figure 28.

This data may vary from device to device. We recommend that you use this data as a reference when selecting a resistor value.

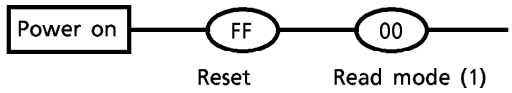



(11) Status after Power On

Although the device is set to Read mode after power-up, the following sequence is needed because all input signals may not be stable at power on.

- Operating mode : Read mode (1)
- Address register : All "0"
- Data register : Indeterminate
- High voltage generation circuit: Off state

Power on sequence




(12) Power On/Off Sequence:

The $\overline{WP}$ signal is useful for protecting against data corruption at power on/off. The following timing is recommended:

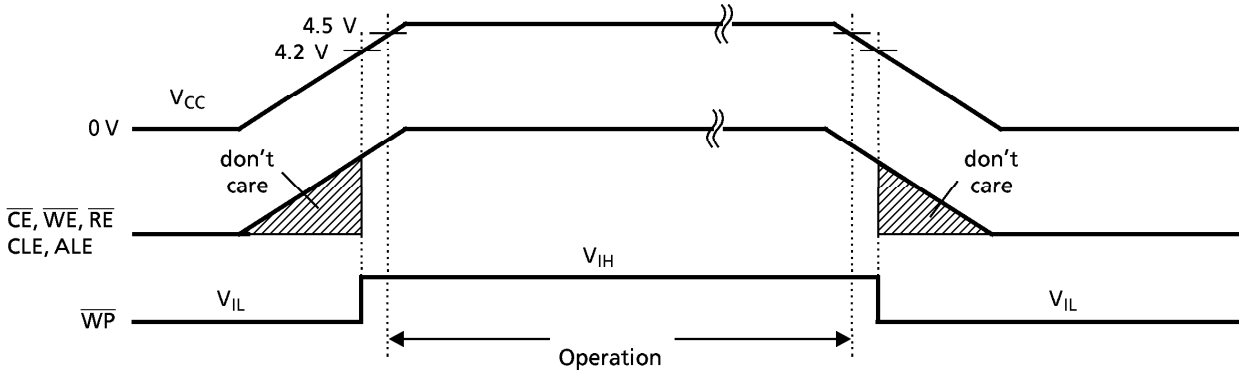



Figure 29. TC5816 Power On/Off Sequence

(13) Note regarding the $\overline{WP}$ Signal

The Erase and Program operations are automatically reset when $\overline{WP}$ goes low. The $\overline{WP}$ signal must be kept high before the input of a "80H"/"60H" command, the Program and Erase commands.

If $\overline{WP}$ goes high after a Program ("80H") or Erase ("60H") command, the Program or Erase operation cannot be guaranteed.

Program

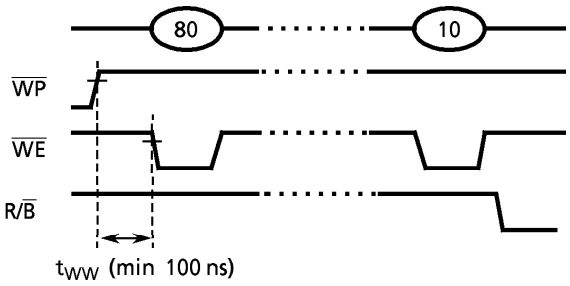



Figure 30.

Erase

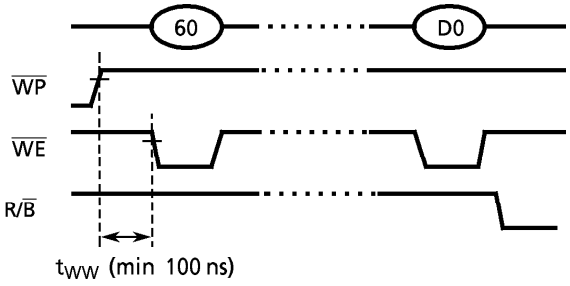
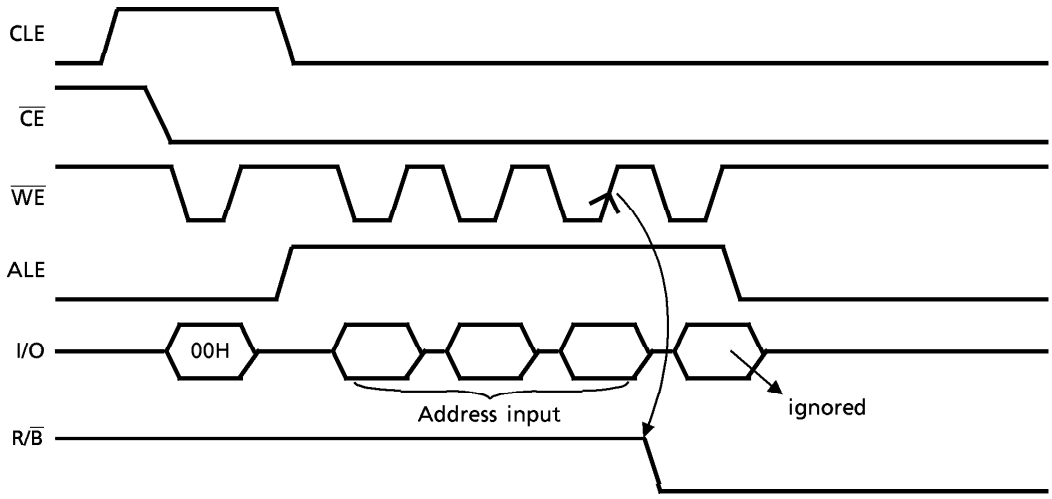



Figure 31.

(14) When four address cycles are input

Although the device may acquire the fourth address, it is ignored inside the chip.

Read operation




Internal read operation starts when $\overline{WE}$ goes high in the third cycle.

Figure 32.

Programming operation

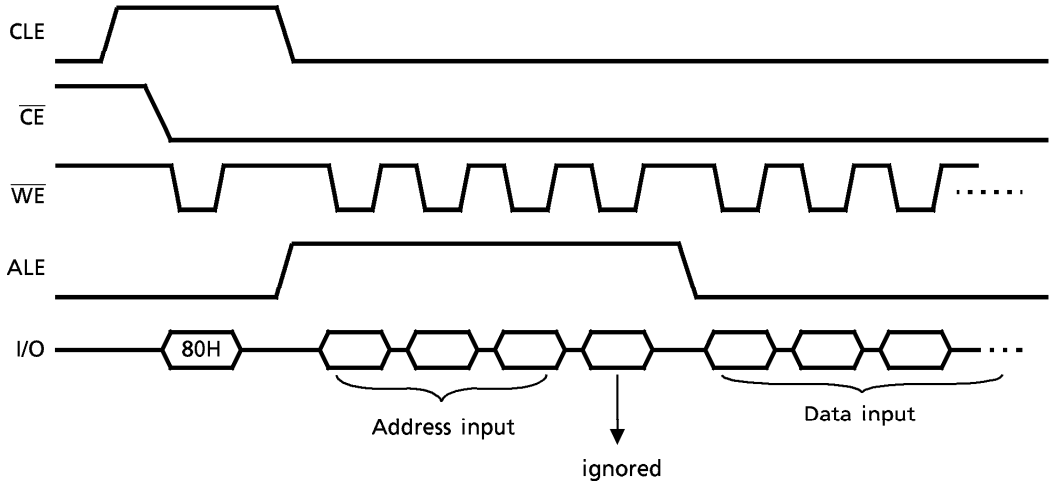



Figure 33.

(15) Number of programming cycle on the same page (Partial Page Program)

A page can be divided into up to 10 segments. Each segment can be programmed individually as shown below.

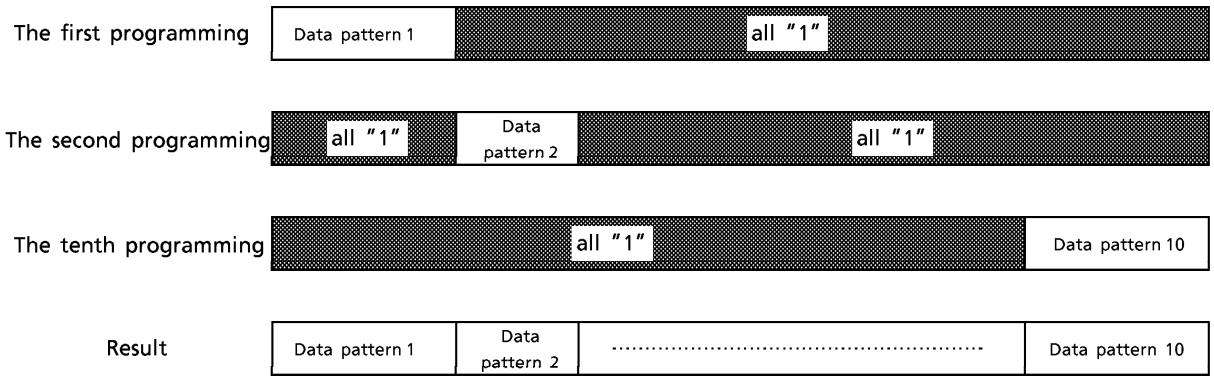



Figure 34.

Note: The input data for unprogrammed or previously programmed page segments must be "1". (i.e. Set all page bytes outside the segment to be programmed to "1".)

(16) Note regarding the $\overline{RE}$ Signal

The internal column address counter is incremented synchronously with the $\overline{RE}$ clock in Read mode. Therefore, once the device has been set to Read mode by the "00H" or "50H" command, the internal column address counter is incremented by the $\overline{RE}$ clock independent of the timing of the address input. If the $\overline{RE}$ clocks are input before address input and the pointer reaches the last column address, an internal read operation (array → register) will occur and the device will be in the Busy state. (Refer to Figure 35.)

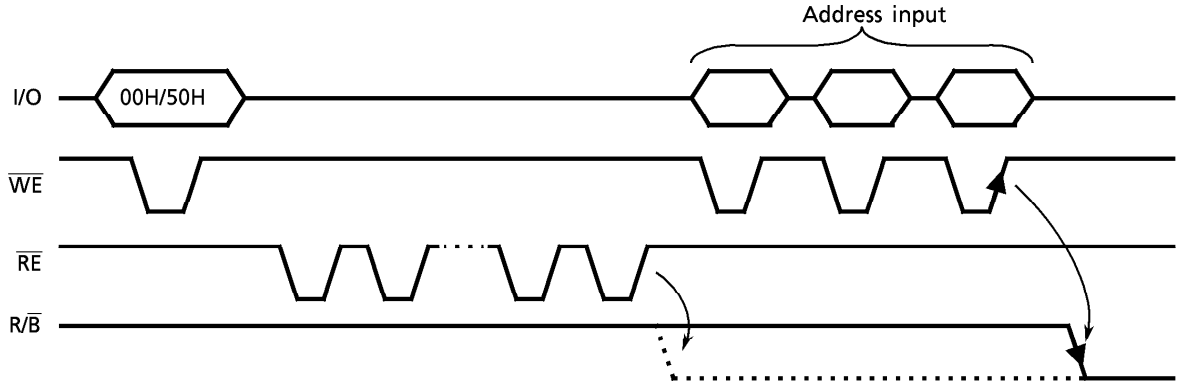
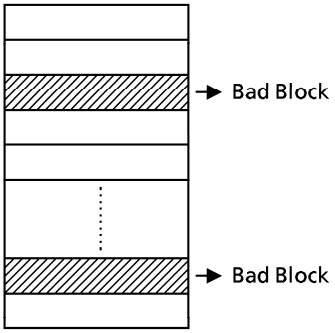



Figure 35.

Hence, the $\overline{RE}$ clocks must be input after address input.

(17) Invalid block (bad block)

The TC5816 device occasionally contains unusable blocks. Therefore, the following issues must be recognized:




Check whether the device has any bad blocks after installation of the device in the system. Do not try to access bad blocks. A bad block does not affect the performance of good blocks as it is isolated from the Bit line by the Select gate. Valid numbers of blocks are as follows:

| | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| Valid Good Block Number | 502 | 508 | 512 | Block |

Figure 36 shows the bad block test flow.

(18) Failure Phenomena for Program and Erase Operations.

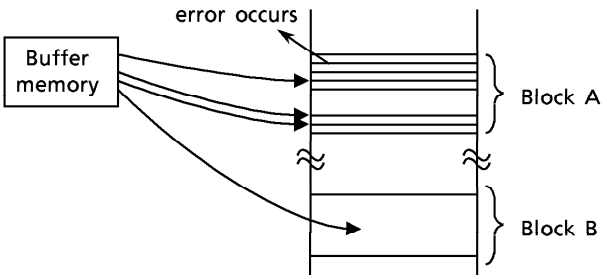
The device may fail during program or erase operation.
The following possible failure modes should be considered when implementing a highly reliable system.

| FAILURE MODE | | DETECTION AND COUNTERMEASURE SEQUENCE |
|---|---|---|
| Block | Erase Failure | Status Read after Erase → Block Replacement |
| Page | Program Failure | Status Read after Prog. → Block Replacement |
| Single Bit* | Program Failure '1' → '0' | (1) Block Verify after Prog. → Retry |
| | | (2) ECC |

* : (1) or (2)

- ECC : Error Correcting code → Hamming Code etc.
  Example : 1 bit correction & 2 bit detection.
- Block Replacement

Program




When an error happens in Block A, try to reprogram the data into another (Block B) by loading from an external buffer. Then, prevent further system accesses to Block A ( by creating a 'bad block' table or an another appropriate scheme.)

Erase

When an error occurs for an erase operation, prevent future accesses to this bad block (again by creating a table within the system or other appropriate scheme).

## BAD BLOCK TEST FLOW

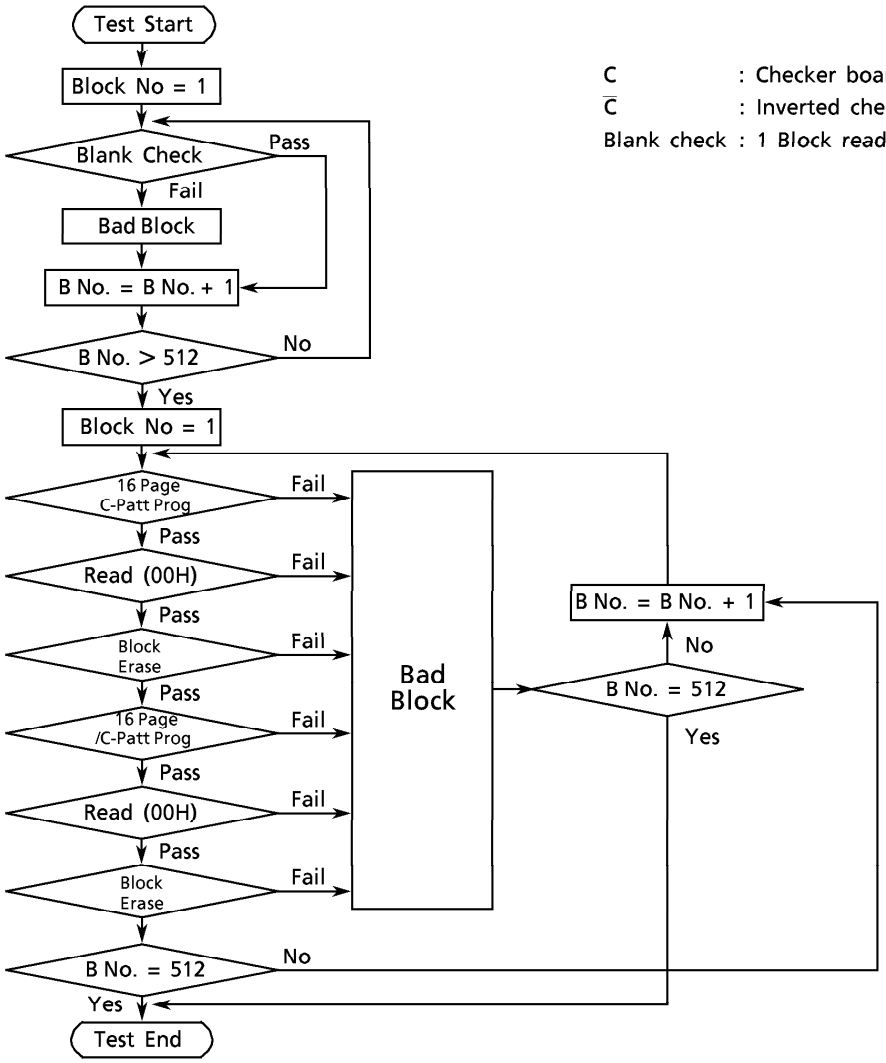



Figure 36.

## ATTENTION

(1) Avoid bending or subjecting the card to sudden impact.

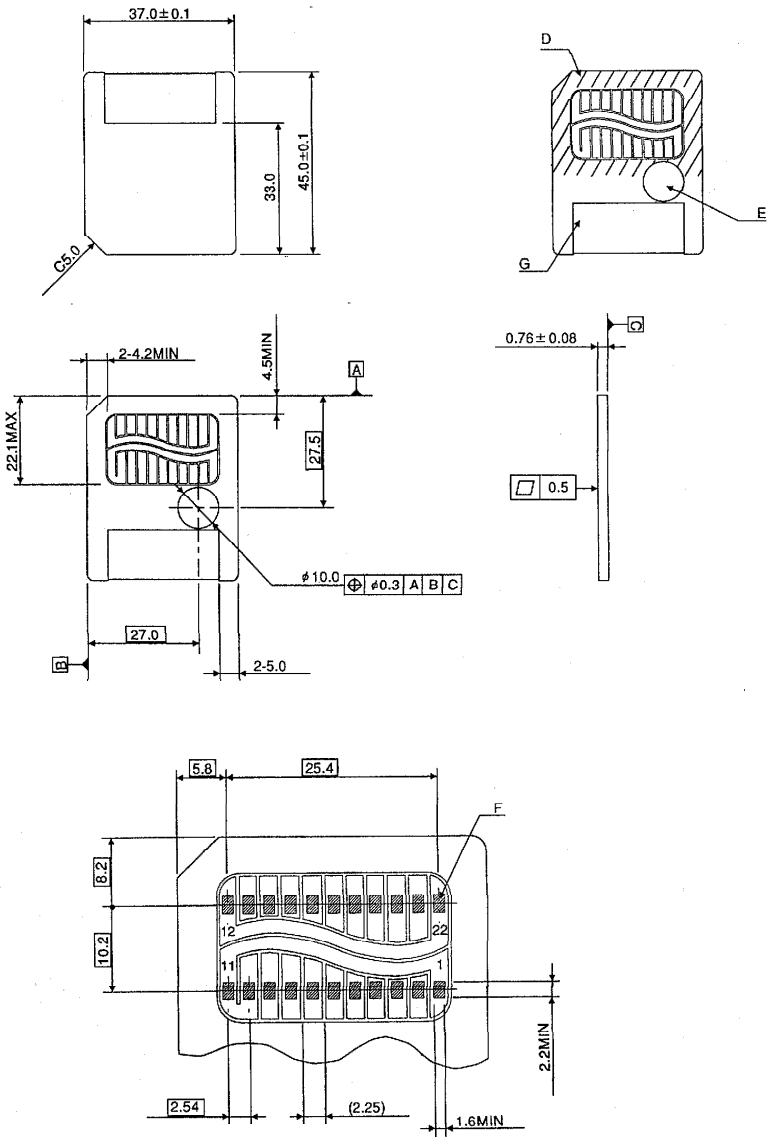
(2) Avoid touching the connectors so as to avoid damage from static electricity.
This card should be kept in the antistatic film case when not in use.

(3) Toshiba cannot accept, and hereby disclaims liability for, any damage to the card including data corruption that may occur because of mishandling.

## PACKAGE DIMENSIONS

FDC – 22

UNITS: mm




Contact area (2 : 1)

E : Write protect area

F : The distance between the surface of D and all contact areas is less than 0.1 mm.

G: Index area