	GM76C256C Series 32Kx8bit CMOS SRAM
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Document Title

32K x8 bit 5.0V Low Power CMOS slow SRAM

Revision History

<u>Revision No</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
00	Revision History Insert Revised - Datasheet format change - PDIP package type insert - Pin configuration change	Jul.07.2000	Final
01	Revised - tWP Value Change @55ns : 45ns -> 40ns	Nov.28.2000	Final
02	Marking Information Add Revised - AC Test Condition Add : 5pF Test Load - tCLZ Value Change : 5ns -> 10ns	Dec.04.2000	Final
03	Changed Logo - HYUNDAI -> hynix	Apr.30.2001	Final



DESCRIPTION

The GM76C256C is a high-speed, low power and 32,786 X 8-bits CMOS Static Random Access Memory fabricated using Hynix's high performance CMOS process technology. It is suitable for use in low voltage operation and battery back-up application. This device has a data retention mode that guarantees data to remain valid at the minimum power supply voltage of 2.0 volt.

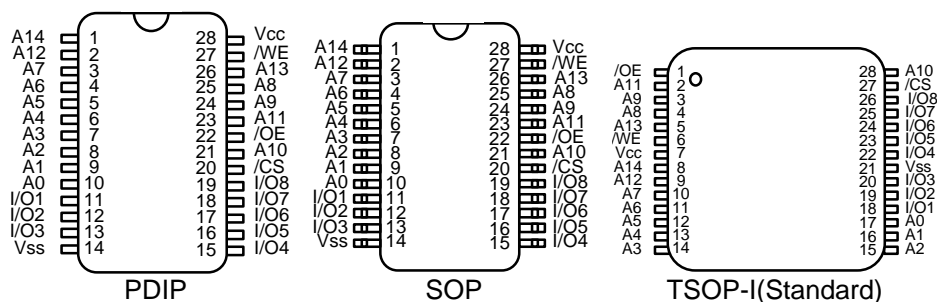
FEATURES

- Fully static operation and Tri-state output
- TTL compatible inputs and outputs
- Low power consumption
- Battery backup(L/LL-part)
- 2.0V(min.) data retention
- Standard pin configuration
- 28 pin 600mil PDIP
- 28 pin 330mil SOP
- 28 pin 8x13.4 mm TSOP-I (Standard)

Product No.	Voltage (V)	Speed (ns)	Operation Current(mA)	Standby Current(uA)		Temperature (°C)
				L	LL	
GM76C256C	5.0	55/70/85	10	40	20	0~70(Normal)
GM76C256CE	5.0	55/70/85	10	60	30	-25~85(Extended)

Note 1. Current value is max.

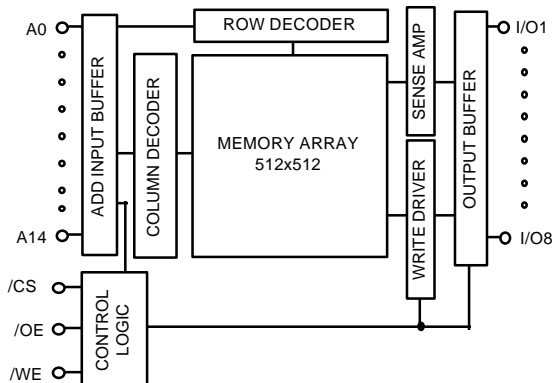
PIN CONNECTION



PIN DESCRIPTION

Pin Name	Pin Function
/CS	Chip Select
/WE	Write Enable
/OE	Output Enable
A0 ~ A14	Address Inputs
I/O1 ~ I/O8	Data Input/Output
Vcc	Power(+5.0V)
Vss	Ground

BLOCK DIAGRAM



ORDERING INFORMATION

Part No.	Speed	Power	Temp	Package
GM76C256CL	55/70/85	L-part	0 to 70°C	PDIP
GM76C256CLL	55/70/85	LL-part	0 to 70°C	PDIP
GM76C256CLE	55/70/85	L-part	-25 to 85°C	PDIP
GM76C256CLLE	55/70/85	LL-part	-25 to 85°C	PDIP
GM76C256CLFW	55/70/85	L-part	0 to 70°C	SOP
GM76C256CLLFW	55/70/85	LL-part	0 to 70°C	SOP
GM76C256CLEFW	55/70/85	L-part	-25 to 85°C	SOP
GM76C256CLLEFW	55/70/85	LL-part	-25 to 85°C	SOP
GM76C256CLT	55/70/85	L-part	0 to 70°C	TSOP-I Standard
GM76C256CLLT	55/70/85	LL-part	0 to 70°C	TSOP-I Standard
GM76C256CLET	55/70/85	L-part	-25 to 85°C	TSOP-I Standard
GM76C256CLET	55/70/85	LL-part	-25 to 85°C	TSOP-I Standard

ABSOLUTE MAXIMUM RATING (1)

Symbol	Parameter	Rating	Unit
V _{CC} , V _{IN} , V _{OUT}	Power Supply, Input/Output Voltage	-0.3 to 7.0	V
T _A	Operating Temperature	GM76C256C	0 to 70
		GM76C256CE	-25 to 85
T _{STG}	Storage Temperature	-65 to 150	°C
P _D	Power Dissipation	1.0	W
I _{OUT}	Data Output Current	50	mA
T _{SDR}	Lead Soldering Temperature & Time	260 •10	°C•sec

Note

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and the functional operation of the device under these or any other conditions above those indicated in the operation of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{CC}	Power Supply Voltage	4.5	5.0	5.5	V
V _{SS}	Ground	0	0	0	V
V _{IH}	Input High Voltage	2.2	-	V _{CC} +0.3	V
V _{IL}	Input Low Voltage	-0.3(1)	-	0.8	V

Note

- V_{IL} = -3.0V for pulse width less than 50ns

TRUTH TABLE

/CS	/WE	/OE	Mode	I/O Operation
H	X	X	Standby	High-Z
L	H	H	Output Disabled	High-Z
L	H	L	Read	Data Out
L	L	X	Write	Data In

Note

- H=V_{IH}, L=V_{IL}, X=Don't Care

DC CHARACTERISTICS

V_{CC} = 5V ±10%, T_A = 0°C to 70°C (Normal)/-25°C to 85°C (Extended), unless otherwise specified.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	
I _{LI}	Input Leakage Current	V _{SS} ≤ V _{IN} ≤ V _{CC}	-1	-	1	μA	
I _{LO}	Output Leakage Current	V _{SS} ≤ V _{OUT} ≤ V _{CC} , /CS = V _{IH} or /OE = V _{IH} or /WE = V _{IL}	-1	-	1	μA	
I _{CC}	Operating Power Supply Current	/CS = V _{IL} , V _{IN} = V _{IH} or V _{IL} , V _{IN} = V _{IH} or V _{IL} , I _{I/O} = 0mA	-	-	10	mA	
I _{CC1}	Average Operating Current	/CS = V _{IL} , V _{IN} = V _{IH} or V _{IL} , Min. Duty Cycle = 100%, I _{I/O} = 0mA	-	-	70	mA	
I _{SB}	TTL Standby Current (TTL Inputs)	/CS = V _{IH} V _{IN} = V _{IH} or V _{IL}	-	-	1	mA	
I _{SB1}	CMOS Standby Current (CMOS Inputs)	/CS ≥ V _{CC} - 0.2V, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ V _{SS} + 0.2V	L	-	-	40	μA
			LL	-	-	20	μA
			LE	-	-	60	μA
			LLE	-	-	30	μA
V _{OL}	Output Low Voltage	I _{OL} = 2.1mA	-	-	0.4	V	
V _{OH}	Output High Voltage	I _{OH} = -1.0mA	2.4	-	-	V	

Note : Typical values are at V_{CC} = 5.0V, T_A = 25°C

AC CHARACTERISTICS(I)

V_{CC} = 5V ±10%, T_A = 0°C to 70°C (Normal) / -25°C to 85°C (Extended) unless otherwise specified.

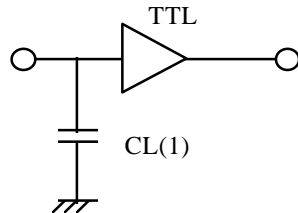
#	Symbol	Parameter	-55		-70		-85		Unit
			Min.	Max.	Min.	Max.	Min	Max.	
READ CYCLE									
1	t _{RC}	Read Cycle Time	55	-	70	-	85	-	ns
2	t _{AA}	Address Access Time	-	55	-	70	-	85	ns
3	t _{ACS}	Chip Select Access Time	-	55	-	70	-	85	ns
4	t _{OE}	Output Enable to Output Valid	-	30	-	35	-	45	ns
5	t _{CLZ}	Chip Select to Output in Low Z	10	-	10	-	10	-	ns
6	t _{OLZ}	Output Enable to Output in Low Z	5	-	5	-	5	-	ns
7	t _{CHZ}	Chip Disable to Output in High Z	0	20	0	30	0	30	ns
8	t _{OHZ}	Out Disable to Output in High Z	0	20	0	30	0	30	ns
9	t _{OH}	Output Hold from Address Change	5	-	5	-	5	-	ns
WRITE CYCLE									
10	t _{WC}	Write Cycle Time	55	-	70	-	85	-	ns
11	t _{CW}	Chip Selection to End of Write	50	-	65	-	75	-	ns
12	t _{AW}	Address Valid to End of Write	50	-	65	-	75	-	ns
13	t _{AS}	Address Set-up Time	0	-	0	-	0	-	ns
14	t _{WP}	Write Pulse Width	40	-	50	-	60	-	ns
15	t _{WR}	Write Recovery Time	0	-	0	-	0	-	ns
16	t _{WHZ}	Write to Output in High Z	0	20	0	25	0	30	ns
17	t _{DW}	Data to Write Time Overlap	25	-	30	-	40	-	ns
18	t _{DH}	Data Hold from Write Time	0	-	0	-	0	-	ns
19	t _{OW}	Output Active from End of Write	5	-	5	-	5	-	ns

AC TEST CONDITIONS

TA = 0°C to 70°C (Normal) / -25°C to 85°C (Extended) unless otherwise specified.

Parameter		Value
Input Pulse Level		0.8V to 2.4V
Input Rise and Fall Time		5ns
Input and Output Timing Reference Level		1.5V
Output Load	tCLZ,tOLZ,tCHZ,tOHZ,tWHZ,tOW	CL = 5pF + 1TTL Load
	Others	CL = 100pF + 1TTL Load

AC TEST LOADS



Note : Including jig and scope capacitance

CAPACITANCE

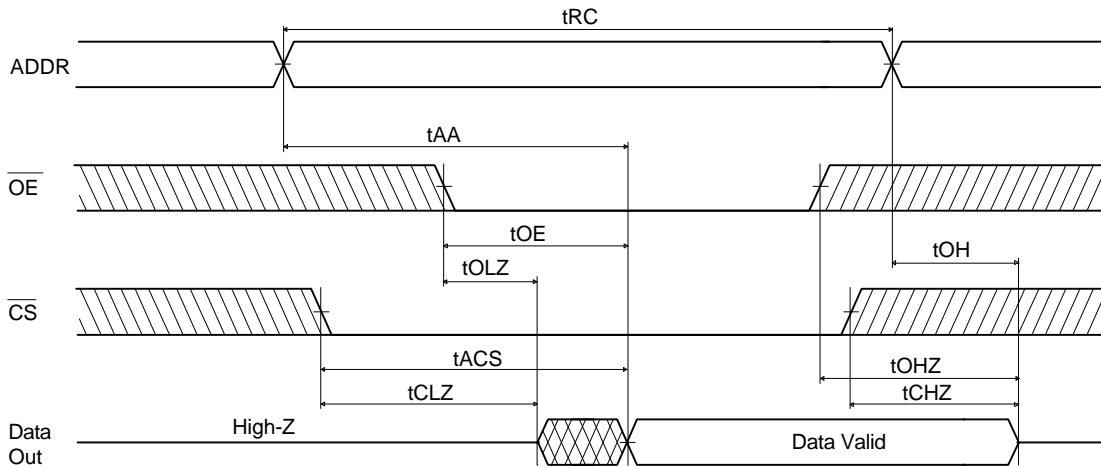
TA = 25°C, f = 1.0MHz

Symbol	Parameter	Condition	Max.	Unit
CIN	Input Capacitance	VIN = 0V	6	pF
C _{I/O}	Input /Output Capacitance	V _{I/O} = 0V	8	pF

Note : These parameters are sampled and not 100% tested

TIMING DIAGRAM

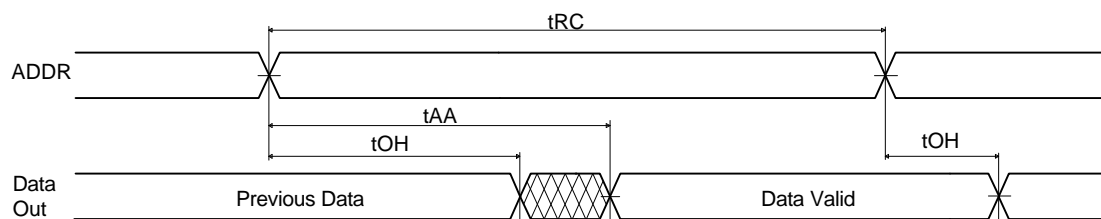
READ CYCLE 1



Note(READ CYCLE):

1. t_{CHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{CHZ} max. is less than t_{CLZ} min. both for a given device and from device to device.
3. \overline{WE} is high for the read cycle.

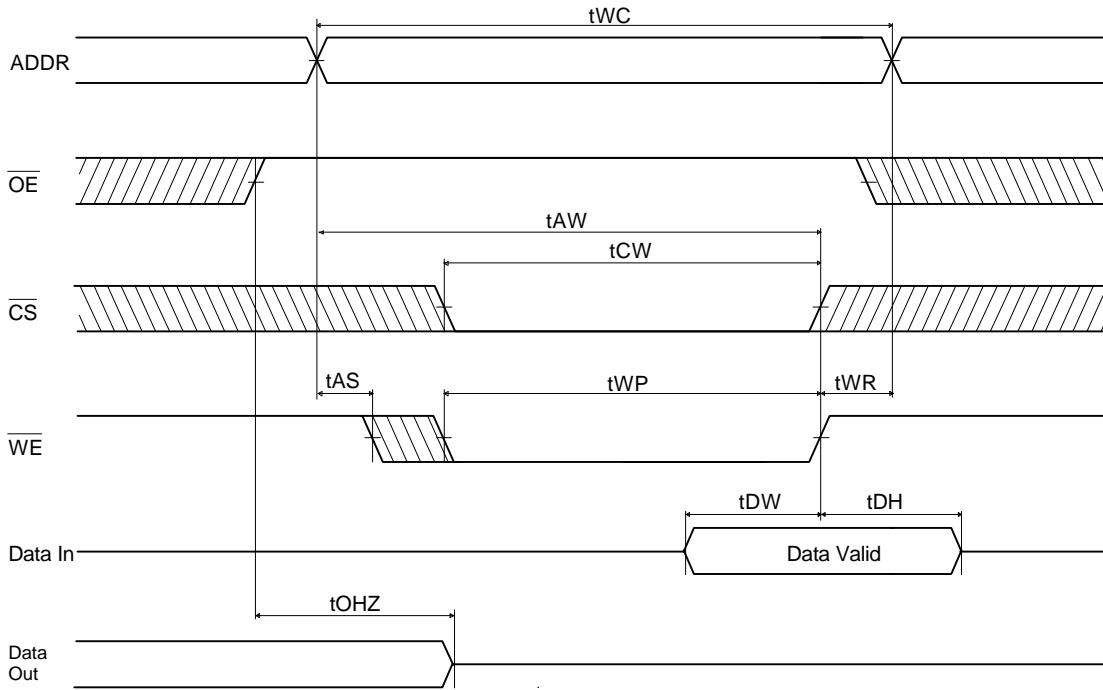
READ CYCLE 2



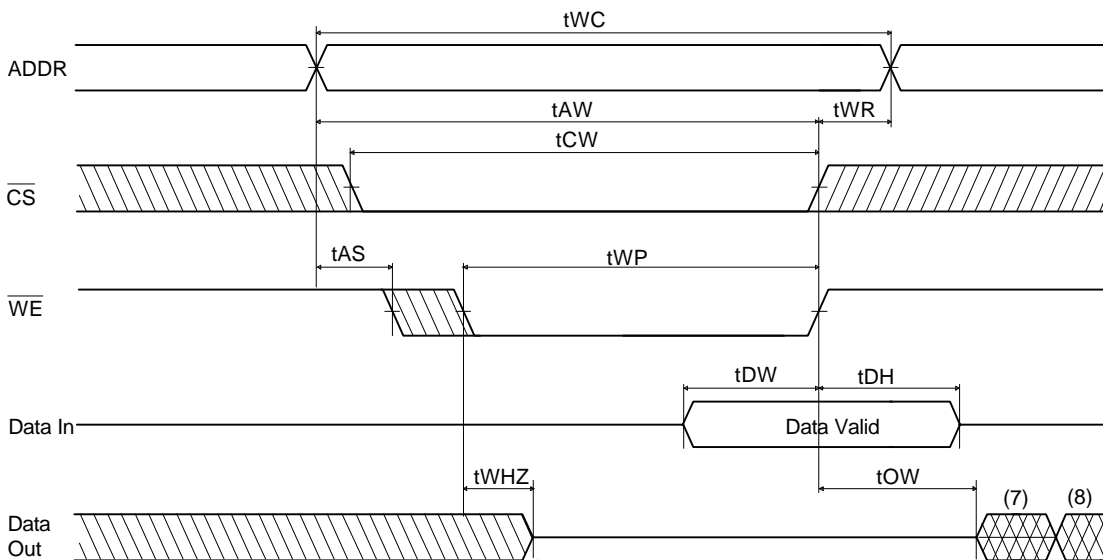
Note(READ CYCLE):

1. \overline{WE} is high for the read cycle.
2. Device is continuously selected $\overline{CS} = V_{IL}$.
3. $\overline{OE} = V_{IL}$.

WRITE CYCLE 1 (/OE Clocked)



WRITE CYCLE 2 (/OE Low Fixed)



Notes(WRITE CYCLE):

1. A write occurs during the overlap of a low /CS and a low /WE. A write begins at the latest transition among /CS going low and /WE going low: A write ends at the earliest transition among /CS going high and /WE going high. tWP is measured from the beginning of write to the end of write.
2. tcw is measured from the later of /CS going low to the end of write .
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end of write to the address change. tWR is applied in case a write ends as /CS, or /WE going high.
5. If /OE and /WE are in the read mode during this period, and the I/O pins are in the output low-Z state, input of opposite phase of the output must not be applied because bus contention can occur.
6. If /CS goes low simultaneously with /WE going low, or after /WE going low, the outputs remain in high impedance state.
7. DOUT is the same phase of the latest written data in this write cycle.
8. DOUT is the read data of the new address.

DATA RETENTION CHARACTERISTIC

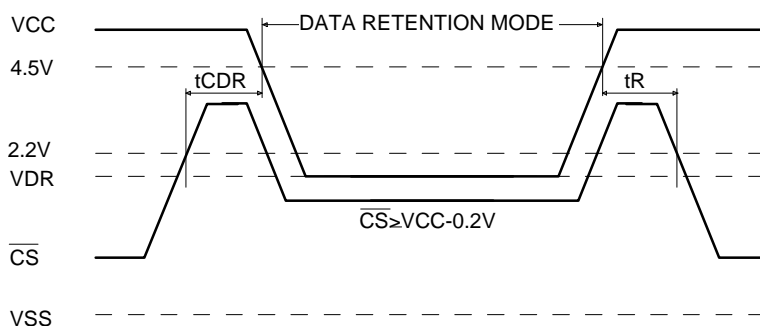
TA = 0°C to 70°C (Normal) / -25°C to 85°C (Extended) unless otherwise specified.

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit	
VDR	Vcc for Data Retention	$CS \geq V_{cc} - 0.2V$, $V_{IN} \geq V_{cc} - 0.2V$ or $V_{IN} \leq V_{ss} + 0.2V$	2.0	-	-	V	
ICCDR	Data Retention Current	$V_{cc} = 3.0V$, $/CS \geq V_{cc} - 0.2V$, $V_{IN} \geq V_{cc} - 0.2V$ or $V_{IN} \leq V_{ss} + 0.2V$	L	-	1	15	uA
			LL	-	0.5	7	uA
			LE	-	1	20	uA
			LLE	-	0.5	10	uA
tCDR	Chip Deselect to Data Retention Time	See Data Retention	0	-	-	ns	
tR	Operating Recovery Time	Timing Diagram	tRC(2)	-	-	ns	

Notes

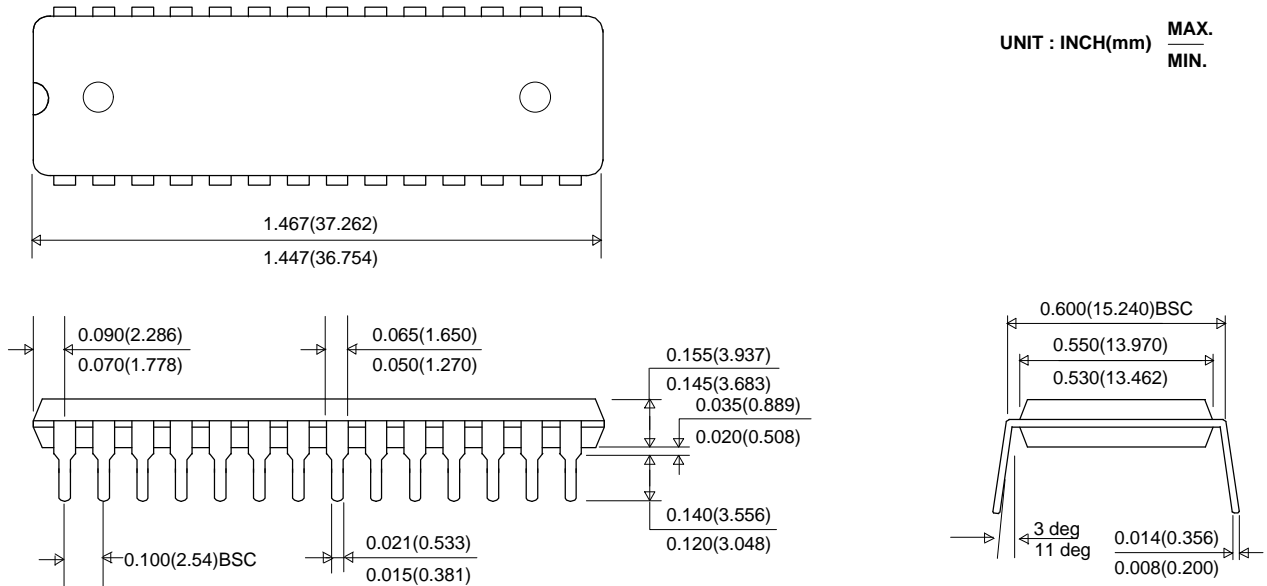
1. Typical values are under the condition of TA = 25 °C.
2. tRC is read cycle time.

DATA RETENTION TIMING DIAGRAM

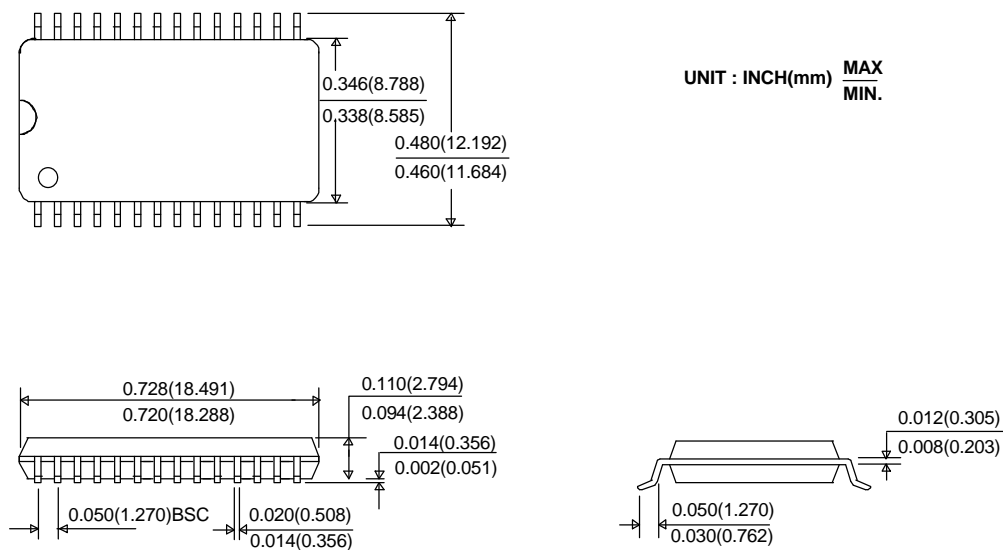


PACKAGE INFORMATION

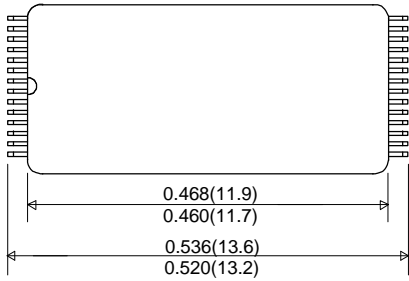
28pin 600mil Dual In-Line Package(Blank)



28pin 330mil Small Outline Package(FW)



28pin 8x13.4mm Thin Small Outline Package Standard(T)



UNIT : INCH(mm) ^{MAX.}
_{MIN.}

