PRODUCT SPECIFICATION

GoldStar
GOLD STAR CO.,LTD.

GM76C88

8,192 × 8 BIT STATIC RAM

T-46-23-12

Description

The GM76C88 is 65,536 bit staic random access memory organized as 8,192 words by 8 bits using CMOS technology, and operated from a single 5V supply. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 80mA and minimum cycle time of 70/85/100ns. The combination of speed-optimized circuitry results in a very high-speed memory device. Thus the GM76C88 is suitable for use in various microprocessor application systems where high speed are required. The GM76C88 is offered in 28 pin DIP.

Features

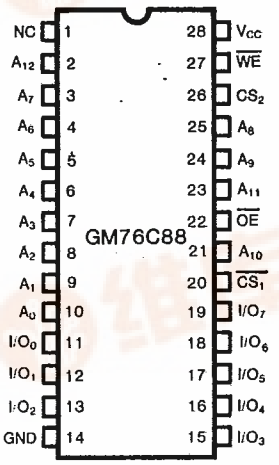
- **8,192 × 8 organization**
- **High Speed:**
  Fast Access and Cycle Time 70/85/100ns (max.)
- **Low Power Standby and Low Power Operation**
- **Completely Static RAM: No Clock or Timing Strobe Required**
- **Common I/O (Three-State Output)**
- **Directly TTL Compatible: All Inputs and Outputs**
- **Single + 5V Operation (±10%)**
- **Standard 28 DIP (600 mil)/28 SOP (330 mil)**

Pin Name

A_0~A_{12}	:	Address Input
$\overline{WE}$	:	Write Enable Input
$\overline{OE}$	:	Output Enable Input
$\overline{CS1}$, CS2	:	Chip Select Input
I/O_0~I/O_7	:	Data Input/Output
V_{CC}	:	Power Supply, +5V
GND	:	Ground

Pin Configuration

(Top View)



Absolute Maximum Ratings

Voltage on Any Pin with respect to GND	V_{CC}	−2.0 to 7.0V
Storage Temperature	T_{STG}	−55°C to +150°C
Operating Temperature	T_{OPR}	0°C to +70°C
Power dissipation	P_D	1.0W

Recommended Operating Conditions:

T_A=0°C to +70°C

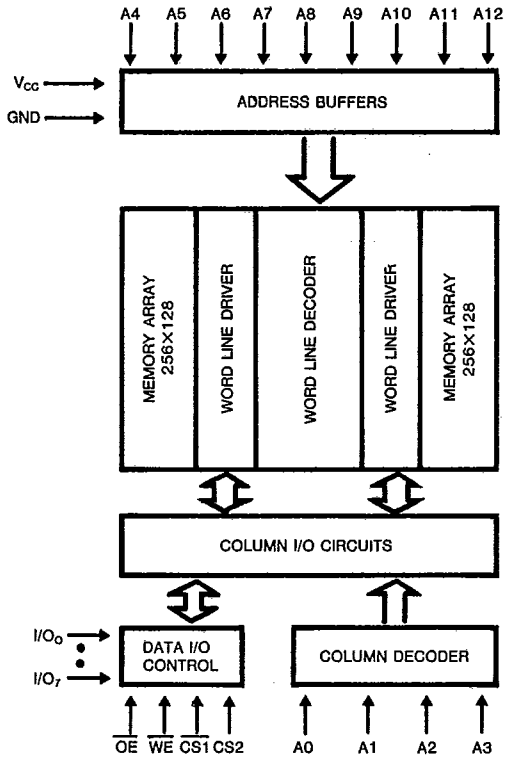
V_{CC}	Supply Voltage	4.5 to 5.5V
V_{IH}	Input High Voltage	2.2 to 6.0V
V_{IL}	Input Low Voltage	−0.5 to 0.8V

All voltages are referenced to GND pin=0V.

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

Functional Block Diagram



Truth Table

$\overline{WE}$	$\overline{CS_1}$	CS_2	$\overline{OE}$	Mode	I/O PIN	V_{CC} CURRENT	NOTE
X	H	X	X	Not Selected (Power Down)	High Z	I_{SB}, I_{SB1}	
X	X	L	X		High Z	I_{SB}, I_{SB2}	
H	L	H	H	Output Disabled	High Z	I_{CC}, I_{CC1}	
H	L	H	L	Read	Dout	I_{CC}, I_{CC1}	
L	L	H	H	Write	Din	I_{CC}, I_{CC1}	Write Cycle (1)
L	L	H	L		Din	I_{CC}, I_{CC1}	Write Cycle (2)

X: Don't Care

DC Electrical Characteristics: (V_{CC}=5V±10%, T_A=0°~70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP*	MAX	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{IN}=GND to V_{CC}	−5	—	+5	μA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS1}$=V_{IH} or CS2=V_{IL} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, $V_{I/O}$=GND to V_{CC}	−10	—	+10	μA
I_{CC}	Operating Power Supply Current	$\overline{CS1}$=V_{IL}, CS2=V_{IH}, $I_{I/O}$=0mA	—	40	80	mA
I_{CC1}	Average Operating Current	Min. cycle, duty=100%, $I_{I/O}$=0mA	—	60	110	mA
I_{SB}	Standby Power Supply Current	$\overline{CS1}$=V_{IH} or CS2=V_{IL}	—	1	3	mA
I_{SB1}**		$\overline{CS1}$≥V_{CC}−0.2V, CS2≥V_{CC}−0.2V or CS2≤0.2V	—	0.02	2	mA
I_{SB2}**		CS2≤0.2V	—	0.02	2	mA
V_{OL}	Output Voltage	I_{OL}=2.1mA	—	—	0.4	V
V_{OH}		I_{OH}=−1.0mA	2.4	—	—	V

* Typical limits are at V_{CC}=5.0V, T_A=25°C and specified loading.
** V_{IL} min=−0.3V

Capacitance: (T_A=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN	MAX	UNIT
C_{IN}	Input Capacitance	V_I=0V		6	pF
C_{OUT}	Output Capacitance	V_O=0V		8	

Note: This parameter is sampled and not 100% tested.

AC Test Conditions

Input Pulse Levels ..... GND to 3.0V
Input Rise and Fall Times 10ns
Input and Output Timing References 1.5V
Output Load ..... 1 TTL Gate and C_L=100 pF (including scope and jig.)

Figure 1 Output Load

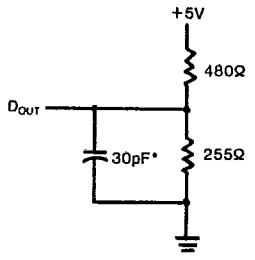
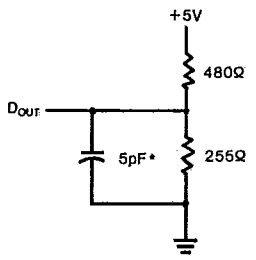


Figure 2 Output Load
(for t_{LZ1}, t_{LZ2}, t_{WHZ}, t_{OW})



*Including scope and jig

AC Operating Characteristics: V_{DD}=5V±10%, T_A=0°~70°C

- **Read Cycle**

SYMBOL	PARAMETER		GM76C88-70		GM76C88-85		GM76C88-10		UNIT
			MIN	MAX	MIN	MIX	MIN	MAX	
t_{RC}	Read Cycle Time		70		85		100		ns
t_{ACC}	Address Access Time			70		85		100	ns
t_{CO1}	Chip Selection to Output	$\overline{CW1}$		70		85		100	ns
t_{CO2}		CS2		70		85		100	ns
t_{OE}	Output Enable to Output Valid			35		40		50	ns
t_{LZ1}	Chip Selection to Output in Low Z	$\overline{CS1}$	10		10		10		ns
t_{LZ2}		CS2	10		10		10		ns
t_{OLZ}	Output Enable to Output in Low Z		5		5		5		ns
t_{HZ1}	Chip Deselection to Output in High Z	$\overline{CS1}$	0	30	0	35	0	35	ns
t_{HZ2}		CS2	0	30	0	35	0	35	ns
t_{OHZ}	Output Disable to Output in High Z		0	30	0	35	0	35	ns
t_{OH}	Output Hold from Address Change		10		10		10		ns

- **Write Cycle**

SYMBOL	PARAMETER		GM76C88-70		GM76C88-85		GM76C88-10		UNIT
			MIN	MAX	MIN	MIX	MIN	MAX	
t_{WC}	Write Cycle Time		70		85		100		ns
t_{CW}	Chip Selection to End of Write		60		70		80		ns
t_{AS}	Address Set up Time		0		0		0		ns
t_{AW}	Address Valid to End of Write		60		70		80		ns
t_{WP}	Write Pulse Width		40		50		60		ns
t_{WR1}	Write Recovery Time	$\overline{CS1}$, $\overline{WE}$	5		5		5		ns
t_{WR2}		CS2	15		15		15		ns
t_{WHZ}	Write to Output in High Z		0	30	0	35	0	35	ns
t_{DW}	Data to Write Overlap		35		40		40		ns
t_{DH}	Data Hold from Write Time		0		0		0		ns
t_{OHZ}	$\overline{OE}$ to Output in High Z		0	30	0	35	0	35	ns
t_{OW}	Output Active from end of Write		5		5		5		ns

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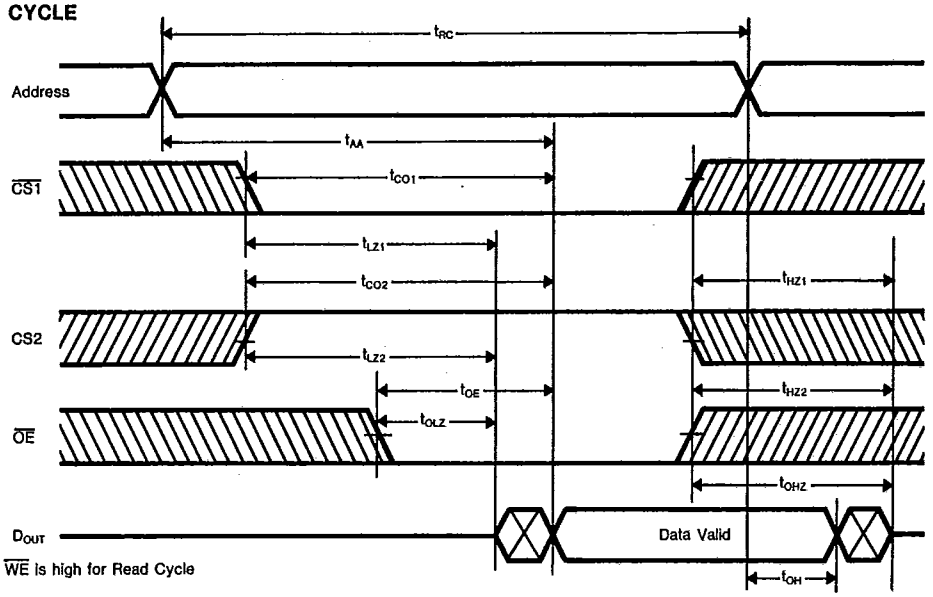
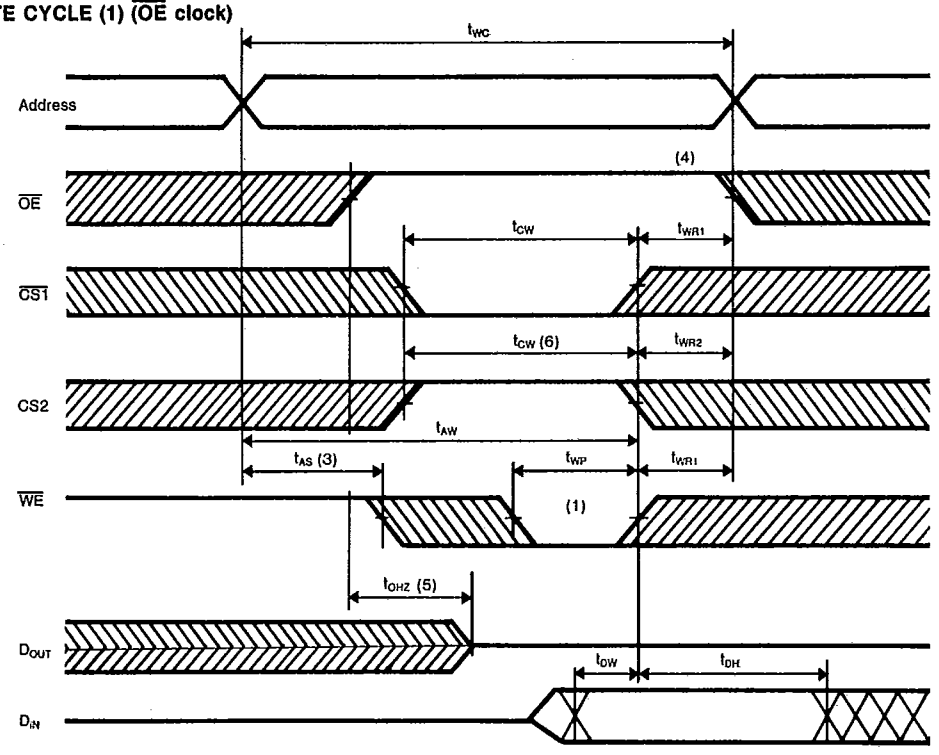
Timing Waveforms

- **READ CYCLE**



NOTE: 1) $\overline{WE}$ is high for Read Cycle

- **WRITE CYCLE (1) ($\overline{OE}$ clock)**



- **WRITE CYCLE (2) ($\overline{OE}$ Low Fix)**

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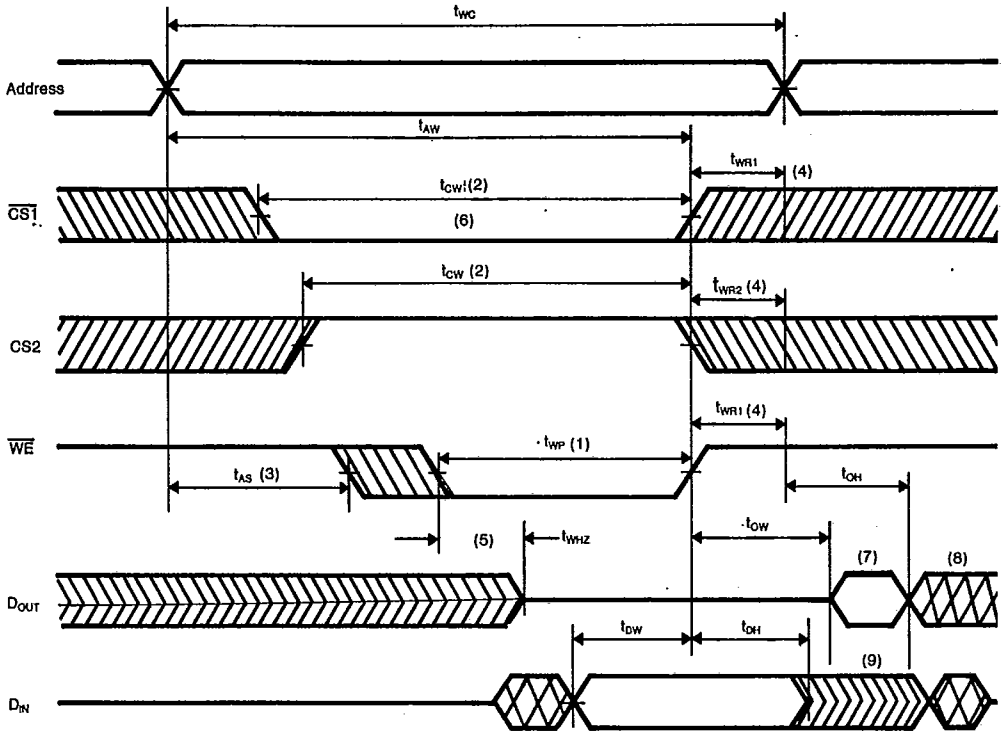

NOTES:
1. A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change.
   t_{WR1} applies in case a write ends at $\overline{CS1}$ or $\overline{WE}$ going high.
   t_{WR2} applies in case a write ends at CS2 going low.
5. During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
6. If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
7. Dout is the same phase of the latest written data in this write cycle.
8. Dout is the read data of next address.
9. If $\overline{CS1}$ is low and CS2 is high during this period, I/O pins are in the output state. Therefore, the input signals of opposite phase to the outputs must not be applied to them.

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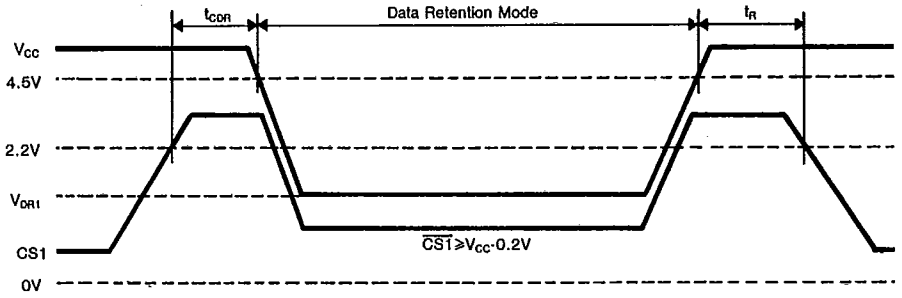
Data Retention Characteristics: (T_A=0°~70°C)

SYMBOL	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DR}	V_{CC} for Data Retention	V_{DR1}	$\overline{CS1}\geq V_{CC}-0.2V$, $CS2\geq V_{CC}-0.2V$ or $CS2\leq 0.2V$	2.0	—	—	V
		V_{DR2}	$CS2\leq 0.2V$	2.0	—	—	V
I_{CCDR}	Data Retention Current	I_{CCDR1}	V_{CC}=3.0V, $\overline{CS1}\geq V_{CC}-0.2V$, $CS2\geq V_{CC}-0.2V$ or $CS2\leq 0.2V$	—	1	50*	μA
		I_{CCDR2}	V_{CC}=3.0V, $CS2\leq 0.2V$	—	1	50*	μA
t_{CDR}	Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	—	—	ns
t_R	Operation Recovery Time	t_R		t_{RC}**	—	—	ns

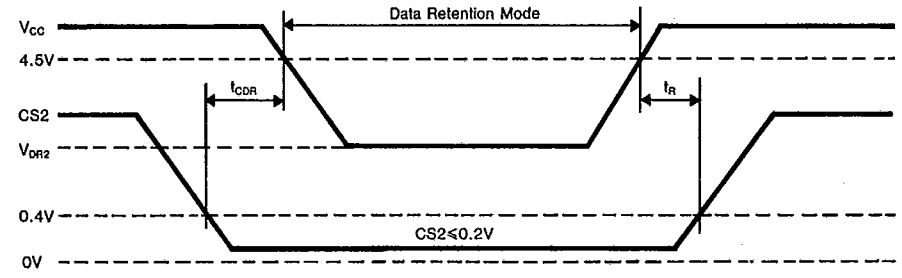
* V_{IL} min=−0.3V, 20μA max at T_A=0~40°C

** t_{RC}=Read Cycle Time

- **Low V_{CC} Data Retention Mode:** (1) $\overline{CS1}$ Controlled



- **Low V_{CC} Data Retention Mode:** (2) CS2 Controlled



NOTE: In Data Retention Mode, CS2 controls the Address, $\overline{WE}$, $\overline{CS1}$, $\overline{OE}$ and Din buffer. If CS2 controls data retention mode, Vin for these inputs can be in the high impedance state. If $\overline{CS1}$ controls the data retention mode, CS2 must satisfy either $CS2\geq V_{CC}-0.2V$ or $CS2\leq 0.2V$. The other input levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

PACKAGE DIMENSION

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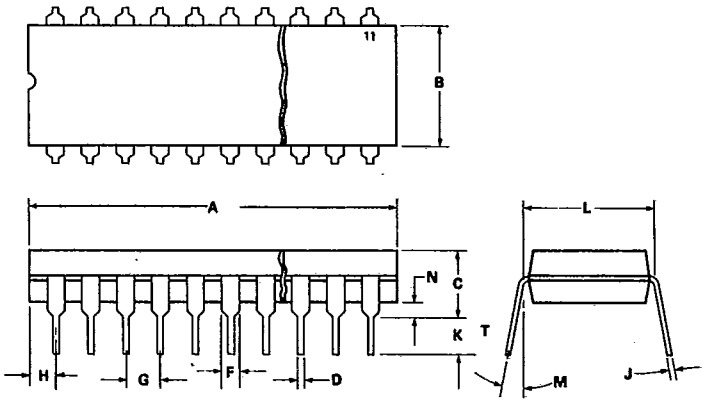
PLASTIC DIP



(UNIT: INCHES)

SYMBOL	16 PIN		18 PIN		20 PIN		22 PIN	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	0.738	0.752	0.875	0.900	1.013	1.040	1.095	1.150
B	0.245	0.255	0.245	0.255	0.263	0.273	0.260	0.287
C	0.143	0.152	0.145	0.162	0.143	0.152	0.145	0.160
D	TYP. 0.018		TYP. 0.018		TYP. 0.018		TYP. 0.018	
F	TYP. 0.063		TYP. 0.060		TYP. 0.065		TYP. 0.060	
G	0.09	0.11	0.09	0.11	0.09	0.11	0.09	0.11
H	0.015	0.030	0.04	0.05	0.058	0.066	—	0.075
J	0.009	0.014	0.009	0.015	0.009	0.010	0.009	0.010
K	0.125	0.145	0.125	0.130	0.125	0.132	0.125	0.142
L	0.300 BSC		0.300 BSC		0.300 BSC		0.300 BSC	
M	0′	10′	0′	10′	0′	10′	0′	10′
N	0.015	—	0.015	—	0.015	—	0.015	

SYMBOL	24 PIN		28 PIN					
	MIN	MAX	MIN	MAX				
A	1.243	1.260	1.415	1.460				
B	0.535	0.545	0.535	0.545				
C	0.158	0.170	0.158	0.170				
D	TYP. 0.018		TYP. 0.018					
F	TYP. 0.060		TYP. 0.060					
G	0.09	0.11	0.09	0.11				
H	0.06	0.075	0.06	0.076				
J	0.009	0.015	0.009	0.015				
K	0.125	0.132	0.125	0.132				
L	0.600	0.625	0.600	0.620				
M	0′	10′	0′	10′				
N	0.008	—	0.008	—				

PACKAGE DIMENSION

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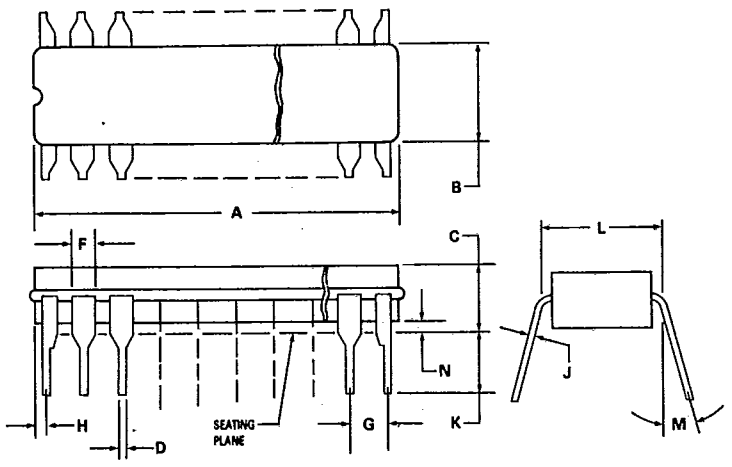
CER DIP



(UNIT : INCHES)

SYMBOL	16 PIN		20 PIN		24 PIN		28 PIN	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	0.753	0.785	0.940	0.985	1.240	1.290	1.440	1.485
B	0.272	0.294	0.265	0.306	0.514	0.526	0.514	0.598
C	0.165	0.200	0.165	0.200	0.165	0.200		0.225
D	0.015	0.021	0.015	0.021	0.015	0.021	0.015	0.023
F	0.055	0.065	0.055	0.065	0.055	0.065	0.055	0.065
G	0.09	0.11	0.09	0.11	0.09	0.11	0.09	0.11
H	0.012	0.060	0.012	0.060	0.040	0.098	0.040	0.098
J	0.008	0.012	0.008	0.012	0.008	0.012	0.008	0.012
K	0.125	0.20	0.125	0.20	0.125	0.20	0.125	0.20
L	0.29	0.32	0.29	0.32	0.590	0.620	0.590	0.620
M	0°	10°	0°	10°	0°	10°	0°	10°
N	0.02	0.06	0.02	0.07	0.02	0.07	0.02	0.07

PACKAGE DIMENSION

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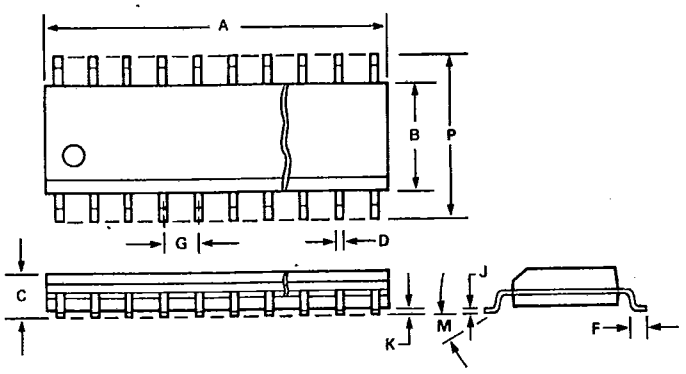
SOP



(UNIT : INCHES)

CODE NO.	20 F		24 F		24 FW			
PIN	20 PIN		24 PIN		24 PIN			
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX		
A	0.496	0.510	0.602	0.614	0.622	0.638		
B	0.292	0.299	0.292	0.299	TYP. 0.331			
C	0.097	0.104	0.097	0.104	—	0.098		
D	0.014	0.019	0.014	0.019	0.012	0.018		
F	0.018	0.035	0.018	0.035	TYP 0.039			
G	0.050 BSC		0.050 BSC		0.050 BSC			
J	0.010 BSC		0.010 BSC		0.010 BSC			
K	0.004	0.008	0.0055	0.0115	0.004			
P	0.400	0.410	0.400	0.410	0.453	0.477		
M	0'	8'	0'	8'	—	—		

CODE NO.	28 F		28 FW					
PIN	28 PIN		28 PIN					
SYMBOL	MIN	MAX	MIN	MAX				
A	0.703	0.712	0.720	0.750				
B	0.292	0.289	TYP. 0.331					
C	0.097	0.104		0.098				
D	0.014	0.019	0.012	0.018				
F	0.018	0.035	TYP. 0.039					
G	0.050 BSC		0.050 BSC					
J	0.010 BSC		0.010 BSC					
K	0.0055	0.0115	0.004	—				
P	0.400	0.410	0.453	0.477				
M	0'	8'	—	—				

PACKAGE DIMENSION

SIDE BRAZED

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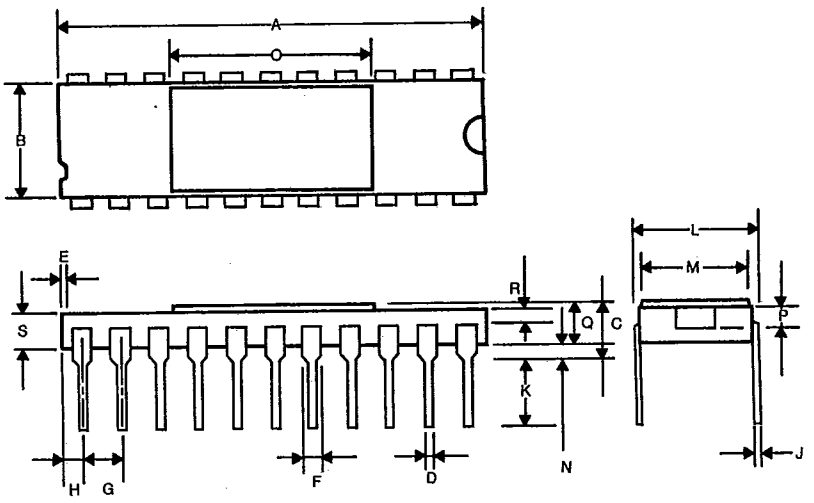

(UNIT: INCHES)

SYMBOL	22 PIN	
	MIN	MAX
A	1.088	1.112
B	0.281	0.298
C	—	0.160
D	0.016	0.020
E	0.004	—
F	TYP. 0.050	
G	0.09	0.105
H	0.035	0.065
J	0.009	0.011

SYMBOL	22 PIN	
	MIN	MAX
K	0.14	0.170
L	0.290	0.310
M	0.265	0.275
N	0.020	0.050
O	0.555	0.565
P	TYP. 0.050	
Q	0.092	0.122
R	0.005	—
S	0.08	—