



**GM76U256C Series**  
**32Kx8bit CMOS SRAM**

Document Title

**32K x8 bit 3.0V Low Power CMOS slow SRAM**

Revision History

<u>Revision No</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
00	Revision History Insert Revised - Datasheet format change - PDIP package type insert - Pin configuration change	Jul.08.2000	Final
01	Marking Information Add Revised - AC Test Condition Add : 5pF Test Load	Dec.04.2000	Final
02	Changed Logo - HYUNDAI -> hynix	Apr.30.2001	Final





**ORDERING INFORMATION**

Part No.	Speed	Power	Temp	Package
GM76U256CL	100/120	L-part	0 to 70°C	PDIP
GM76U256CLL	100/120	LL-part	0 to 70°C	PDIP
GM76U256CLE	100/120	L-part	-25 to 85°C	PDIP
GM76U256CLLE	100/120	LL-part	-25 to 85°C	PDIP
GM76U256CLFW	100/120	L-part	0 to 70°C	SOP
GM76U256CLLFW	100/120	LL-part	0 to 70°C	SOP
GM76U256CLEFW	100/120	L-part	-25 to 85°C	SOP
GM76U256CLLEFW	100/120	LL-part	-25 to 85°C	SOP
GM76U256CLT	100/120	L-part	0 to 70°C	TSOP-I Standard
GM76U256CLLT	100/120	LL-part	0 to 70°C	TSOP-I Standard
GM76U256CLET	100/120	L-part	-25 to 85°C	TSOP-I Standard
GM76U256CLET	100/120	LL-part	-25 to 85°C	TSOP-I Standard

**ABSOLUTE MAXIMUM RATING (1)**

Symbol	Parameter	Rating	Unit
V <sub>CC</sub> , V <sub>IN</sub> , V <sub>OUT</sub>	Power Supply, Input/Output Voltage	-0.3 to 4.6	V
T <sub>A</sub>	Operating Temperature	GM76U256C	0 to 70
		GM76U256CE	-25 to 85
T <sub>STG</sub>	Storage Temperature	-65 to 150	°C
P <sub>D</sub>	Power Dissipation	1.0	W
I <sub>OUT</sub>	Data Output Current	50	mA
T <sub>SOLDER</sub>	Lead Soldering Temperature & Time	260 •10	°C•sec

**Note**

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and the functional operation of the device under these or any other conditions above those indicated in the operation of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect reliability.

**RECOMMENDED DC OPERATING CONDITIONS**

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>CC</sub>	Power Supply Voltage	2.7	3.0	3.3	V
V <sub>SS</sub>	Ground	0	0	0	V
V <sub>IH</sub>	Input High Voltage	2.2	-	V <sub>CC</sub> +0.3	V
V <sub>IL</sub>	Input Low Voltage	-0.3(1)	-	0.4	V

**Note**

- V<sub>IL</sub> = -3.0V for pulse width less than 50ns

**TRUTH TABLE**

/CS	/WE	/OE	Mode	I/O Operation
H	X	X	Standby	High-Z
L	H	H	Output Disabled	High-Z
L	H	L	Read	Data Out
L	L	X	Write	Data In

**Note**

- H=V<sub>IH</sub>, L=V<sub>IL</sub>, X=Don't Care

## DC CHARACTERISTICS

V<sub>CC</sub> = 3.0V ±10%, T<sub>A</sub> = 0°C to 70°C (Normal)/-25°C to 85°C (Extended), unless otherwise specified.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	
I <sub>LI</sub>	Input Leakage Current	V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	-1	-	1	μA	
I <sub>LO</sub>	Output Leakage Current	V <sub>SS</sub> ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , /CS = V <sub>IH</sub> or /OE = V <sub>IH</sub> or /WE = V <sub>IL</sub>	-1	-	1	μA	
I <sub>CC</sub>	Operating Power Supply Current	/CS = V <sub>IL</sub> , V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , I <sub>I/O</sub> = 0mA	-	-	2	mA	
I <sub>CC1</sub>	Average Operating Current	/CS = V <sub>IL</sub> , V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , Min. Duty Cycle = 100%, I <sub>I/O</sub> = 0mA	-	-	30	mA	
I <sub>CC2</sub>	Average Operating Current	/CS = V <sub>IL</sub> , V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , Cycle = 1us, I <sub>I/O</sub> = 0mA	-	-	5	mA	
I <sub>SB</sub>	TTL Standby Current (TTL Inputs)	/CS = V <sub>IH</sub> , V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	-	-	0.3	mA	
I <sub>SB1</sub>	CMOS Standby Current (CMOS Inputs)	/CS ≥ V <sub>CC</sub> - 0.2V V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ V <sub>SS</sub> + 0.2V	L	-	-	20	μA
			LL	-	-	10	μA
			LE	-	-	30	μA
			LLE	-	-	15	μA
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2.1mA	-	-	0.4	V	
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -1.0mA	2.4	-	-	V	

Note : Typical values are at V<sub>CC</sub> = 3.0V, T<sub>A</sub> = 25°C

## AC CHARACTERISTICS(I)

V<sub>CC</sub> = 3.0V ±10%, T<sub>A</sub> = 0°C to 70°C (Normal) / -25°C to 85°C (Extended) unless otherwise specified.

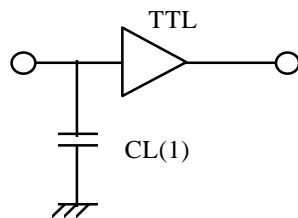
#	Symbol	Parameter	-10		-12		Unit
			Min.	Max.	Min	Max.	
<b>READ CYCLE</b>							
1	t <sub>RC</sub>	Read Cycle Time	100	-	120	-	ns
2	t <sub>AA</sub>	Address Access Time	-	100	-	120	ns
3	t <sub>ACS</sub>	Chip Select Access Time	-	100	-	120	ns
4	t <sub>OE</sub>	Output Enable to Output Valid	-	50	-	60	ns
5	t <sub>CLZ</sub>	Chip Select to Output in Low Z	10	-	10	-	ns
6	t <sub>OLZ</sub>	Output Enable to Output in Low Z	5	-	5	-	ns
7	t <sub>CHZ</sub>	Chip Disable to Output in High Z	0	35	0	40	ns
8	t <sub>OHZ</sub>	Out Disable to Output in High Z	0	35	0	40	ns
9	t <sub>OH</sub>	Output Hold from Address Change	15	-	15	-	ns
<b>WRITE CYCLE</b>							
10	t <sub>WC</sub>	Write Cycle Time	100	-	120	-	ns
11	t <sub>CW</sub>	Chip Selection to End of Write	80	-	100	-	ns
12	t <sub>AW</sub>	Address Valid to End of Write	80	-	100	-	ns
13	t <sub>AS</sub>	Address Set-up Time	0	-	0	-	ns
14	t <sub>WP</sub>	Write Pulse Width	70	-	85	-	ns
15	t <sub>WR</sub>	Write Recovery Time	0	-	0	-	ns
16	t <sub>WHZ</sub>	Write to Output in High Z	0	30	0	40	ns
17	t <sub>DW</sub>	Data to Write Time Overlap	40	-	50	-	ns
18	t <sub>DH</sub>	Data Hold from Write Time	0	-	0	-	ns
19	t <sub>OW</sub>	Output Active from End of Write	10	-	10	-	ns

## AC TEST CONDITIONS

$T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$  (Normal) /  $-25^\circ\text{C}$  to  $85^\circ\text{C}$  (Extended) unless otherwise specified.

Parameter		Value
Input Pulse Level		0.4V to 2.2V
Input Rise and Fall Time		5ns
Input and Output Timing Reference Level		1.5V
Output Load	tCLZ,tOLZ,tCHZ,tOHZ,tWHZ,tOW	CL = 5pF + 1TTL Load
	Others	CL = 100pF + 1TTL Load

## AC TEST LOADS



Note : Including jig and scope capacitance

## CAPACITANCE

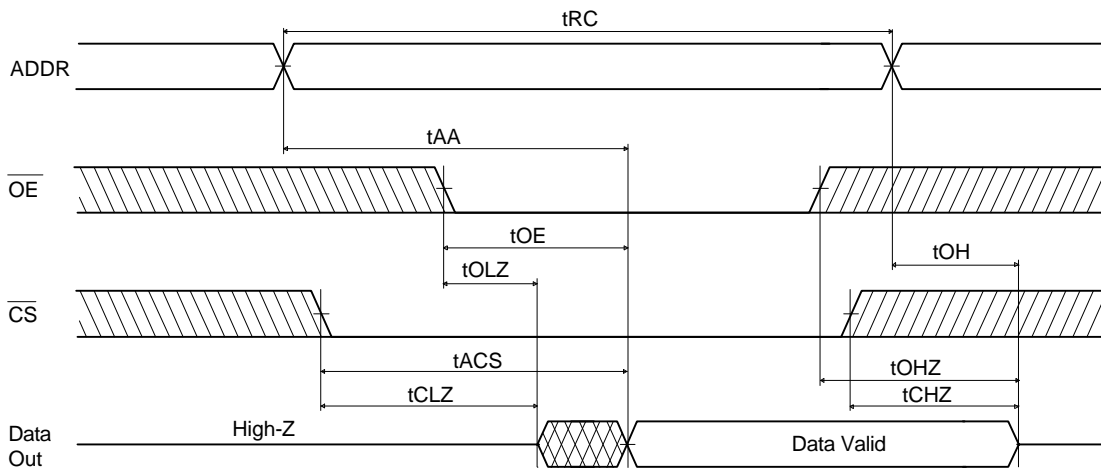
$T_A = 25^\circ\text{C}$ ,  $f = 1.0\text{MHz}$

Symbol	Parameter	Condition	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	6	pF
C <sub>I/O</sub>	Input /Output Capacitance	V <sub>I/O</sub> = 0V	8	pF

Note : These parameters are sampled and not 100% tested

## TIMING DIAGRAM

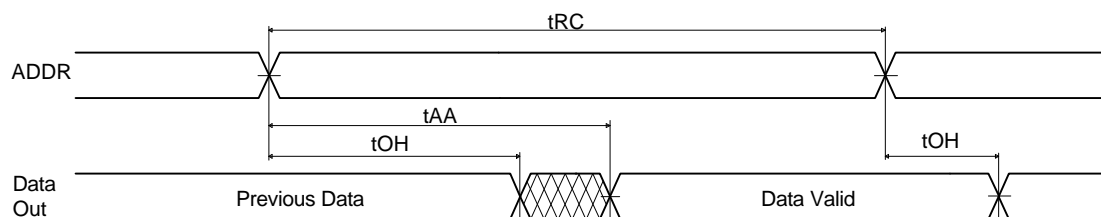
### READ CYCLE 1



Note(READ CYCLE):

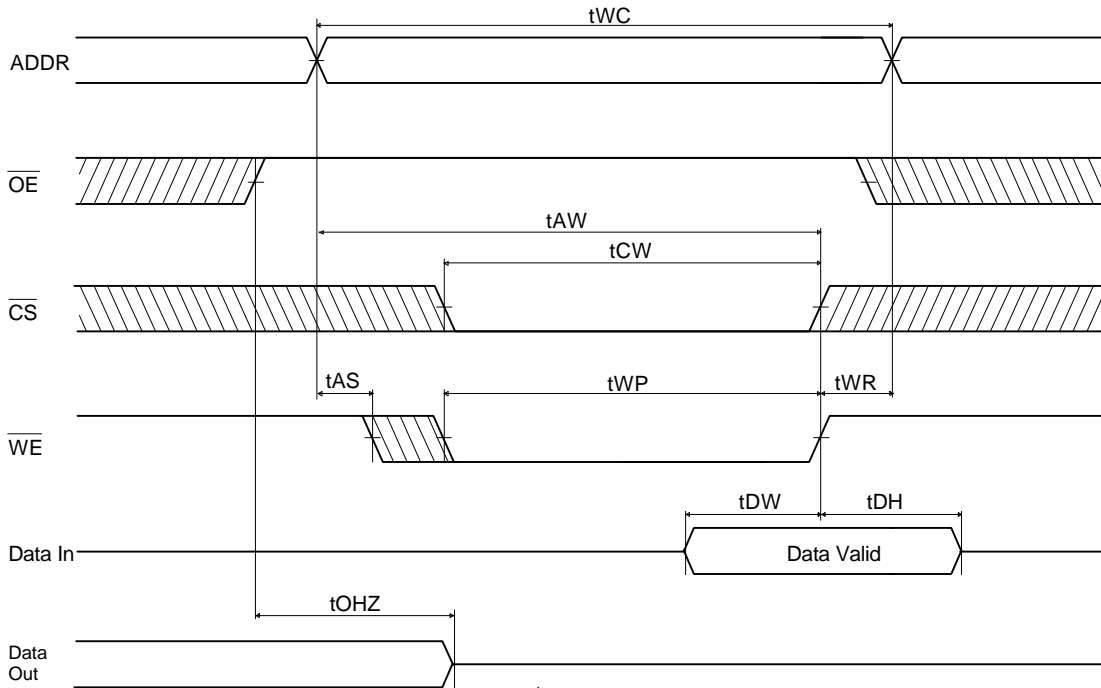
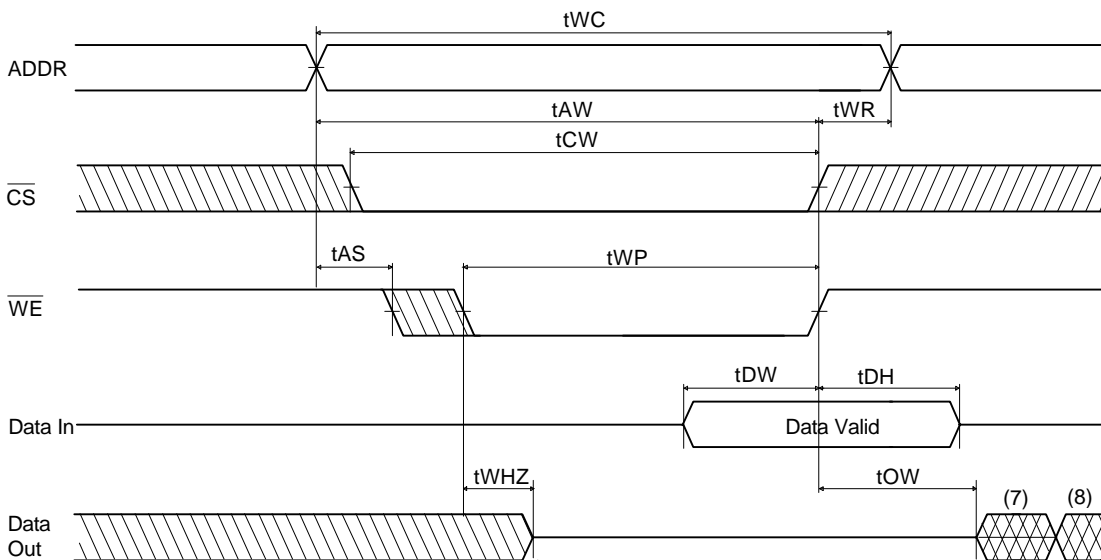
1.  $t_{CHz}$  and  $t_{OHz}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition,  $t_{CHz}$  max. is less than  $t_{CLz}$  min. both for a given device and from device to device.
3.  $\overline{WE}$  is high for the read cycle.

### READ CYCLE 2



Note(READ CYCLE):

1.  $\overline{WE}$  is high for the read cycle.
2. Device is continuously selected  $\overline{CS} = V_{IL}$ .
3.  $\overline{OE} = V_{IL}$ .

**WRITE CYCLE 1 (/OE Clocked)**

**WRITE CYCLE 2 (/OE Low Fixed)**


**Notes(WRITE CYCLE):**

1. A write occurs during the overlap of a low /CS and a low /WE. A write begins at the latest transition among /CS going low and /WE going low: A write ends at the earliest transition among /CS going high and /WE going high. tWP is measured from the beginning of write to the end of write.
2. tcw is measured from the later of /CS going low to the end of write .
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end of write to the address change. tWR is applied in case a write ends as /CS, or /WE going high.
5. If /OE and /WE are in the read mode during this period, and the I/O pins are in the output low-Z state, input of opposite phase of the output must not be applied because bus contention can occur.
6. If /CS goes low simultaneously with /WE going low, or after /WE going low, the outputs remain in high impedance state.
7. DOUT is the same phase of the latest written data in this write cycle.
8. DOUT is the read data of the new address.

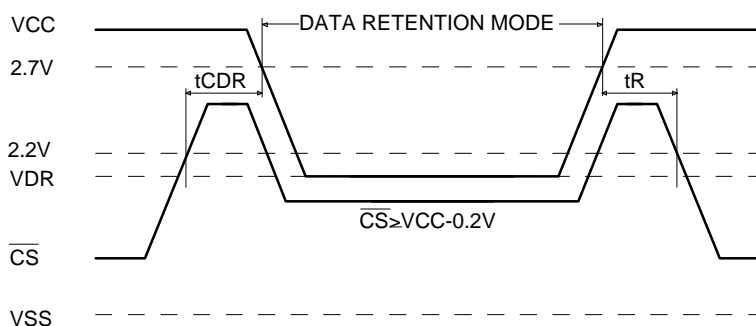
**DATA RETENTION CHARACTERISTIC**

TA=0°C to 70°C (Normal)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit	
VDR	Vcc for Data Retention	$CS \geq V_{CC} - 0.2V$ , $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq V_{SS} + 0.2V$	2.0	-	-	V	
ICCDR	Data Retention Current	$V_{CC} = 3.0V$ , $/CS \geq V_{CC} - 0.2V$ , $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq V_{SS} + 0.2V$	L	-	1	15	uA
			LL	-	0.5	7	uA
			LE	-	1	20	uA
			LLE	-	0.5	10	uA
tCDR	Chip Deselect to Data Retention Time	See Data Retention	0	-	-	ns	
tR	Operating Recovery Time	Timing Diagram	tRC(2)	-	-	ns	

**Notes**

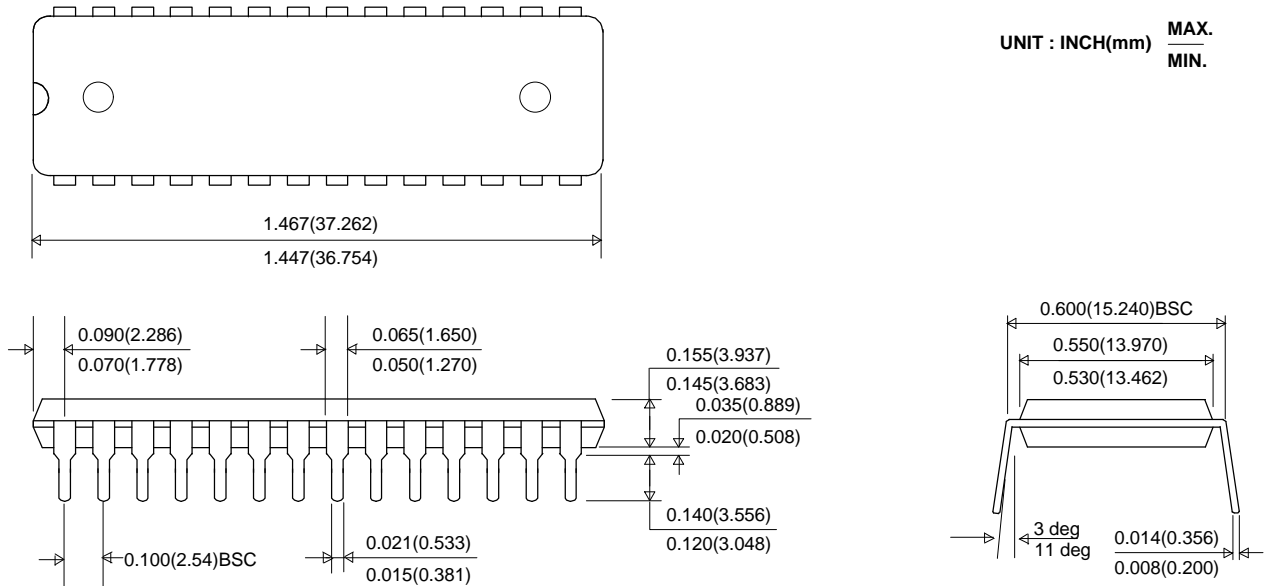
1. Typical values are under the condition of TA = 25°C.
2. tRC is read cycle time.

**DATA RETENTION TIMING DIAGRAM**


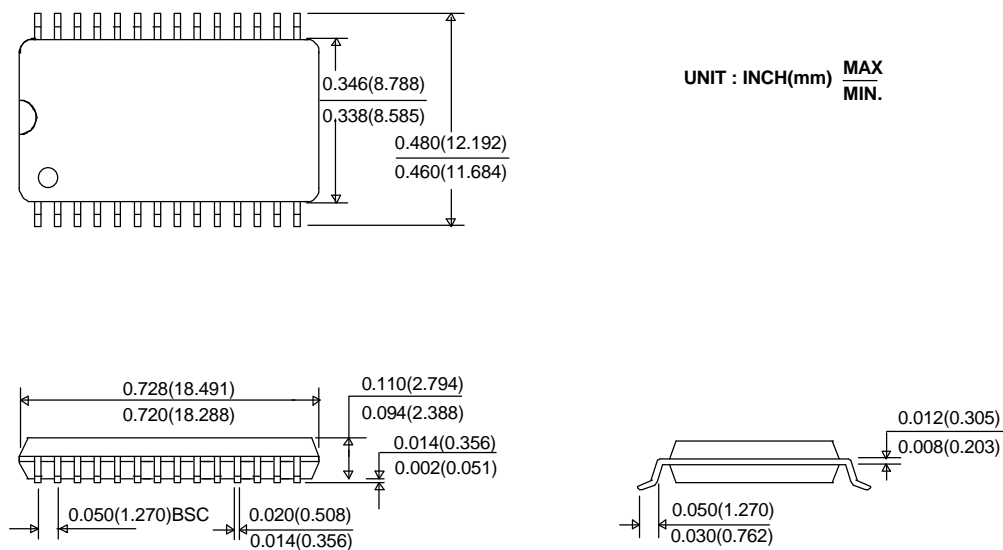


**PACKAGE INFORMATION**

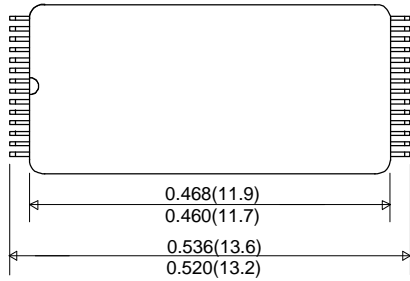
28pin 600mil Dual In-Line Package(Blank)



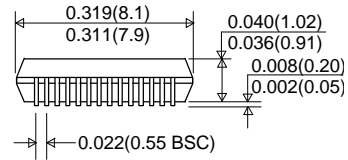
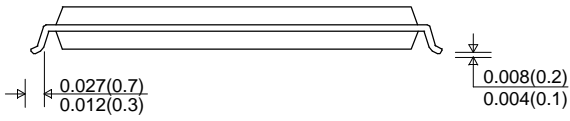
28pin 330mil Small Outline Package(FW)



28pin 8x13.4mm Thin Small Outline Package Standard(T)



UNIT : INCH(mm) <sup>MAX.</sup>  
<sub>MIN.</sub>



**MARKING INFORMATION**

Package	Marking Example																																																
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**Index**

• <b>HYUNDAI</b>	: Hynix Logo
• <b>KOREA</b>	: Origin Country
• <b>GM76U256C</b>	: Part Name
• <b>cc</b>	: Power Consumption
	- L : Low Power
	- LL : Low Low Power
• <b>Blank / FW / T</b>	: Package Type
	- Blank : DIP
	- FW : SOP
	- T : TSOP-I
• <b>ss</b>	: Speed
	- 10 : 100ns
	- 12 : 150ns
• <b>t</b>	: Temperature
	- Blank : Commercial ( 0 ~ 70 °C )
	- E : Extended ( -25 ~ 85 °C )
• <b>yy</b>	: Year ( ex : 00 = year 2000, 01 = year 2001 )
• <b>ww</b>	: Work Week ( ex : 12 = ww12 )
<b>Note</b>	
- Capital Letter	: Fixed Item
- Small Letter	: Non-fixed Item