19-4519; Rev. 0; 1/92

MAXIM

High-Speed, Positive Edge-Triggered, ECL-Compatible Voltage Comparators

General Description

The MAX905/MAX906 high-speed, single and dual ECL-compatible voltage comparators eliminate oscillation by separating the comparator input and output stages with a positive edge-triggered master-slave D flip-flop. Comparator propagation delay is typically 2ns, and is insensitive to input overdrive. The MAX905 and MAX906 resolve input signals as small as 3mV and 4mV respectively.

These comparators feature separate analog and digital ground connections for maximum noise rejection, and operate from either dual supplies or from a single supply. Input common-mode voltage range extends to the negative supply rail for a wide 7.9V input voltage range with ±5V supplies.

The MAX905 is a single ECL comparator, available in 14-pin DIP and SO packages. The MAX906 is a dual version available in 16-pin DIP and SO packages.

Applications

High-Speed A/D Converters

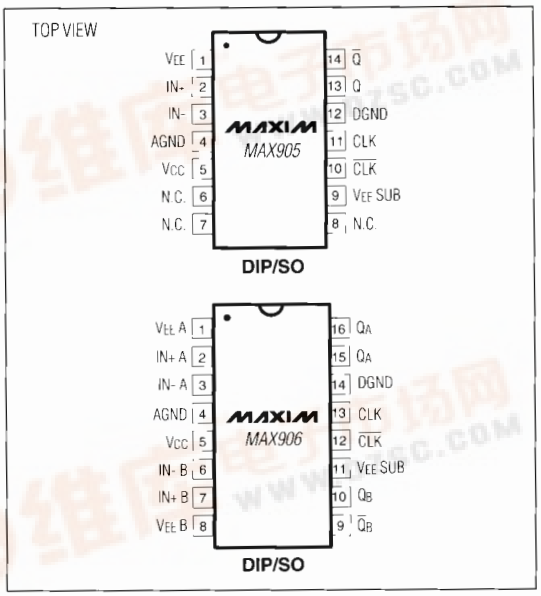
High-Speed Line Receivers

Peak Detectors

Threshold Detectors

High-Speed Triggers

Pin Configurations



Features

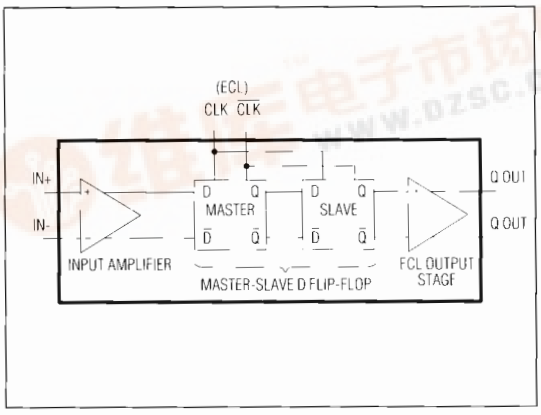
- ♦ Immune to Oscillation: Clocked Architecture
- ♦ 2ns Setup Time
- ♦ 2ns Propagation Delay
- ♦ Prop Delay Independent of Overdrive
- ♦ 3mV Input Resolution (MAX905)
- ♦ Input Range Includes Negative Supply Rail
- ♦ Single- or Dual-Supply Capability
- ♦ Separate Analog and Digital Supplies
- ♦ Low Power: 180mW/Comparator

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX905CPD	0°C to +70°C	14 Plastic DIP
MAX905CSD	0°C to +70°C	14 Narrow SO
MAX905C/D	0°C to +70°C	Dice*
MAX905EPD	-40°C to +85°C	14 Plastic DIP
MAX905ESD	-40°C to +85°C	14 Narrow SO
MAX905MJD	-55°C to +125°C	14 CERDIP
MAX906CPE	0°C to +70°C	16 Plastic DIP
MAX906CSE	0°C to +70°C	16 Narrow SO
MAX906C/D	0°C to +70°C	Dice*
MAX906EPE	-40°C to +85°C	16 Plastic DIP
MAX906ESE	-40°C to +85°C	16 Narrow SO

*Contact factory for dice specifications.

Functional Diagram



High-Speed, Positive Edge-Triggered, ECL-Compatible Voltage Comparators

ABSOLUTE MAXIMUM RATINGS

Analog Supply Voltage (V_{CC} to V_{EE}) ..... +12V
Digital Supply Voltage (V_{EE} to GND) ..... -6V
Differential Input Voltage ..... (V_{EE} - 0.2V) to (V_{CC} + 0.2V)
Common-Mode Input Voltage .... (V_{EE} - 0.2V) to (V_{CC} + 0.2V)
Clock Input Voltage (CLK or $\overline{CLK}$) .. (V_{EE} - 0.2V) to DGND + 0.2V
Output Current (Q or $\overline{Q}$) 30mA
Output Short-Circuit Duration (Q or $\overline{Q}$ to GND) ..... Indefinite
Continuous Power Dissipation
MAX905 DIP (derate 10.00mW/°C above +70°C) 800mW
SO (derate 8.00mW/°C above +70°C) 640mW
CERDIP (derate 9.09mW/°C above +70°C) ... 727mW
MAX906 DIP (derate 10.53mW/°C above +70°C) 842mW
SO (derate 8.70mW/°C above +70°C) 696mW

Operating Temperature Ranges:
MAX90_C_ _ ..... 0°C to +70°C
MAX90_E_ _ ..... -40°C to +85°C
MAX90_MJD ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... -65°C to +170°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = -5V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	V_{CM} = 0V	MAX905		0.5	1.0	mV
			MAX906		0.5	1.5	
Input Bias Current	I_B	I_{B+} or I_{B-}			4	10	µA
Input Offset Current	I_{OS}	V_{CM} = 0V			0.1	1.0	µA
Input Referred Noise Voltage	e_n	(Note 1)			600	900	µV
Input Common-Mode Range	V_{CM}	(Note 2)		V_{EE} - 0.1		V_{CC} - 2.2	V
Common-Mode Rejection Ratio	CMRR	Over V_{CM} range	MAX905		60	120	µV/V
			MAX906		60	180	
Power-Supply Rejection Ratio	PSRR	(Note 3)			60	120	µV/V
Output High Voltage	V_{OH}	(Note 4)		-0.96		-0.81	V
Output Low Voltage	V_{OL}	(Note 4)		-1.85		-1.65	V
Clock Input Voltage High	V_{CH}			-0.96		0	V
Clock Input Voltage Low	V_{CL}			-2.00		-1.65	V
Clock Input Current High	I_{CH}					50	µA
Clock Input Current Low	I_{CL}					50	µA
Positive Supply Current	I_{CC}	(Note 5)	MAX905		5	8	mA
			MAX906		10	16	
Negative Supply Current	I_{EE}	(Note 5)	MAX905		18	24	mA
			MAX906		36	48	
Power Dissipation	PD	(Notes 5, 6)	MAX905		180	260	mW
			MAX906		360	520	
Positive Propagation Delay	t_{PD+}	(Notes 7, 8)			1.8	3.5	ns
Negative Propagation Delay	t_{PD-}	(Notes 7, 8)			1.8	3.5	ns
Clock Setup Time	t_S	V_{OD} = 5mV (Note 8)			2.0		ns
		V_{OD} = 10mV (Notes 7, 8)			1.5	3.0	

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = -5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	V_{CM} = 0V	MAX905C		0.5	1.5	mV
			MAX905E/M		0.5	2.5	
			MAX906C		0.5	2.5	
			MAX906E/M		0.5	3.5	
Input Bias Current	I_B	I_{B+} or I_{B-}			6	15	µA
Input Offset Current	I_{OS}	V_{CM} = 0V			0.2	2.0	µA
Input Referred Noise Voltage	e_n	(Note 1)			600	900	µV
Input Common-Mode Range	V_{CM}	(Note 2)		V_{EE} - 0.1		V_{CC} - 2.2	V
Common-Mode Rejection Ratio	CMRR				80	180	µV/V
Power-Supply Rejection Ratio	PSRR	(Note 3)			70	150	µV/V
Output High Voltage (Note 4)	V_{OH}	T_A = -55°C		-1.11		-0.93	V
		T_A = -40°C		-1.08		-0.91	
		T_A = 0°C		-1.01		-0.85	
		T_A = +70°C		-0.90		-0.72	
		T_A = +85°C		-0.89		-0.70	
		T_A = +125°C		-0.85		-0.63	
Output Low Voltage (Note 4)	V_{OL}	T_A = -55°C		-1.90		-1.69	V
		T_A = -40°C		-1.90		-1.68	
		T_A = 0°C		-1.87		-1.66	
		T_A = +70°C		-1.83		-1.62	
		T_A = +85°C		-1.83		-1.62	
		T_A = +125°C		-1.80		-1.60	
Clock Input Voltage High	V_{CH}			-1.11		0	V
Clock Input Voltage Low	V_{CL}			-2.00		-1.60	V
Clock Input Current High	I_{CH}					50	µA
Clock Input Current Low	I_{CL}					50	µA
Positive Supply Current	I_{CC}	(Note 5)	MAX905		6	10	mA
			MAX906		12	20	
Negative Supply Current	I_{EE}	(Note 5)	MAX905		23	32	mA
			MAX906		46	64	
Power Dissipation	PD	(Notes 5, 6)	MAX905		220	320	mW
			MAX906		440	640	
Positive Propagation Delay	t_{PD+}	(Notes 7, 8)			2.0	4.0	ns
Negative Propagation Delay	t_{PD-}	(Notes 7, 8)			2.0	4.0	ns
Clock Setup Time	t_S	V_{OD} = 10mV (Notes 7, 8)			2.0	4.0	ns

Note 1: Guaranteed by design. Input Referred Noise Voltage uncertainty is specified over the full bandwidth of the device.
Note 2: The input common-mode voltage or either input signal voltage should not be allowed to go more than 0.2V below V_{EL}. The upper input common-mode range limit is typically V_{CC} - 2V, but either input can go to V_{CC} + 0.2V without damage.
Note 3: Tested for +4.75V < V_{CC} < +5.25V and -5.50V < V_{EE} < -4.75V.
Note 4: Tested with R_{LOAD} = 50Ω terminated in -2V.
Note 5: I_{CC}, I_{EE} and PD tested for worst-case condition of V_{CC} = +5.25V and V_{EE} = -5.5V.
Note 6: Includes internal power dissipation due to external load resistors.
Note 7: Guaranteed by design. Measured in a high-speed fixture with R_{LOAD} = 50Ω, and C_{LOAD} = 15pF, terminated into -2V.
Note 8: Clock input voltage rise and fall times should not exceed 50ns for correct triggering of comparator.

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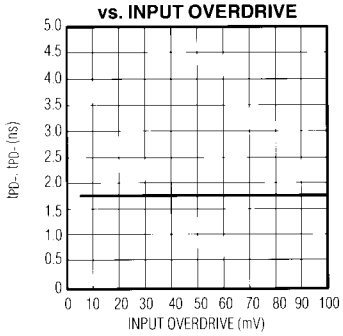
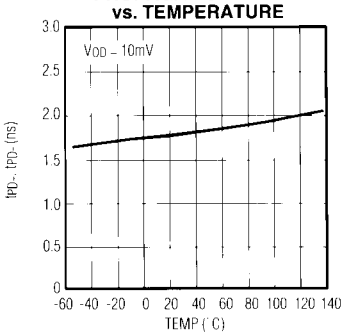
Typical Operating Characteristics

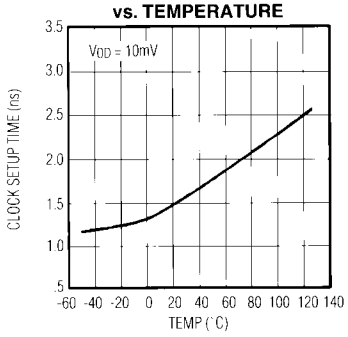
PROPAGATION DELAY vs. INPUT OVERDRIVE



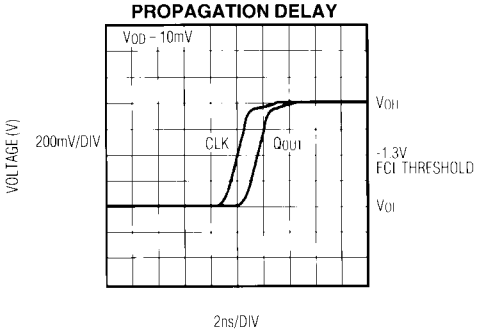
PROPAGATION DELAY vs. TEMPERATURE



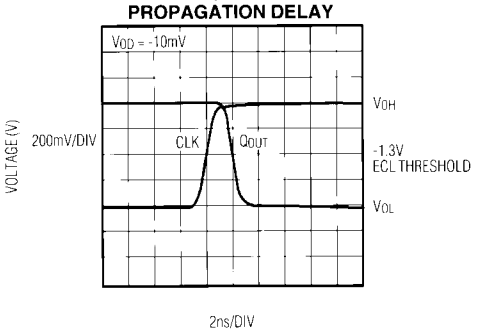
CLOCK SETUP TIME vs. TEMPERATURE



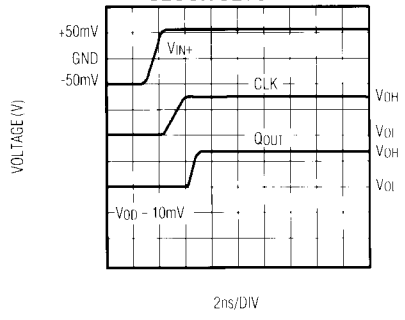
POSITIVE PROPAGATION DELAY



NEGATIVE PROPAGATION DELAY

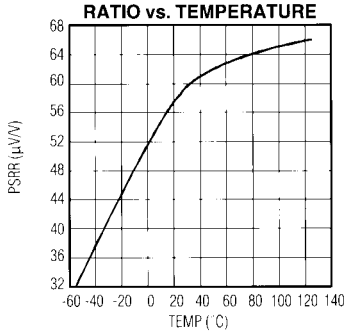


CLOCK SETUP TIME

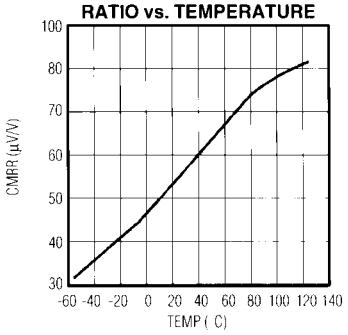


Typical Operating Characteristics (continued)

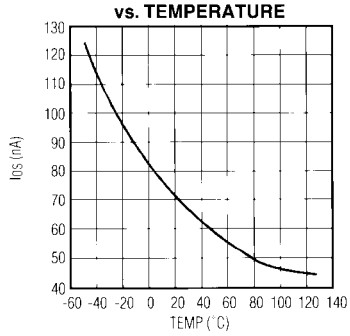
POWER-SUPPLY REJECTION RATIO vs. TEMPERATURE



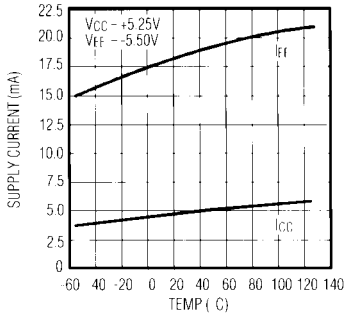
COMMON-MODE REJECTION RATIO vs. TEMPERATURE



INPUT OFFSET CURRENT vs. TEMPERATURE



SUPPLY CURRENT PER COMPARATOR vs. TEMPERATURE



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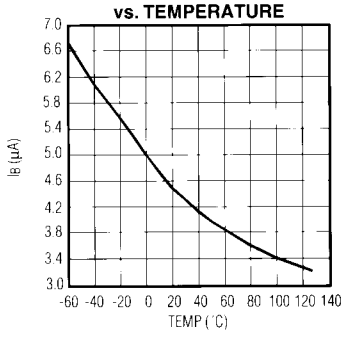
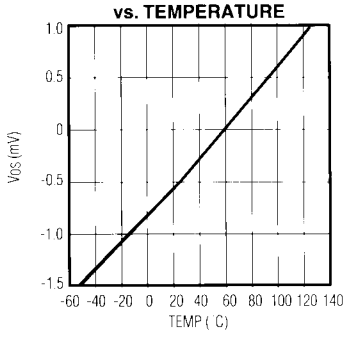
Typical Operating Characteristics (continued)

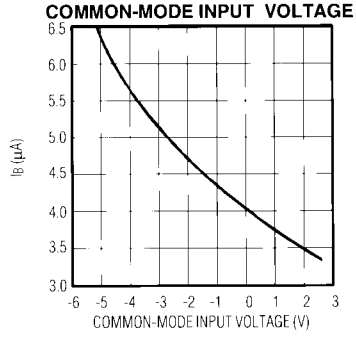
INPUT BIAS CURRENT vs. TEMPERATURE



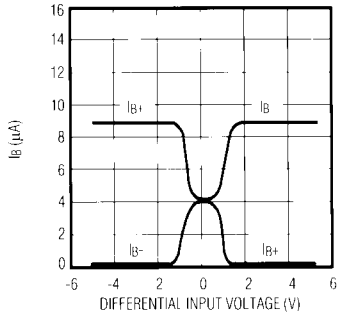
INPUT OFFSET VOLTAGE vs. TEMPERATURE



INPUT BIAS CURRENT vs. COMMON-MODE INPUT VOLTAGE



INPUT BIAS CURRENT vs. DIFFERENTIAL INPUT VOLTAGE



High-Speed, Positive Edge-Triggered, ECL-Compatible Voltage Comparators

Pin Description

MAX905

PIN	NAME	FUNCTION
1	V_{EE}	Negative Digital Supply
2	IN+	Positive Input
3	IN-	Negative Input
4	AGND	Analog Ground Terminal
5	V_{CC}	Positive Analog Supply
6,7,8	N.C.	No Connect
9	V_{EE} SUB	Negative Analog Supply
10	$\overline{CLK}$	Negative ECL Clock Input
11	CLK	Positive ECL Clock Input
12	DGND	Digital Ground Terminal
13	Q	Positive ECL Output
14	$\overline{Q}$	Negative ECL Output

MAX906

PIN	NAME	FUNCTION
1	$V_{EE}A$	Negative Digital Supply (Channel A)
2	IN+ A	Positive Input (Channel A)
3	IN- A	Negative Input (Channel A)
4	AGND	Analog Ground Terminal
5	V_{CC}	Positive Analog Supply
6	IN- B	Negative Input (Channel B)
7	IN+ B	Positive Input (Channel B)
8	$V_{EE}B$	Negative Digital Supply (Channel B)
9	Q_B	Negative ECL Output (Channel B)
10	$\overline{Q_B}$	Positive ECL Output (Channel B)
11	V_{EE} SUB	Negative Analog Supply
12	$\overline{CLK}$	Negative ECL Clock Input
13	CLK	Positive ECL Clock Input
14	DGND	Digital Ground Terminal
15	Q_A	Positive ECL Output (Channel A)
16	$\overline{Q_A}$	Negative ECL Output (Channel A)

Device Overview

The MAX905 (single) and MAX906 (dual) are ultra high-speed ECL-compatible comparators with an internal positive edge-triggered master-slave D flip-flop. Unlike industry-standard ECL comparators, this architecture breaks the input-to-output signal path to accomplish the following:

1) Prevent oscillations caused by unwanted parasitic feedback when the comparator is in its linear region. No minimum input slew rate is required.

2) Propagation delay remains constant with varying input overdrive.

Detailed Description

The comparator can be divided into three stages, as shown in Figure 1:

1) Input Amplifier

2) Master-Slave D Flip-Flop

3) ECL Output Stage

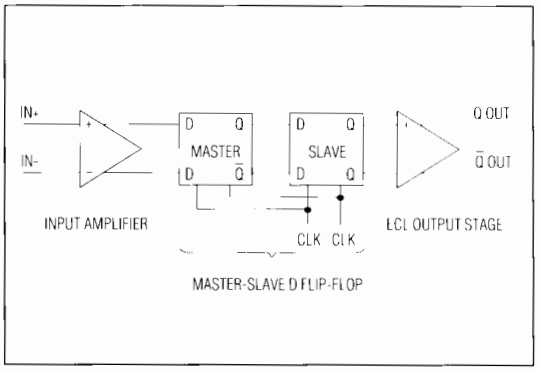


Figure 1. MAX905/MAX906 Block Diagram

Input Amplifier

The comparator input amplifier is fully differential. Input offset voltage is trimmed to less than 1.0mV for the MAX905, and less than 1.5mV for the MAX906. Input common-mode range extends from 100mV below the negative supply rail (V_{EE}) to 2.2V below the positive supply rail (V_{CC}). Total input voltage range is 7.9V when operating from ±5V supplies.

The master-slave architecture enables the MAX905 to compare input signals down to 3mV over its entire common-mode range. Similarly, the MAX906 compares input signals as low as 4mV (see Table 1). Any input signal less than 3mV (4mV for MAX906) may not be distinguished from the comparator's total worst-case DC error. The MAX905/MAX906 total worst-case DC error is calculated by summing input offset voltage (V_{OS}), input referred noise (e_n), common-mode rejection ratio (CMRR), and power-supply rejection ratio (PSRR). Table 1 shows the maximum total input referred error at +25°C and over temperature. For many applications, take the RMS summation of the individual errors for a more meaningful representation of the total input referred error (see Table 2).

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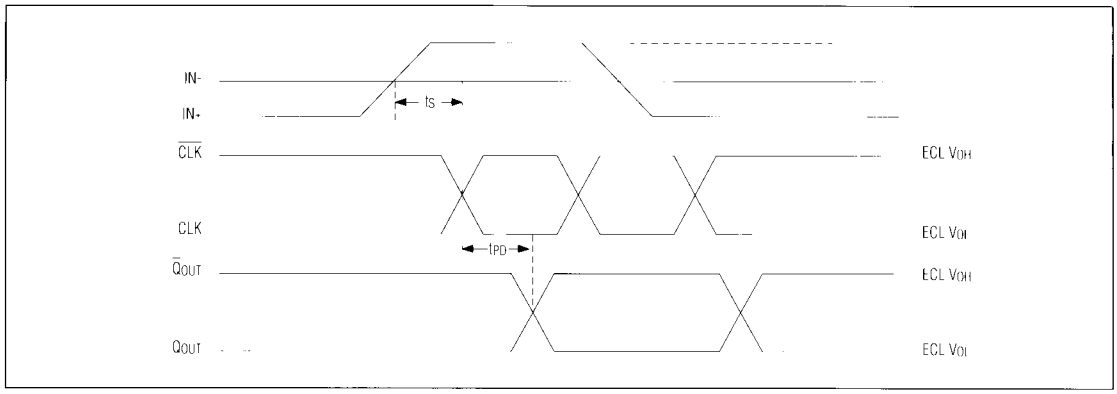


Figure 2. Timing Diagram

Table 1. Total Worst-Case Input Referred Error/Resolution

Part	+25°C (mV)	Commercial Temp. (mV)	Ext. Ind/Military Temp. (mV)
MAX905	3	4	5
MAX906	4	5	6

Table 2. Total RMS Input Referred Error/Resolution

Part	+25°C (mV)	Commercial Temp. (mV)	Ext. Ind/Military Temp. (mV)
MAX905	1.7	2.3	3.0
MAX906	2.3	3.0	3.9

Master-Slave D Flip-Flop

The master-slave D flip-flop is immune to metastability by design, and propagation delay is independent of input overdrive (V_{OD}). The MAX905/MAX906 master flip-flop has an input stage that samples the output of the input amplifier and a latch to hold the sampled data when the master input stage is disabled. The latched data is transferred to the MAX905/MAX906 slave flip-flop only on the clock's rising edge. The input amplifier continuously monitors the input signal.

Clock Cycle

Clock Low: When the clock is low, the master flip-flop's input stage samples the output of the input amplifier. The slave flip-flop maintains valid outputs from the previously sampled data. The comparator inputs are isolated from the comparator outputs because the slave flip-flop's input stage is disabled. See Figure 2.

Clock Rising Edge: On the rising edge of the clock, the master flip-flop input stage turns off and the latch holds the sampled data. Shortly after, the slave input stage turns on and samples the outputs of the master. The ECL output stage simultaneously receives data from the slave.

Clock High: The slave flip-flop continues to sample data from the master while the clock is high. The master flip-flop latch holds data from the previous rising clock edge.

Clock Falling Edge: On the falling edge of the clock, data from the previous rising clock edge is latched into the slave, and the input of the master flip-flop is turned on. New data is not transferred to the ECL output stage on the falling edge of the clock cycle.

ECL Output Stage

The ECL output stage receives data from the slave flip-flop. Proper ECL output voltage levels and temperature coefficients are maintained by the output amplifier over commercial, extended industrial, and military temperature ranges. The comparator's outputs (Q and Q) are fully differential and MECL 10k compatible.

Applications Information

Maximum Clock Rate

The MAX905/MAX906 maximum clock frequency is a direct function of the comparator's minimum clock setup time. Typical clock setup time is 2ns, which translates to a theoretical 500MHz maximum clock frequency. As shown in Figure 3, the maximum output toggle rate is 1/2 the clock frequency, because the comparator triggers only on the rising edge of each clock cycle.

For proper clock triggering, the MAX905/MAX906 ECL clock rise and fall times must be less than 50ns. If clock rise/fall times are greater than 50ns, the comparator may incorrectly sample the input signal at the clock's falling edge.

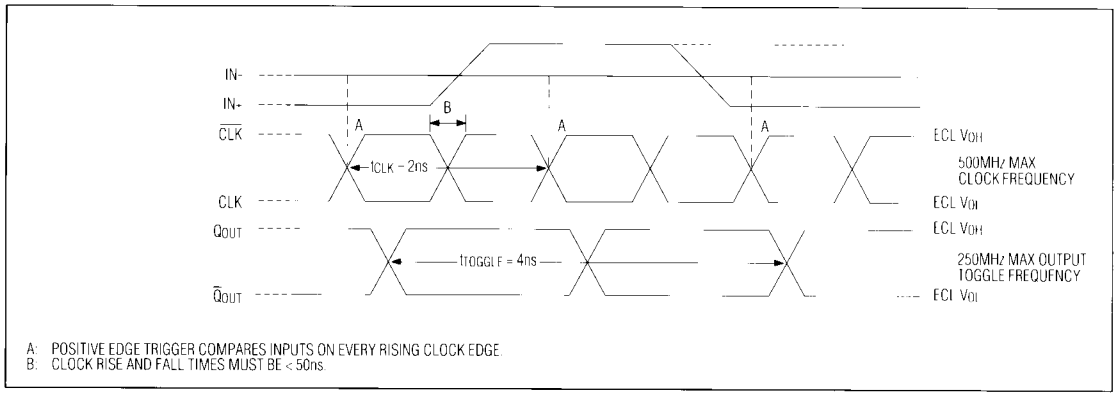


Figure 3. Maximum Clock Rate Timing Diagram

Power Supplies

The MAX905/MAX906 are tested while operating from ±5V supplies. The comparators also operate from standard ECL +5V and -5.2V power supplies with the same guaranteed performance.

In high-speed, mixed-signal applications where a common ground is shared, a noisy digital environment can adversely affect the integrity of the analog input signal. The MAX905/MAX906 isolate the analog and digital signals by providing separate analog (AGND) and digital (DGND) grounds. For applications that cannot separate analog and digital grounds, AGND and DGND may be tied together if a good ground plane is available.

The MAX905/MAX906 offer the unique ability to operate from a single supply. The comparators' input common-mode voltage range includes the negative supply rail. Figure 4 shows the two supply voltage conditions:

1) Dual ±5V Supplies (or +5V and -5.2V)

2) Single -5V Supply (or -5.2V)

Input Slew Rate

The MAX905/MAX906's master-slave architecture eliminates the minimum input slew-rate requirement common to standard comparator architectures. As long as the comparator is clocked after the minimum data-to-clock setup time requirement, and the input is greater

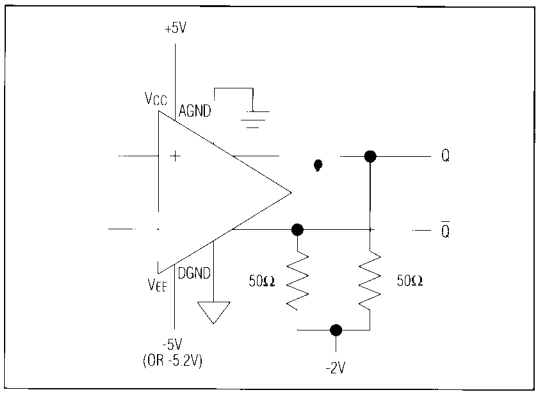


*Figure 4a. ±5V Supplies, Separate Ground**

** Separate ground is optional. DGND and AGND may be tied together.*

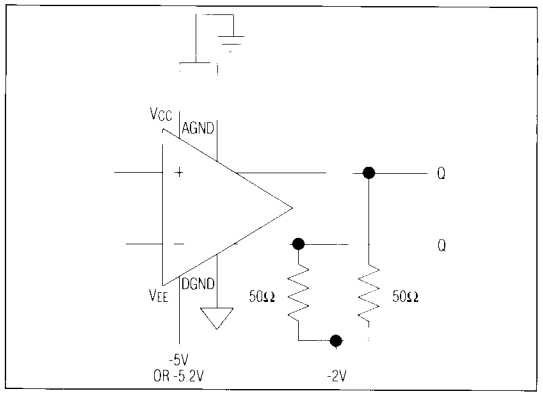


*Figure 4b. Single -5V Supply, Separate Ground**

High-Speed, Positive Edge-Triggered, ECL-Compatible Voltage Comparators

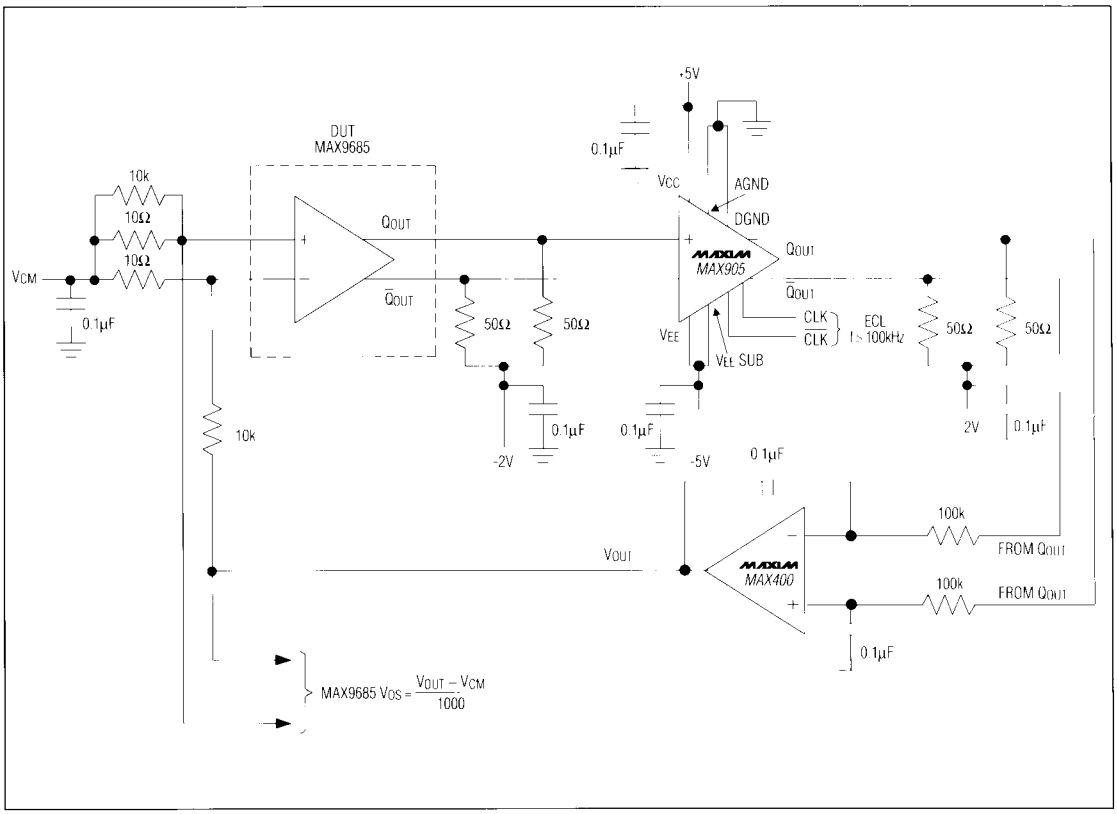


Figure 5. High-Speed Comparator V_{OS} Measurement Circuit

than the comparator's total DC error, the output data will be valid without oscillations.

Board Layout

As with all high-speed components, careful high-speed board layout and bypassing are essential for optimal performance. A printed circuit board with low inductance and separate digital and analog grounds is recommended. All decoupling capacitors should be mounted as close to the comparator power-supply pins as possible, with ground return lead lengths as short as possible. Pay close attention to the bandwidth of the decoupling and terminating components. Soldering the MAX905/MAX906 and other components directly to the board without sockets minimizes unwanted parasitic capacitance.

Typical Application

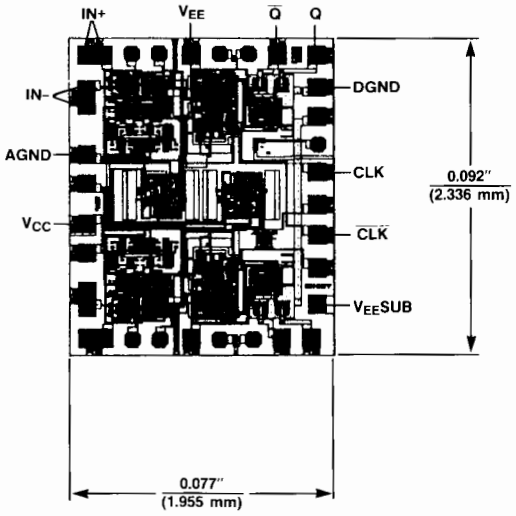
High-Speed Comparator V_{OS} Measurement Circuit: The circuit of Figure 5 shows the MAX905 used to measure input offset voltage (V_{OS}) of the MAX9685, an ultra high-speed ECL comparator. When the MAX9685 comparator is put into a standard op-amp test loop, its high-frequency open-loop gain causes oscillations. However, in this application, the MAX9685's output feeds into the MAX905, which then feeds into a differential integrator. The MAX905's D flip-flop architecture breaks the feedback path that normally causes oscillations. The test loop forces the MAX9685's output to switch with a precise 50% duty cycle, thus

$$V_{OS} = \frac{V_{OUT} - V_{CM}}{1000}$$

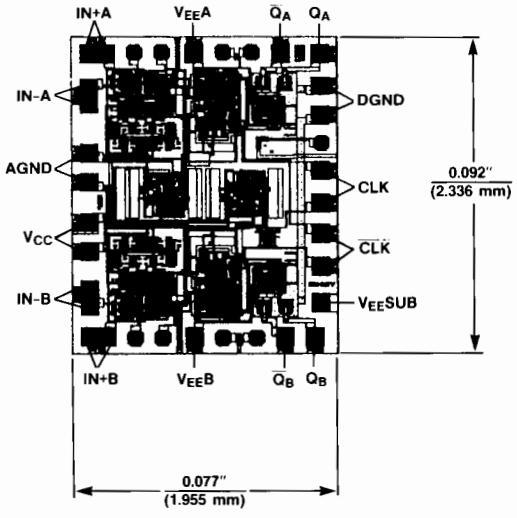
High-Speed, Positive Edge-Triggered, ECL-Compatible Voltage Comparators

Chip Topographies

MAX905

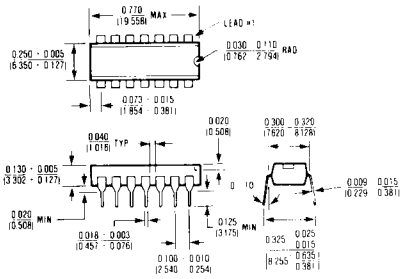


MAX906

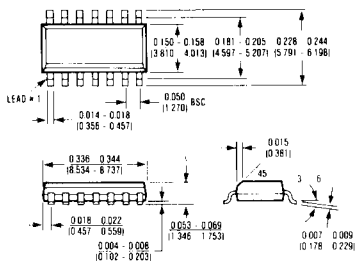


High-Speed, Positive Edge-Triggered, ECL-Compatible Voltage Comparators

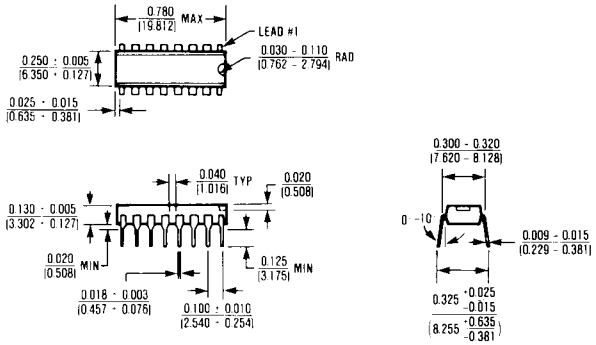
Package Information



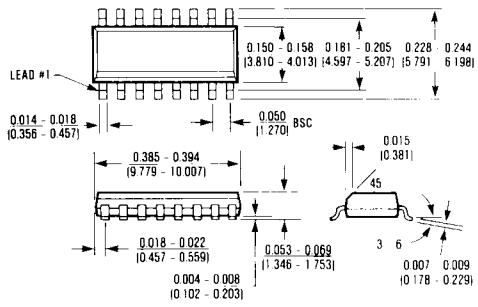
14 Lead Plastic DIP
θ_{JA} = 140 C/W
θ_{JC} = 70 C/W



14 Lead Small Outline
θ_{JA} = 115 C/W
θ_{JC} = 60 C/W



16 Lead Plastic DIP
θ_{JA} = 135°C/W
θ_{JC} = 65°C/W



16 Lead Small Outline
θ_{JA} = 110 C/W
θ_{JC} = 60 C/W