PCB · **SN54ABT646, SN74ABT646**
# OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS
SCBS068E – JULY 1991 – REVISED JULY 1994

- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical $V_{OLP}$ (Output Ground Bounce) < 1 V at $V_{CC}$ = 5 V, $T_A$ = 25°C**
- **High-Drive Outputs (−32-mA $I_{OH}$, 64-mA $I_{OL}$)**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Plastic (NT) and Ceramic (JT) DIPs**

**SN54ABT646 . . . JT PACKAGE**
**SN74ABT646 . . . DB, DW, NT, OR PW PACKAGE**
**(TOP VIEW)**

| | | |
|---|---|---|
| CLKAB | 1 | 24 | $V_{CC}$ |
| SAB | 2 | 23 | CLKBA |
| DIR | 3 | 22 | SBA |
| A1 | 4 | 21 | $\overline{OE}$ |
| A2 | 5 | 20 | B1 |
| A3 | 6 | 19 | B2 |
| A4 | 7 | 18 | B3 |
| A5 | 8 | 17 | B4 |
| A6 | 9 | 16 | B5 |
| A7 | 10 | 15 | B6 |
| A8 | 11 | 14 | B7 |
| GND | 12 | 13 | B8 |

**SN54ABT646 . . . FK PACKAGE**
**(TOP VIEW)**



NC – No internal connection

## description

These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the ′ABT646.

Output-enable ($\overline{OE}$) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both.

The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The direction control (DIR) determines which bus will receive data when $\overline{OE}$ is low. In the isolation mode ($\overline{OE}$ high), A data may be stored in one register and/or B data may be stored in the other register.
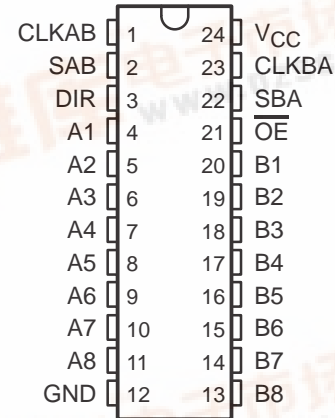
When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.
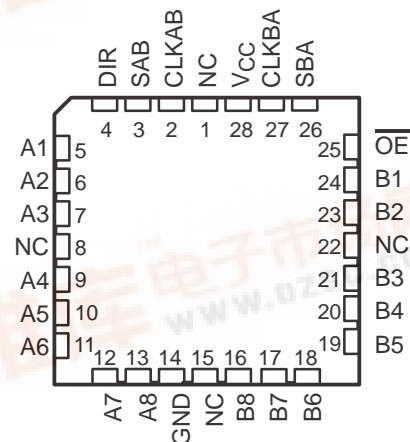
The SN74ABT646 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT646 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ABT646 is characterized for operation from −40°C to 85°C.

**TEXAS INSTRUMENTS**

| 21 | 3 | 1 | 23 | 2 | 22 |
|----|----|----|----|----|----|
| $\overline{OE}$ | DIR | CLKAB | CLKBA | SAB | SBA |
| L | L | X | X | X | L |

**REAL-TIME TRANSFER**
**BUS B TO BUS A**

| 21 | 3 | 1 | 23 | 2 | 22 |
|----|----|----|----|----|----|
| $\overline{OE}$ | DIR | CLKAB | CLKBA | SAB | SBA |
| L | H | X | X | L | X |

**REAL-TIME TRANSFER**
**BUS A TO BUS B**

| 21 | 3 | 1 | 23 | 2 | 22 |
|----|----|----|----|----|----|
| $\overline{OE}$ | DIR | CLKAB | CLKBA | SAB | SBA |
| X | X | ↑ | X | X | X |
| X | X | X | ↑ | X | X |
| H | X | ↑ | ↑ | X | X |

**STORAGE FROM**
**A, B, OR A AND B**

| 21 | 3 | 1 | 23 | 2 | 22 |
|----|----|----|----|----|----|
| $\overline{OE}$ | DIR | CLKAB | CLKBA | SAB | SBA |
| L | L | X | L | X | H |
| L | H | L | X | H | X |

**TRANSFER STORED DATA**
**TO A AND/OR B**
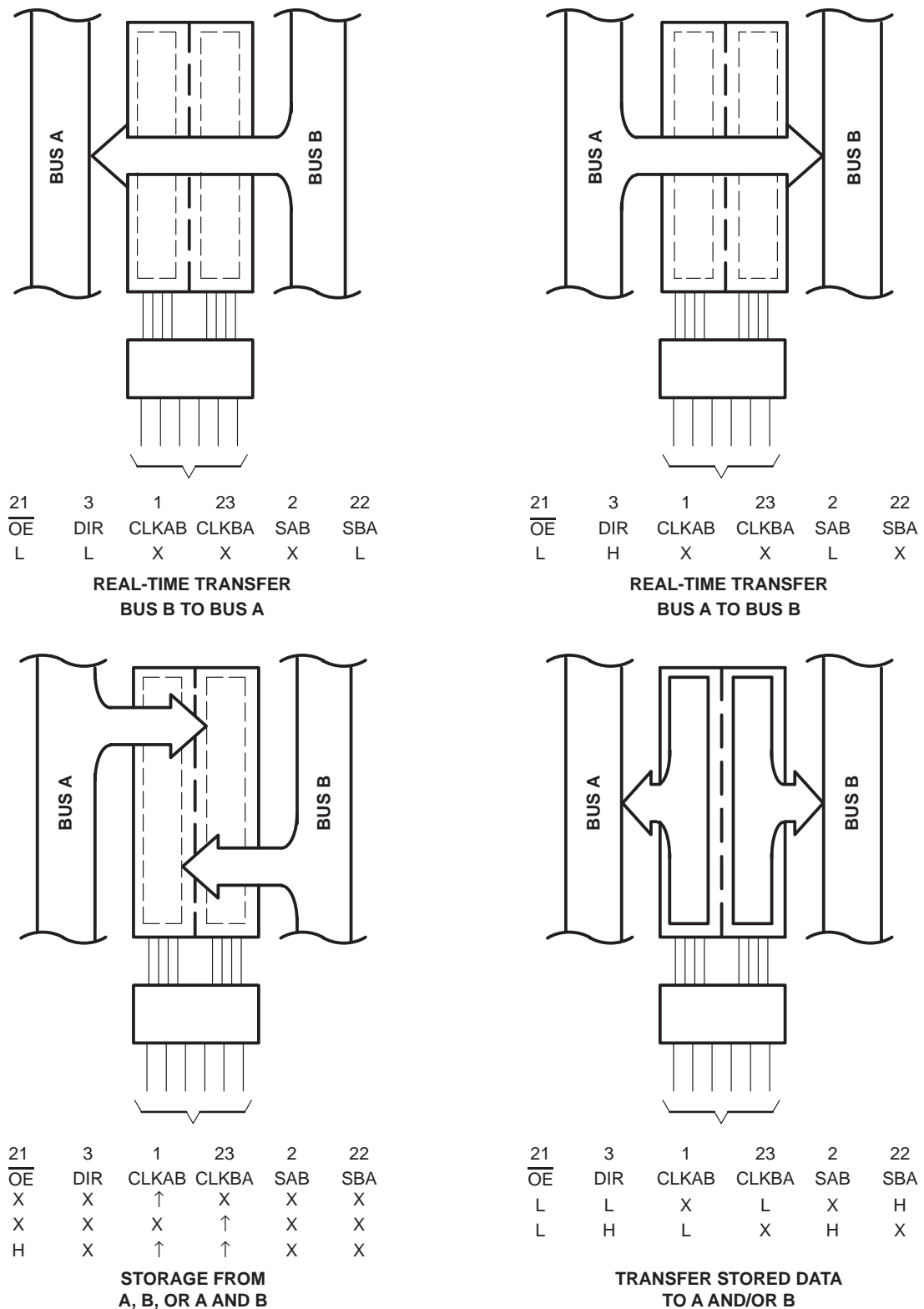
**Figure 1. Bus-Management Functions**

Pin numbers shown are for DB, DW, JT, NT, and PW packages.

TEXAS
INSTRUMENTS

**FUNCTION TABLE**

| INPUTS | | | | | | DATA I/Os | | OPERATION OR FUNCTION |
|---|---|---|---|---|---|---|---|---|
| $\overline{OE}$ | DIR | CLKAB | CLKBA | SAB | SBA | A1 THRU A8 | B1 THRU B8 | |
| X | X | ↑ | X | X | X | Input | Unspecified[†] | Store A, B unspecified[†] |
| X | X | X | ↑ | X | X | Unspecified[†] | Input | Store B, A unspecified[†] |
| H | X | ↑ | ↑ | X | X | Input | Input | Store A and B data |
| H | X | H or L | H or L | X | X | Input disabled | Input disabled | Isolation, hold storage |
| L | L | X | X | X | L | Output | Input | Real-time B data to A bus |
| L | L | X | H or L | X | H | Output | Input | Stored B data to A bus |
| L | H | X | X | L | X | Input | Output | Real-time A data to B bus |
| L | H | H or L | X | H | X | Input | Output | Stored A data to B bus |

[†] The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs.
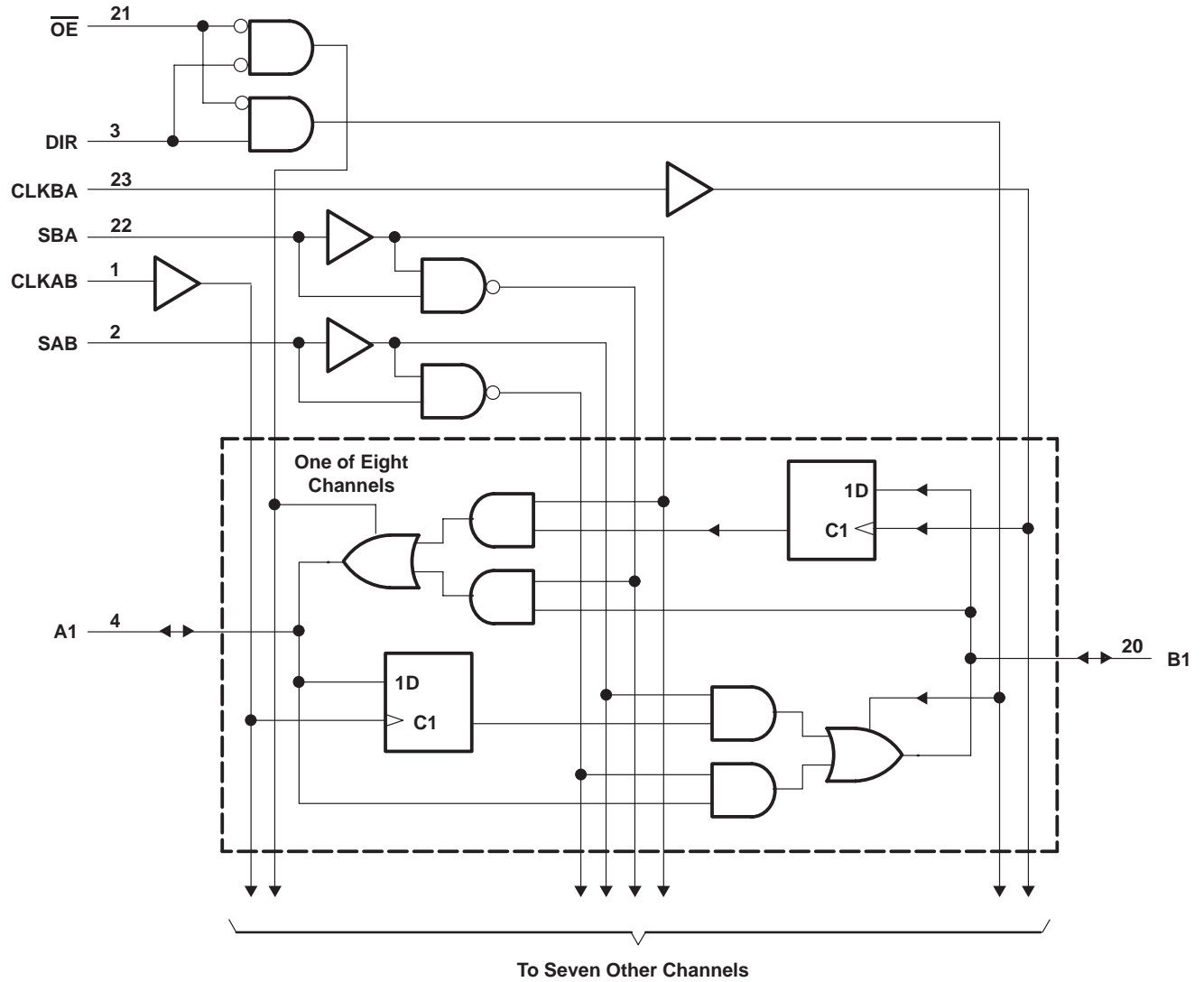
## logic symbol[‡]



[‡] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DB, DW, JT, NT, and PW packages.

## logic diagram (positive logic)



Pin numbers shown are for the DB, DW, JT, NT, and PW packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ................................................................. −0.5 V to 7 V
Input voltage range, $V_I$ (except I/O ports) (see Note 1) .................................... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, $V_O$ ............. −0.5 V to 5.5 V
Current into any output in the low state, $I_O$: SN54ABT646 .................................... 96 mA
                                              SN74ABT646 .................................... 128 mA
Input clamp current, $I_{IK}$ ($V_I < 0$) ......................................................... −18 mA
Output clamp current, $I_{OK}$ ($V_O < 0$) ...................................................... −50 mA
Maximum power dissipation at $T_A$ = 55°C (in still air) (see Note 2): DB package .................... 0.65 W
                                                             DW package .................... 1.7 W
                                                             NT package .................... 1.3 W
                                                             PW package .................... 0.7 W
Storage temperature range ................................................................. −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
          2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the NT package, which has a trace length of zero. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

## recommended operating conditions (see Note 3)

| | | SN54ABT646 | | SN74ABT646 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | −24 | | −32 | mA |
| $I_{OL}$ | Low-level output current | | 48 | | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 5 | | 5 | ns/V |
| $T_A$ | Operating free-air temperature | −55 | 125 | −40 | 85 | °C |

NOTE 3: Unused or floating pins (input or I/O) must be held high or low.

**TEXAS**
**INSTRUMENTS**

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | $T_A = 25°C$ | | | SN54ABT646 | | SN74ABT646 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | |
| $V_{IK}$ | $V_{CC} = 4.5$ V, $I_I = -18$ mA | | | | −1.2 | | −1.2 | | −1.2 | V |
| $V_{OH}$ | $V_{CC} = 4.5$ V, $I_{OH} = -3$ mA | | 2.5 | | | 2.5 | | 2.5 | | V |
| | $V_{CC} = 5$ V, $I_{OH} = -3$ mA | | 3 | | | 3 | | 3 | | |
| | $V_{CC} = 4.5$ V | $I_{OH} = -24$ mA | 2 | | | 2 | | | | |
| | | $I_{OH} = -32$ mA | 2* | | | | | 2 | | |
| $V_{OL}$ | $V_{CC} = 4.5$ V | $I_{OL} = 48$ mA | | | 0.55 | | 0.55 | | | V |
| | | $I_{OL} = 64$ mA | | | 0.55* | | | | 0.55 | |
| $I_I$ | $V_{CC} = 5.5$ V, $V_I = V_{CC}$ or GND | Control inputs | | | ±1 | | ±1 | | ±1 | μA |
| | | A or B ports | | | ±100 | | ±100 | | ±100 | |
| $I_{OZH}$‡ | $V_{CC} = 5.5$ V, $V_O = 2.7$ V | | | | 10§ | | 50 | | 10§ | μA |
| $I_{OZL}$‡ | $V_{CC} = 5.5$ V, $V_O = 0.5$ V | | | | −10§ | | −50 | | −10§ | μA |
| $I_{off}$ | $V_{CC} = 0$, $V_I$ or $V_O ≤ 4.5$ V | | | | ±100 | | | | ±100 | μA |
| $I_{CEX}$ | $V_{CC} = 5.5$ V, $V_O = 5.5$ V | Outputs high | | | 50 | | 50 | | 50 | μA |
| $I_O$¶ | $V_{CC} = 5.5$ V, $V_O = 2.5$ V | | −50 | −100 | −180 | −50 | −180 | −50 | −180 | mA |
| $I_{CC}$ | $V_{CC} = 5.5$ V, $I_O = 0$, $V_I = V_{CC}$ or GND | Outputs high | | | 250 | | 250 | | 250 | μA |
| | | Outputs low | | | 30 | | 30 | | 30 | mA |
| | | Outputs disabled | | | 250 | | 250 | | 250 | μA |
| $\Delta I_{CC}$# | $V_{CC} = 5.5$ V, One input at 3.4 V, Other inputs at $V_{CC}$ or GND | | | | 1.5 | | 1.5 | | 1.5 | mA |
| $C_i$ | $V_I = 2.5$ V or 0.5 V | Control inputs | | 7 | | | | | | pF |
| $C_{io}$ | $V_O = 2.5$ V or 0.5 V | A or B ports | | 12 | | | | | | pF |

\* On products compliant to MIL-STD-883, Class B, this parameter does not apply.
† All typical values are at $V_{CC} = 5$ V.
‡ The parameters $I_{OZH}$ and $I_{OZL}$ include the input leakage current.
§ This data sheet limit may vary among suppliers.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.

## timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)

| | | | $V_{CC} = 5$ V, $T_A = 25°C$ | | SN54ABT646 | | SN74ABT646 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | | 0 | 125 | 0 | 125 | 0 | 125 | MHz |
| $t_w$ | Pulse duration, CLK high or low | | 4 | | 4 | | 4 | | ns |
| $t_{su}$ | Setup time, A or B before CLKAB↑ or CLKBA↑ | High | 3.5 | | 3.5 | | 3.5 | | ns |
| | | Low | 3 | | 3 | | 3 | | |
| $t_h$ | Hold time, A or B after CLKAB↑ or CLKBA↑ | | 0 | | 0 | | 0 | | ns |

**TEXAS INSTRUMENTS**

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Figure 2)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | SN54ABT646 | | SN74ABT646 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | 125 | | | | | 125 | | MHz |
| $t_{PLH}$ | CLKBA or CLKAB | A or B | 2.2 | 4 | 6.8 | | | 2.2 | 7.8 | ns |
| $t_{PHL}$ | | | 1.7 | 4 | 7.4 | | | 1.7 | 8.4 | |
| $t_{PLH}$ | A or B | B or A | 1.5 | 3 | 5.9 | | | 1.5 | 6.9 | ns |
| $t_{PHL}$ | | | 1.5 | 3.3 | 5.9 | | | 1.5 | 6.9 | |
| $t_{PLH}$ | SAB or SBA† | B or A | 1.5 | 4 | 6.1 | | | 1.5 | 7.1 | ns |
| $t_{PHL}$ | | | 1.5 | 3.6 | 6.9 | | | 1.5 | 7.9 | |
| $t_{PZH}$ | $\overline{OE}$ | A or B | 1 | 4.3 | 5.3 | | | 1 | 6.3 | ns |
| $t_{PZL}$ | | | 2.1 | 5.8 | 7.4 | | | 2.1 | 8.8 | |
| $t_{PHZ}$ | $\overline{OE}$ | A or B | 1.5 | 3.5 | 7.3 | | | 1.5 | 8.3 | ns |
| $t_{PLZ}$ | | | 1.5 | 3 | 7 | | | 1.5 | 7.5 | |
| $t_{PZH}$ | DIR | A or B | 1.2 | 4.5 | 5.7 | | | 1.2 | 6.7 | ns |
| $t_{PZL}$ | | | 2.5 | 6.5 | 9 | | | 2.5 | 9.5 | |
| $t_{PHZ}$ | DIR | A or B | 1.5 | 3.8 | 6.7 | | | 1.5 | 7.7 | ns |
| $t_{PLZ}$ | | | 1.5 | 3.8 | 7.2 | | | 1.5 | 8.2 | |

† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

TEXAS
INSTRUMENTS

## PARAMETER MEASUREMENT INFORMATION
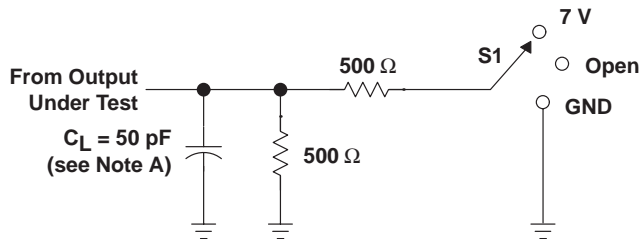
**LOAD CIRCUIT FOR OUTPUTS**

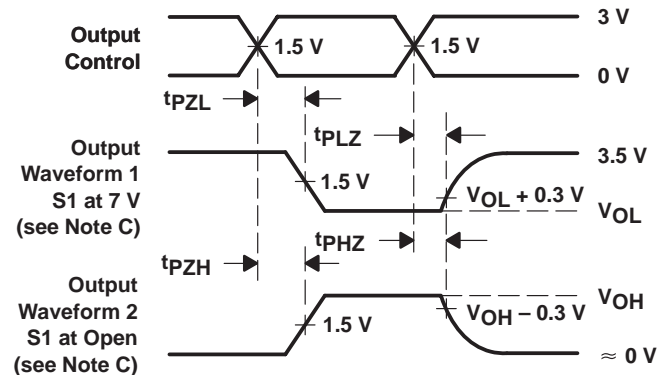| TEST | S1 |
|------|------|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V |
| $t_{PHZ}/t_{PZH}$ | Open |
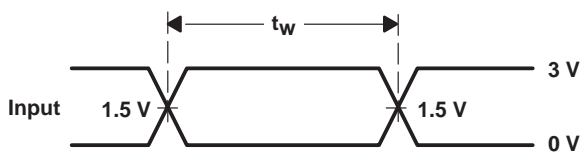
**VOLTAGE WAVEFORMS**
**PULSE DURATION**
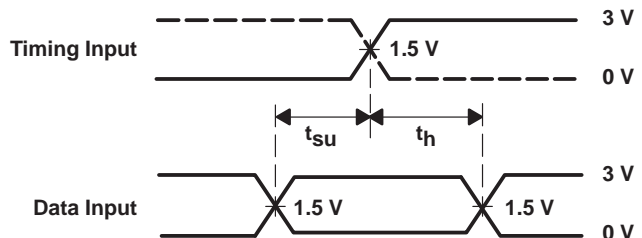
**VOLTAGE WAVEFORMS**
**SETUP AND HOLD TIMES**
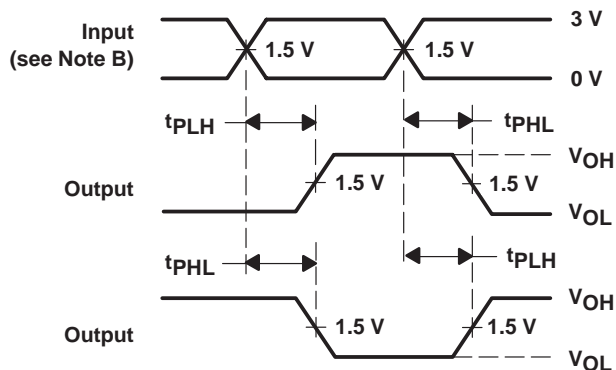
**VOLTAGE WAVEFORMS**
**PROPAGATION DELAY TIMES**
**INVERTING AND NONINVERTING OUTPUTS**

**VOLTAGE WAVEFORMS**
**ENABLE AND DISABLE TIMES**
**LOW- AND HIGH-LEVEL ENABLING**

NOTES:  A.  $C_L$ includes probe and jig capacitance.
   B.  All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
   C.  Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
       Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
   D.  The outputs are measured one at a time with one transition per measurement.

**Figure 2. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| SN74ABT646DBLE | OBSOLETE | SSOP | DB | 24 | | TBD | Call TI | Call TI |
| SN74ABT646DBR | ACTIVE | SSOP | DB | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT646DBRE4 | ACTIVE | SSOP | DB | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT646DGVR | ACTIVE | TVSOP | DGV | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT646DGVRE4 | ACTIVE | TVSOP | DGV | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT646DW | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT646DWE4 | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT646DWR | ACTIVE | SOIC | DW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT646DWRE4 | ACTIVE | SOIC | DW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT646NT | ACTIVE | PDIP | NT | 24 | 15 | Pb-Free (RoHS) | CU NIPDAU | Level-NC-NC-NC |
| SN74ABT646NTE4 | ACTIVE | PDIP | NT | 24 | 15 | Pb-Free (RoHS) | CU NIPDAU | Level-NC-NC-NC |
| SN74ABT646PW | ACTIVE | TSSOP | PW | 24 | 60 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT646PWE4 | ACTIVE | TSSOP | PW | 24 | 60 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT646PWLE | OBSOLETE | TSSOP | PW | 24 | | TBD | Call TI | Call TI |
| SN74ABT646PWR | ACTIVE | TSSOP | PW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT646PWRE4 | ACTIVE | TSSOP | PW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

**(3)** MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**NT (R-PDIP-T\*\*)**

**PLASTIC DUAL-IN-LINE PACKAGE**

**24 PINS SHOWN**
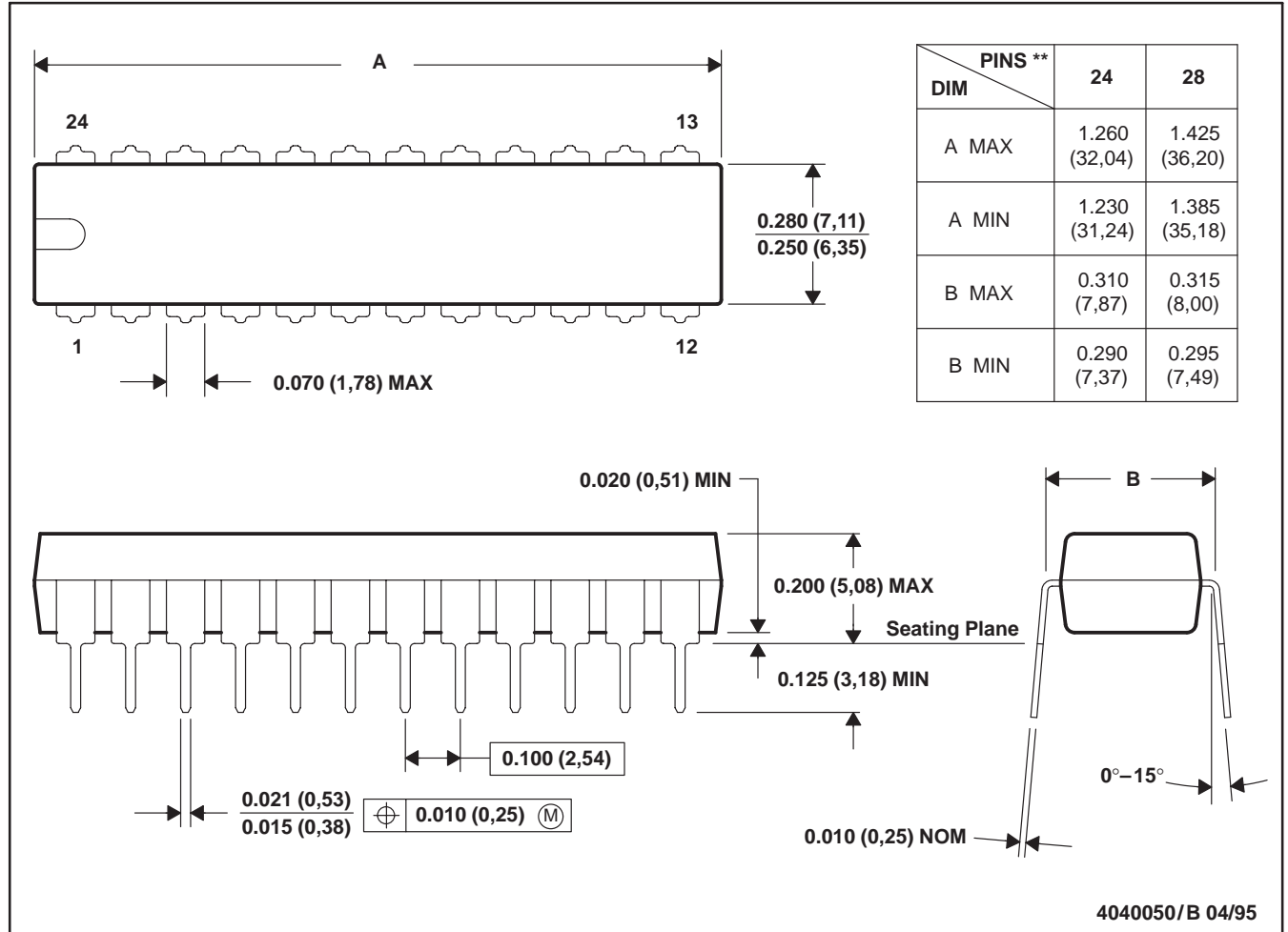


| PINS \*\* DIM | 24 | 28 |
|---|---|---|
| A  MAX | 1.260 (32,04) | 1.425 (36,20) |
| A  MIN | 1.230 (31,24) | 1.385 (35,18) |
| B  MAX | 0.310 (7,87) | 0.315 (8,00) |
| B  MIN | 0.290 (7,37) | 0.295 (7,49) |

0.280 (7,11)
0.250 (6,35)

0.070 (1,78) MAX

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

0.010 (0,25) Ⓜ

B

0°−15°

0.010 (0,25) NOM

**4040050 / B 04/95**

NOTES: A.  All linear dimensions are in inches (millimeters).
B.  This drawing is subject to change without notice.

**TEXAS INSTRUMENTS**

**DGV (R-PDSO-G\*\*)**                                                                          **PLASTIC SMALL-OUTLINE**

**24 PINS SHOWN**
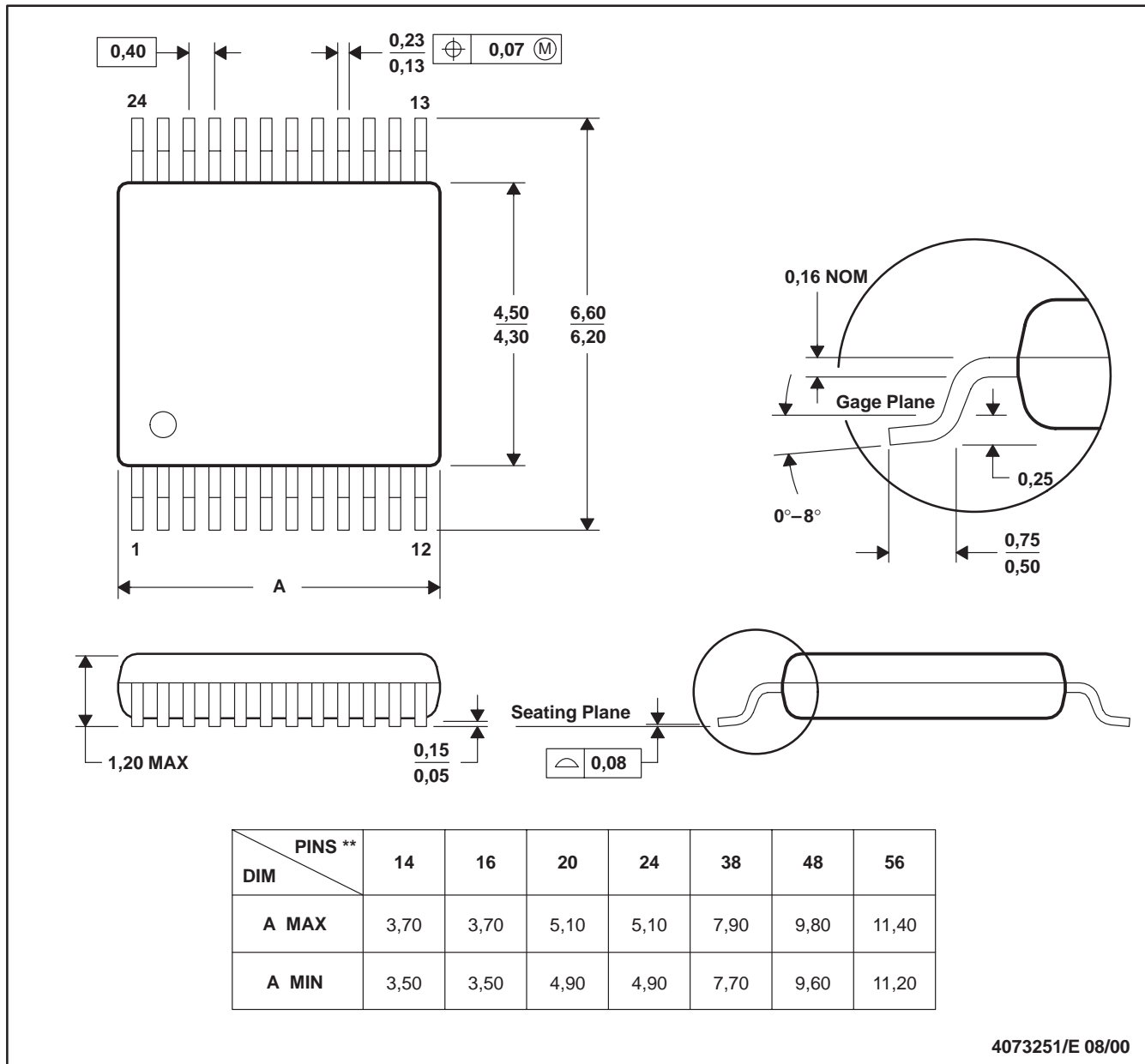
0,40

$\frac{0,23}{0,13}$  ⊕ 0,07 Ⓜ

24                    13

$\frac{4,50}{4,30}$    $\frac{6,60}{6,20}$

1                    12

A

0,16 NOM

Gage Plane

0°–8°

0,25

$\frac{0,75}{0,50}$

1,20 MAX

$\frac{0,15}{0,05}$

Seating Plane

△ 0,08

| DIM \ PINS ** | 14 | 16 | 20 | 24 | 38 | 48 | 56 |
|---|---|---|---|---|---|---|---|
| **A  MAX** | 3,70 | 3,70 | 5,10 | 5,10 | 7,90 | 9,80 | 11,40 |
| **A  MIN** | 3,50 | 3,50 | 4,90 | 4,90 | 7,70 | 9,60 | 11,20 |

4073251/E 08/00

NOTES:  A.  All linear dimensions are in millimeters.
B.  This drawing is subject to change without notice.
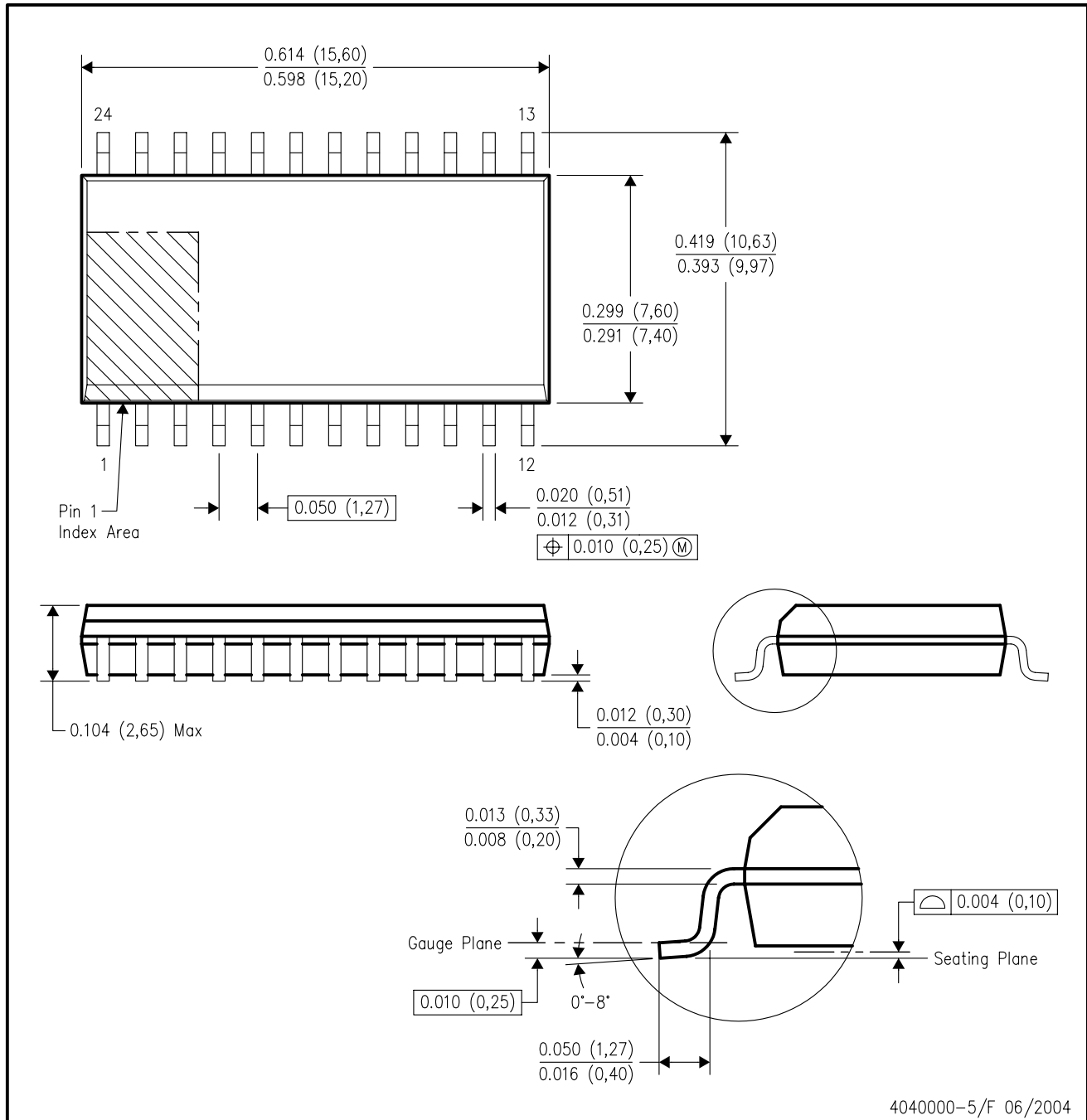C.  Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D.  Falls within JEDEC:  24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

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## DW (R−PDSO−G24)  PLASTIC SMALL−OUTLINE PACKAGE

$\dfrac{0.614\ (15,60)}{0.598\ (15,20)}$

24

13

$\dfrac{0.419\ (10,63)}{0.393\ (9,97)}$

$\dfrac{0.299\ (7,60)}{0.291\ (7,40)}$

1

12

Pin 1
Index Area

0.050 (1,27)

$\dfrac{0.020\ (0,51)}{0.012\ (0,31)}$

⊕ 0.010 (0,25) Ⓜ

0.104 (2,65) Max

$\dfrac{0.012\ (0,30)}{0.004\ (0,10)}$

$\dfrac{0.013\ (0,33)}{0.008\ (0,20)}$

○ 0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)

0°−8°

$\dfrac{0.050\ (1,27)}{0.016\ (0,40)}$

4040000−5/F 06/2004

NOTES:  A.  All linear dimensions are in inches (millimeters).
B.  This drawing is subject to change without notice.
C.  Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
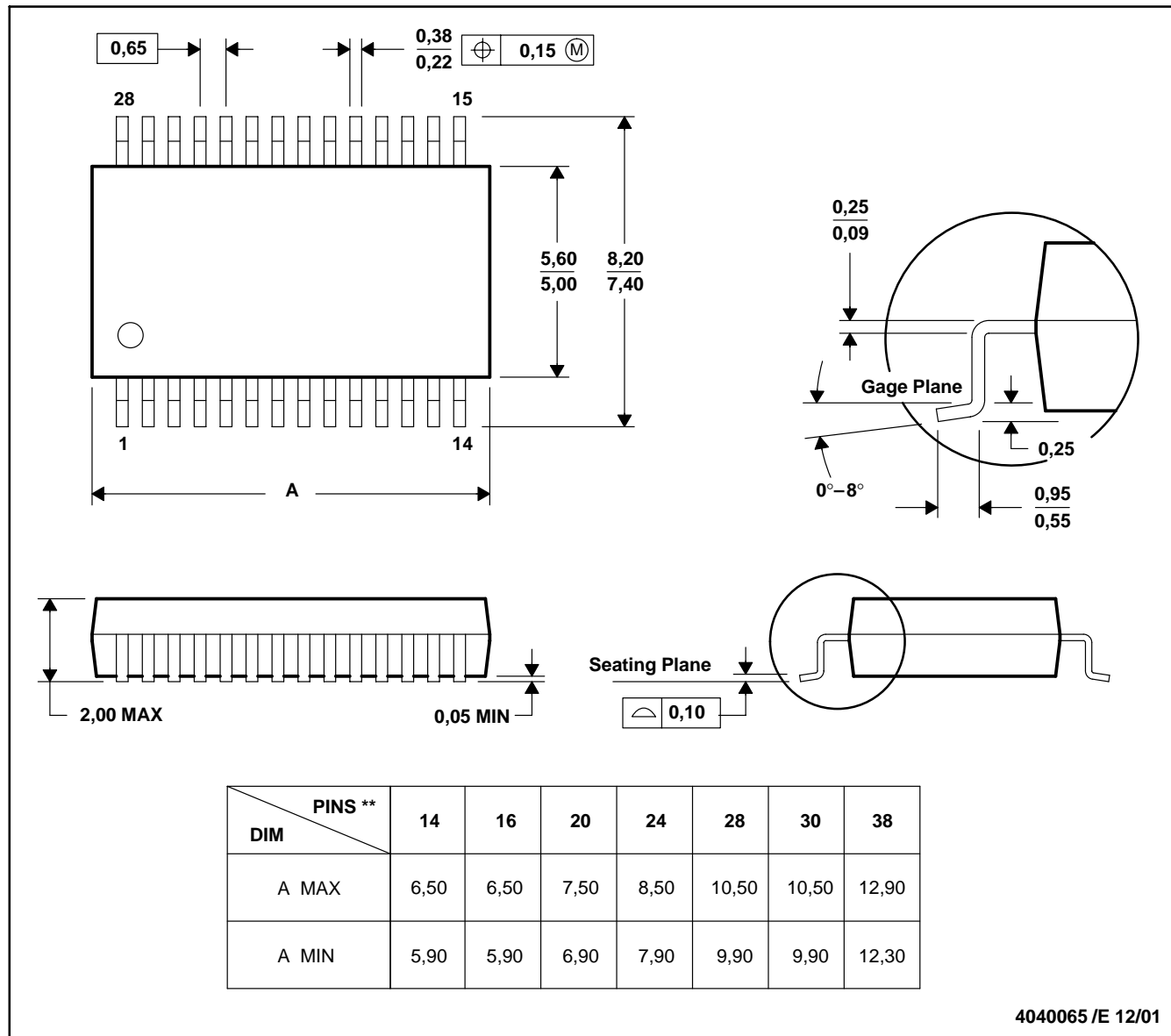D.  Falls within JEDEC MS−013 variation AD.

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**DB (R-PDSO-G\*\*)**                                 **PLASTIC SMALL-OUTLINE**

**28 PINS SHOWN**



| PINS **<br>DIM | 14 | 16 | 20 | 24 | 28 | 30 | 38 |
|---|---|---|---|---|---|---|---|
| A MAX | 6,50 | 6,50 | 7,50 | 8,50 | 10,50 | 10,50 | 12,90 |
| A MIN | 5,90 | 5,90 | 6,90 | 7,90 | 9,90 | 9,90 | 12,30 |

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
        D. Falls within JEDEC MO-150

**TEXAS INSTRUMENTS**

# MECHANICAL DATA

**PW (R-PDSO-G\*\*)**                                          **PLASTIC SMALL-OUTLINE PACKAGE**

**14 PINS SHOWN**



| PINS ** DIM | 8 | 14 | 16 | 20 | 24 | 28 |
|---|---|---|---|---|---|---|
| A MAX | 3,10 | 5,10 | 5,10 | 6,60 | 7,90 | 9,80 |
| A MIN | 2,90 | 4,90 | 4,90 | 6,40 | 7,70 | 9,60 |

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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