

NEC

MOS INTEGRATED CIRCUIT

 μ PD75108F,75112F,75116F

4-BIT SINGLE-CHIP MICROCOMPUTER

DESCRIPTION

The μ PD75116F offers high-speed operation ($t_{CY} = 1.91 \mu s$) at a low supply voltage ($V_{DD} = 2.7 V$) which is not possible with the μ PD75116.

It has the same functions as, and is pin compatible with, the μ PD75116, allowing low voltage sets to be developed by making efficient use of previously developed and used software resources. Note, however, that the operating voltage range is different from that of the μ PD75116.

A version of the μ PD75116F with on-chip PROM, the μ PD75P116*, is also available for evaluation during system development.

* There are some differences in electrical specifications between the μ PD75116F and the μ PD75P116.

Functions are described in detail in the following User's Manual, which should be read when carrying out design work.

μ PD75116 User's Manual : IEM-922

FEATURES

- μ PD75116 low voltage high-speed operation product
- Instruction execution time

	$T_a = -40 \text{ to } +50 \text{ }^\circ\text{C}$	$T_a = -40 \text{ to } +60 \text{ }^\circ\text{C}$
$V_{DD} = 2.7 \text{ to } 5.0 V$	1.91 μs , 15.3 μs (operation at 4.19 MHz) 2 μs , 4 μs , 32 μs (operation at 2 MHz)	—
$V_{DD} = 2.8 \text{ to } 5.0 V$	—	1.91 μs , 15.3 μs (operation at 4.19 MHz) 2 μs , 4 μs , 32 μs (operation at 2 MHz)
$V_{DD} = 4.5 \text{ to } 5.0 V$	0.95 μs , 1.91 μs , 15.3 μs (operation at 4.19 MHz)	

- 43 systematically arranged instructions
 - 8-bit data transfer, compare, operation and increment/decrement instructions
 - GETI instruction allowing any 2-byte or 3-byte instruction to be implemented in 1 byte
- Wide range of input/output ports : 58 ports
- 3 on-chip 8-bit timer channels : synchronous/asynchronous (start/stop)
- 8-bit serial interface on chip
- Programmable threshold port : 4-bit resolution $\times$ 4 channels

"Unless there are any particular functional differences, the μ PD75116F is described in this document as a representative product."

The information in this document is subject to change without notice.

The mark ★ shows major revised points.

ORDERING INFORMATION

Ordering Code	Package	Quality Grade
μ PD75108FGF-xxx-3BE	64-pin plastic QFP (14 × 12 mm)	Standard
μ PD75112FGF-xxx-3BE	64-pin plastic QFP (14 × 12 mm)	Standard
μ PD75116FGF-xxx-3BE	64-pin plastic QFP (14 × 20 mm)	Standard

Remarks xxx: ROM code number

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

APPLICATIONS

Cordless telephone subsets, portable radio equipment, pager, etc.

OVERVIEW OF FUNCTIONS

Item		Contents
Basic instructions		43
Instruction cycle		0.95 μs, 1.91 μs, 15.3 μs (V _{DD} = 4.5 to 5.0 V, 4.19 MHz operation) 2 μs, 4 μs, 32 μs (V _{DD} = 2.7 to 5.0 V, 2 MHz operation) 3-stage switching capability
Minimum instruction execution time		0.95 μs (operating at 4.5 to 5.0 V) 1.91 μs (operating at 2.7 V)
On-chip memory	ROM	8064 × 8 bits (μPD75108F)
		12160 × 8 bits (μPD75112F)
		16256 × 8 bits (μPD75116F)
	RAM	512 × 4 bits
General register		4-bits × 8 × 4 banks (memory mapping)
Accumulator		3 accumulators for different manipulated data lengths • 1-bit accumulator (CY), 4-bit accumulator (A), 8-bit accumulator (XA)
Input/output port		Total 58 • CMOS input pins : 10 • CMOS input/output pins (LED direct drive capability) : 32 • Middle-high voltage N-ch open-drain input/output pins : 12 (LED direct drive capability, a pull-up resistor can be incorporated bit-wise.) • Comparator input pins (4-bit precision) : 4
Timer/counter		• 8-bit timer/event counter × 2 • 8-bit basic interval timer (watchdog timer applicable)
8-bit serial interface		• 2 transfer modes • Serial transmission/reception modes • Serial reception mode • LSB top/MSB top switchable
Vector interrupt		External : 3 Internal : 4
Test input		External : 2
Standby		• STOP/HALT mode
Instruction set		• Various bit manipulation instructions (set, reset, test, Boolean operation) • 8-bit data transfer, comparison, operation, increment/decrement instructions • 1-byte relative branch instruction • GETI instruction that can implement arbitrary 2-byte/3-byte instructions with 1 byte
Others		• Bit manipulation memory (bit sequential buffer) on chip
Package		• 64-pin plastic QFP (14 × 20 mm)

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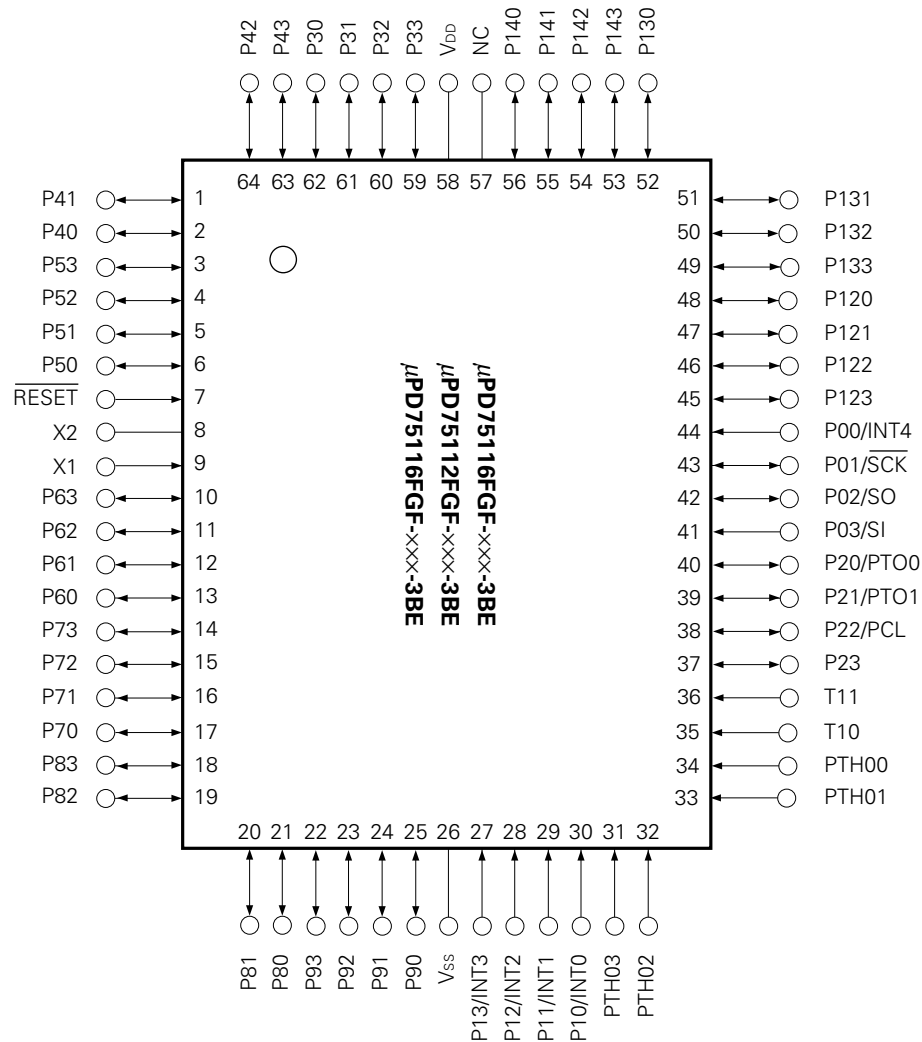
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1. PIN CONFIGURATION (TOP VIEW)

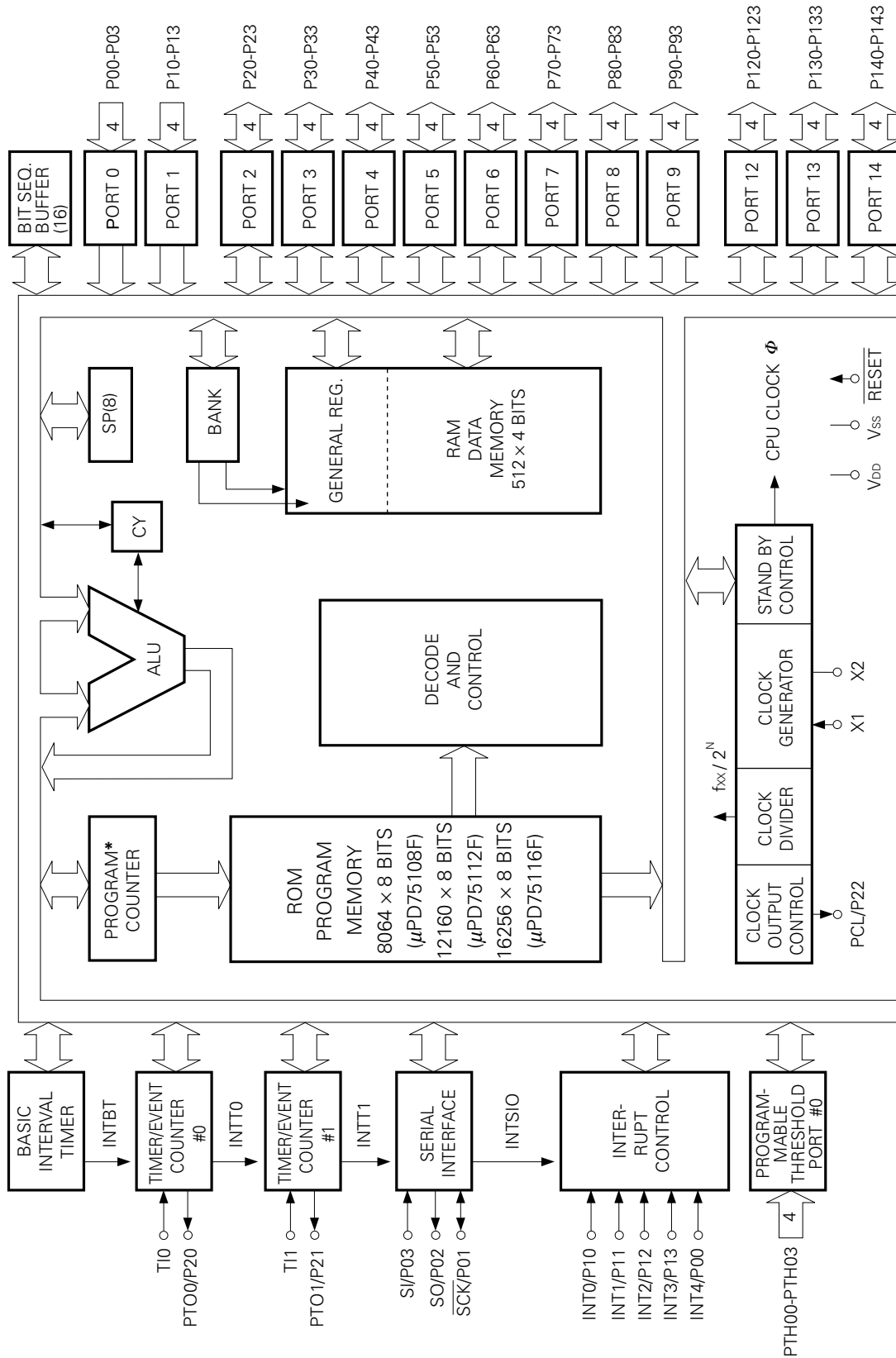
64-Pin Plastic QFP (14 × 20 mm)



★ Pin Name

P00-P03	: Port 0	$\overline{\text{SCK}}$	: Serial Clock
P10-P13	: Port 1	SO	: Serial Output
P20-P23	: Port 2	SI	: Serial Input
P30-P33	: Port 3	PTO0, PTO1	: Programmable Timer Output
P40-P43	: Port 4	PCL	: Programmable Clock
P50-P53	: Port 5	PTH00-PTH03	: Programmable Treshold Input
P60-P63	: Port 6	INT0, INT1, INT4	: External Vectored Interrupt Input
P70-P73	: Port 7	INT2, INT3	: External Test Input
P80-P83	: Port 8	TI0, TI1	: Timer Input
P90-P93	: Port 9	X1, X2	: Clock Oscillation
P120-P123	: Port 12	$\overline{\text{RESET}}$	: Reset
P130-P133	: Port 13	NC	: No Connection
P140-P143	: Port 14	VDD	: Positive Power Supply
		VSS	: Ground

2. BLOCK DIAGRAM



* The μ PD75108F program counter is composed of 13 bits and the μ PD75112F/75116F program counter is composed of 14 bits

3. PIN FUNCTIONS

3.1 PORT PINS

Pin Name	Input/Output	Dual-Function Pin	Function	8-bit I/O	After Reset	I/O Circuit Type *1
P00	Input	INT4	4-bit input port (PORT 0).	×	Input	Ⓑ
P01	Input/output	SCK				Ⓕ
P02	Input/output	SO				E
P03	Input	SI				Ⓑ
P10	Input	INT0	4-bit input port (PORT 1).	×	Input	Ⓑ
P11		INT1				
P12		INT2				
P13		INT3				
P20 *3	Input/output	PTO0	4-bit input/output port (PORT 2).	×	Input	E
P21 *3		PTO1				
P22 *3		PCL				
P23 *3		—				
P30 to P33 *3	Input/output	—	Programmable 4-bit input/output port (PORT 3). Input/output can be specified bit-wise.	×	Input	E
P40 to P43 *3	Input/output	—	4-bit input/output port (PORT 4).	○	Input	E
P50 to P53 *3	Input/output	—	4-bit input/output port (PORT 5).		Input	E
P60 to P63 *3	Input/output	—	Programmable 4-bit input/output port (PORT 6). Input/output can be specified bit-wise.	○	Input	E
P70 to P73 *3	Input/output	—	4-bit input/output port (PORT 7).		Input	E
P80 to P83 *3	Input/output	—	4-bit input/output port (PORT 8).	○	Input	E
P90 to P93 *3	Input/output	—	4-bit input/output port (PORT 9).		Input	E
P120 to P123 *3	Input/output	—	N-ch open-drain 4-bit input/output port (PORT 12). On-chip pull-up resistor can be specified bit-wise (mask option). Open-drain: +10 V withstand voltage	○	Input *2	M
P130 to P133 *3	Input/output	—	N-ch open-drain 4-bit input/output port (PORT 13). On-chip pull-up resistor can be specified bit-wise (mask option). Open-drain: +10 V withstand voltage		Input *2	M
P140 to P143 *3	Input/output	—	N-ch open-drain 4-bit input/output port (PORT 14). On-chip pull-up resistor can be specified bit-wise (mask option). Open-drain: +10 V withstand voltage	—	Input *2	M

- * 1. ○ : Schmitt trigger input
 2. Open-drain ... high impedance
 On-chip pull-up resistor ... high level
 3. Direct LED drive capability

3.2 OTHER PINS

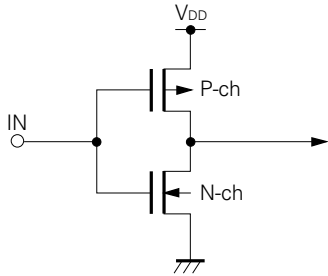
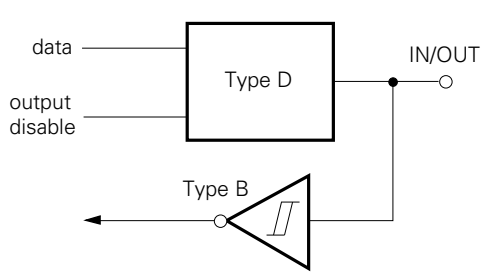
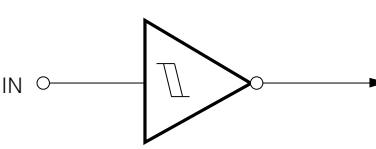
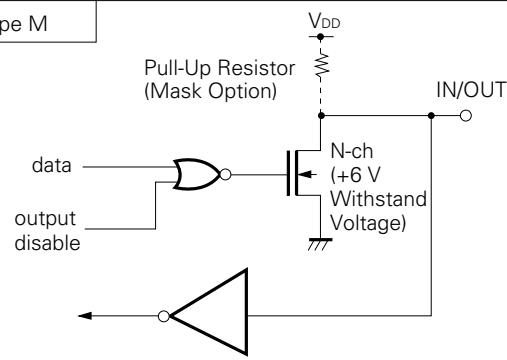
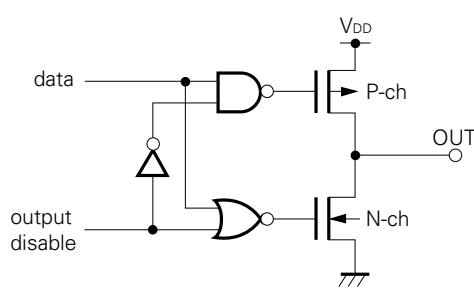
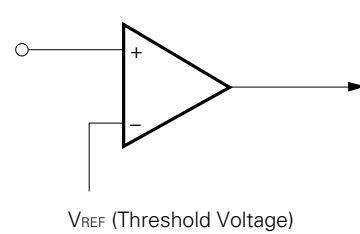
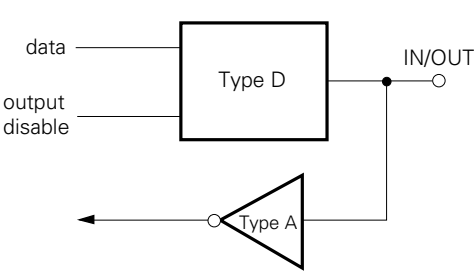
Pin Name	Input/Output	Dual-Function Pin	Function	After Reset	I/O Circuit Type *1
PTH00 to PTH03	Input	—	Variable threshold voltage 4-bit analog input port.		N
TI0	Input	—	External event pulse input to timer/event counter. Or edge detection vectored interrupt input or 1-bit input is also possible.		Ⓑ
TI1					
PTO0	Input/output	P20	Timer/event counter output	Input	E
PTO1		P21			
$\overline{\text{SCK}}$	Input/output	P01	Serial clock input/output	Input	Ⓕ
SO	Input/output	P02	Serial data output	Input	E
SI	Input	P03	Serial data input	Input	Ⓑ
INT4	Input	P00	Edge detection vector interrupt input (detection of both rising and falling edges)	Input	Ⓑ
INT0	Input	P10	Edge detection vector interrupt input (detection edge selectable)	Input	Ⓑ
INT1		P11			
INT2	Input	P12	Edge detection testable input (rising edge detection)	Input	Ⓑ
INT3		P13			
PCL	Input/output	P22	Clock output	Input	E
X1, X2		—	System clock oscillation crystal/ceramic connection pin. When an external clock is used, the clock is input to X1 and the inverted clock is input to X2.		
$\overline{\text{RESET}}$	Input	—	System reset input (low-level active).		Ⓑ
NC*2	—	—	No Connection		
V _{DD}		—	Positive power supply		
V _{SS}		—	GND potential		

- * 1. ○ : Schmitt trigger input
 2. When sharing a print board with μPD75P116, NC pin should be connected to V_{DD}.

3.3 PIN INPUT/OUTPUT CIRCUITS

The input/output circuits of each pin of the μPD75116F are shown in abbreviated form.

Fig. 3-1 Pin Input/Output Circuit List

Type A  CMOS standard input buffer	Type F  This is an input/output circuit made up of a Type D push-pull output and Type B Schmitt-triggered input.
Type B  Schmitt-trigger input with hysteresis characteristic	Type M  Middle-High Voltage Input Buffer (+6 V Withstand Voltage)
Type D  Push-pull output that can be made high-impedance output (P-ch and N-ch OFF)	Type N  Comparator
Type E  This is an input/output circuit made up of a Type D push-pull output and Type A input buffer.	

3.4 RECOMMENDED CONNECTION OF UNUSED PINS

Pin	Recommended Connection
PTH00 to PTH03	Connect to V _{SS} or V _{DD} .
T10	
T11	
P00	Connect to V _{SS} .
P01 to P03	Connect to V _{SS} or V _{DD} .
P10 to P13	Connect to V _{SS} .
P20 to P23	Input : Connect to V_{SS} or V_{DD}. Output : Leave open.
P30 to P33	
P40 to P43	
P50 to P53	
P60 to P63	
P70 to P73	
P80 to P83	
P90 to P93	
P120 to P123	
P130 to P133	
P140 to P143	
NC	Leave open *

* If a printed board is used with the μPD75P116, NC pin should be connected to V_{DD} directly.

3.5 PRECAUTIONS CONCERNING P00/INT4 PIN AND $\overline{\text{RESET}}$ PIN

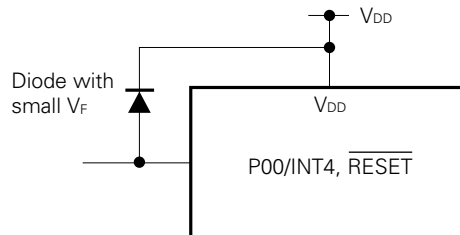
In addition to the functions shown in 3.1 and 3.2, the P00/INT4 pin and $\overline{\text{RESET}}$ pin are also used to set the test mode for testing internal μ PD75116F operation (for IC testing).

The test mode is set when a voltage greater than V_{DD} is applied to either of these pins. Consequently, if noise exceeding V_{DD} is applied during normal operation, the test mode may be entered, making it impossible for normal operation to continue.

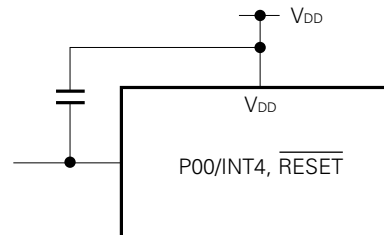
If, for example, inter-wiring noise is applied to the P00/INT4 or $\overline{\text{RESET}}$ pin due to the length of the wiring from these pins, and the pin voltage exceeds V_{DD} , misoperation may result.

Wiring should therefore be carried out so that interwiring noise is suppressed as far as possible. If it is completely impossible to suppress noise, noise prevention measures should be taken using an external component as shown below.

- Diode with small V_F (0.3 V or less) connected between P00/INT4 or $\overline{\text{RESET}}$ and V_{DD}



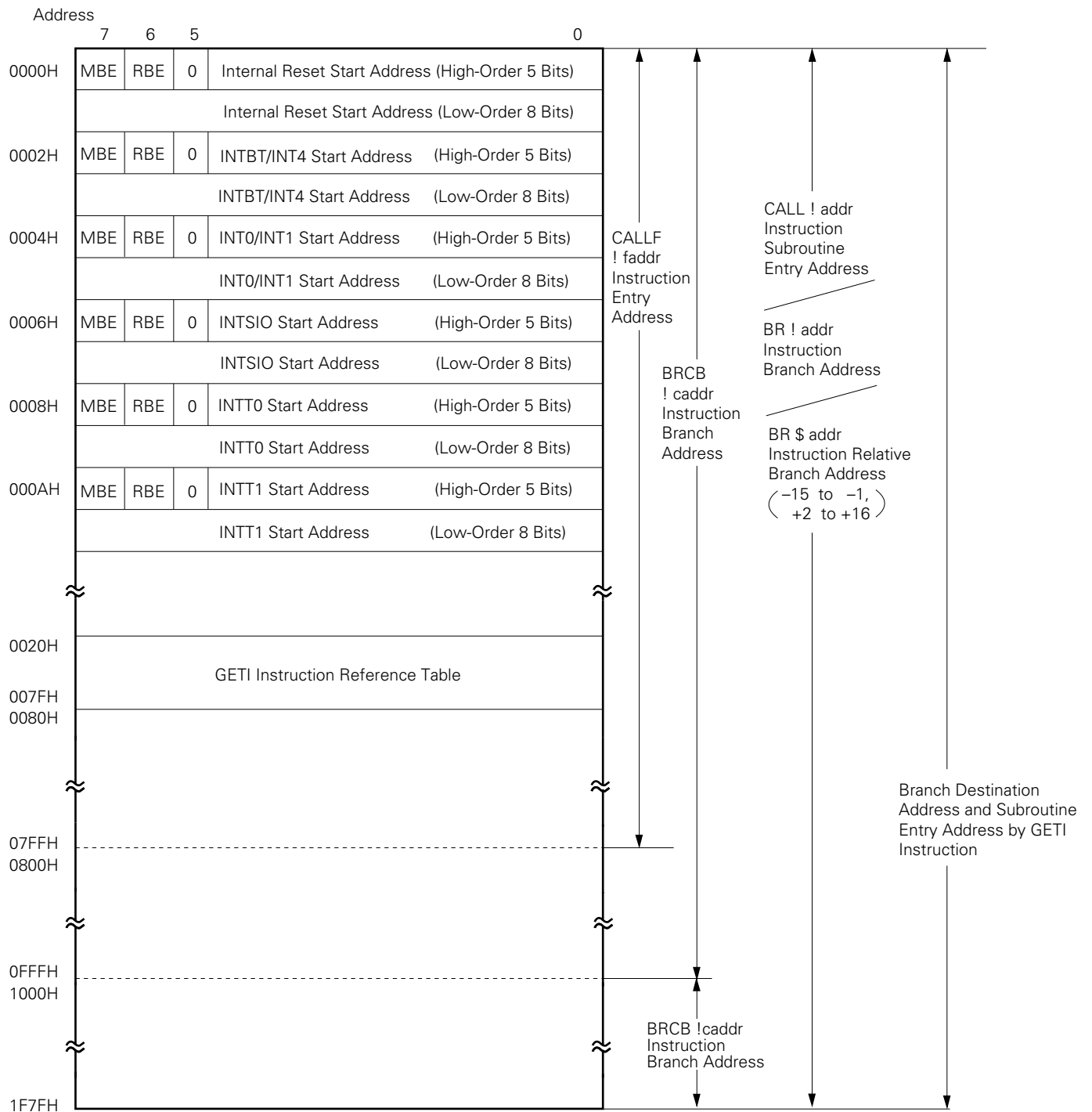
- Capacitor connected between P00/INT4 or $\overline{\text{RESET}}$ and V_{DD}



4. MEMORY CONFIGURATION

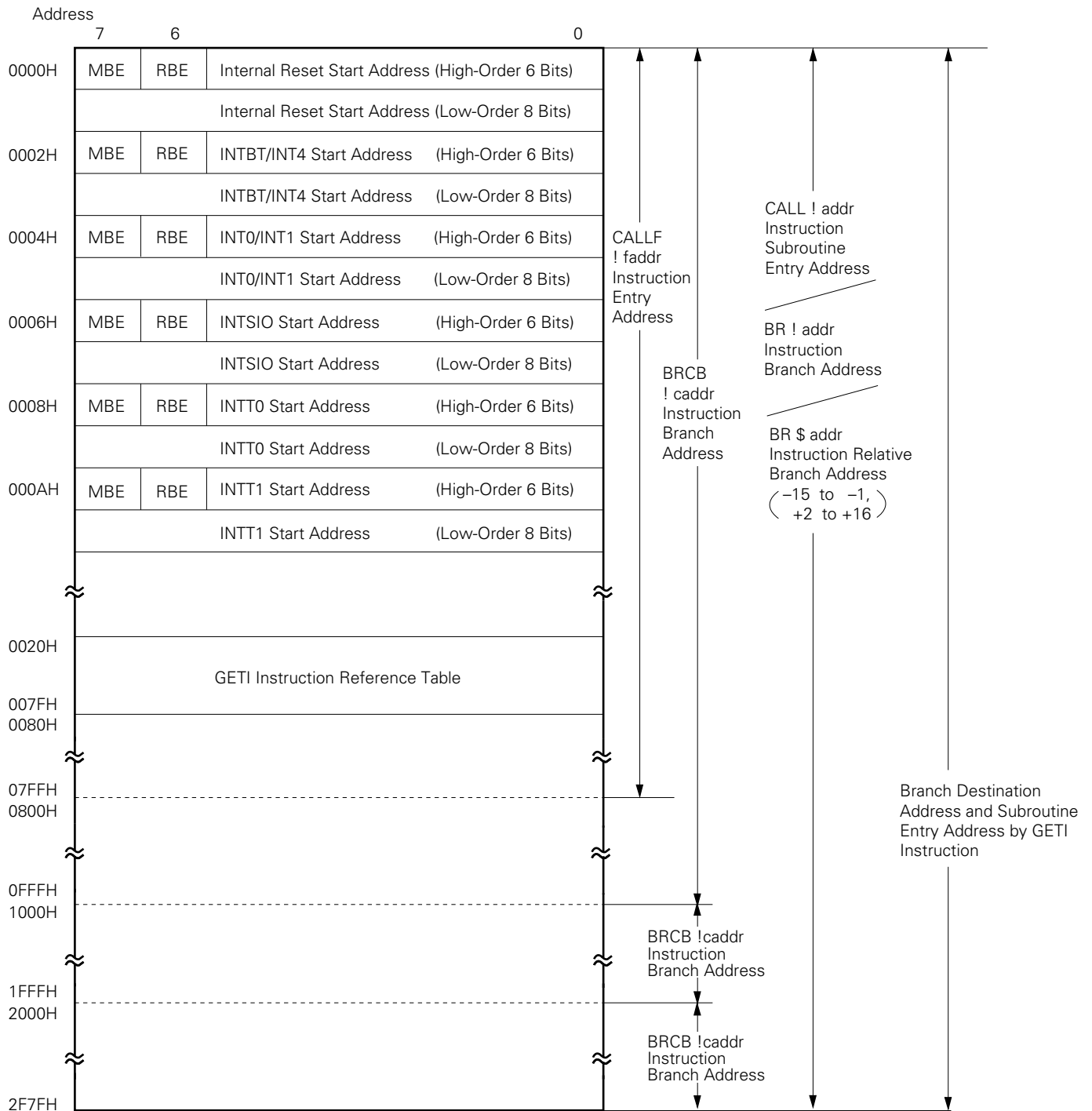
- Program memory (ROM) :
 - 8064 $\times$ 8 bits (0000H to 1F7FH) : μ PD75108F
 - 12160 $\times$ 8 bits (0000H to 2F7FH) : μ PD75112F
 - 16256 $\times$ 8 bits (0000H to 3F7FH) : μ PD75116F
- 0000H to 0001H : Vector table in which a program start address after reset is written.
- 0002H to 000BH : Vector table in which program start addresses after interruption are written.
- 0020H to 007FH : Table area referred by GETI instruction
- Data memory
 - Data area : 512 $\times$ 4 bits (000H to 1FFH)
 - Peripheral hardware area : 128 $\times$ 4 bits (F80H to FFFH)

Fig. 4-1 Program Memory Map (μPD75108F)



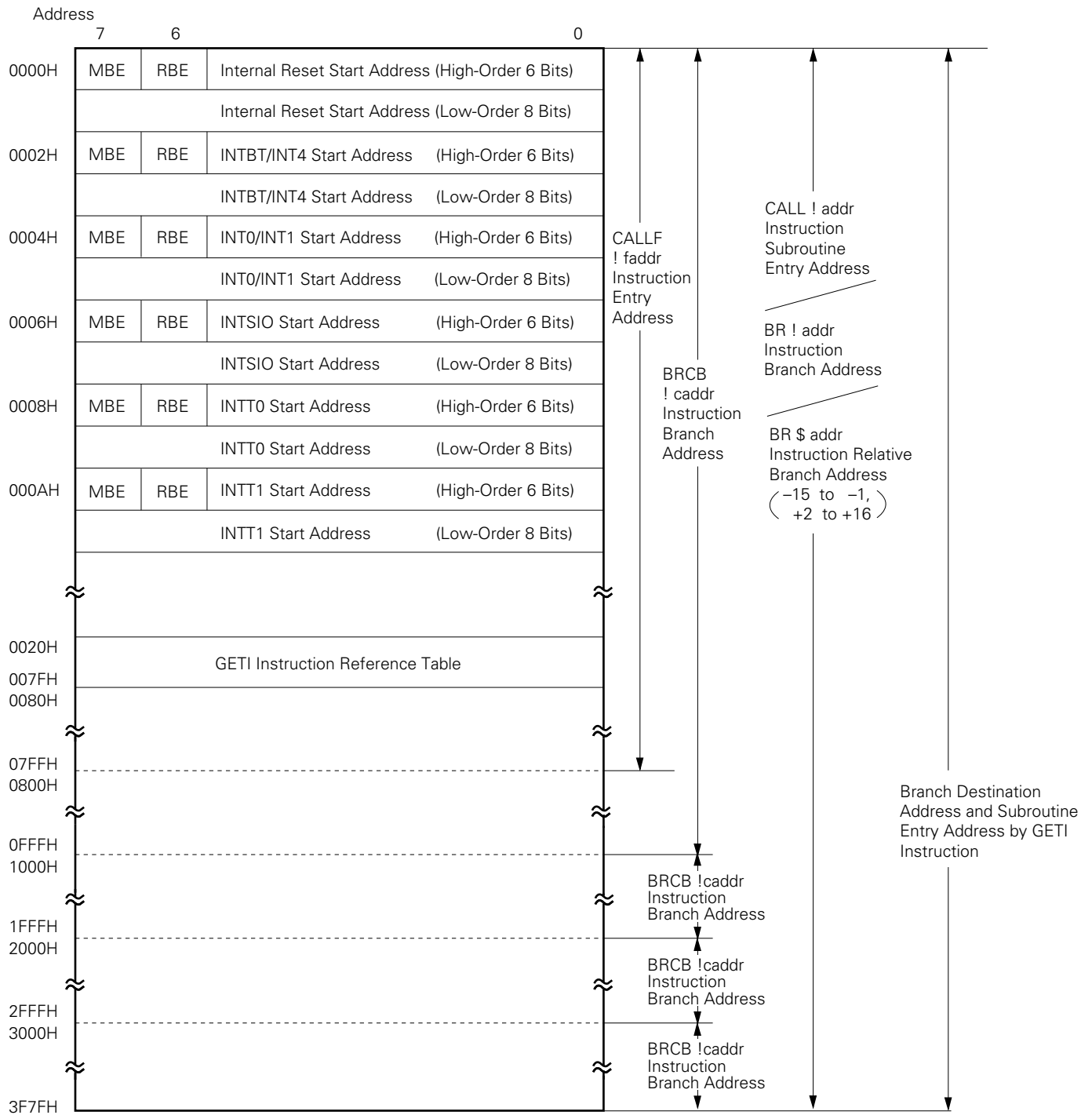
Remarks Apart from the above instructions, branching is possible to an address at which only the PC low-order 8 bits have been changed by the BR PCDE or BR PCXA instruction.

Fig. 4-2 Program Memory Map (μPD75112F)



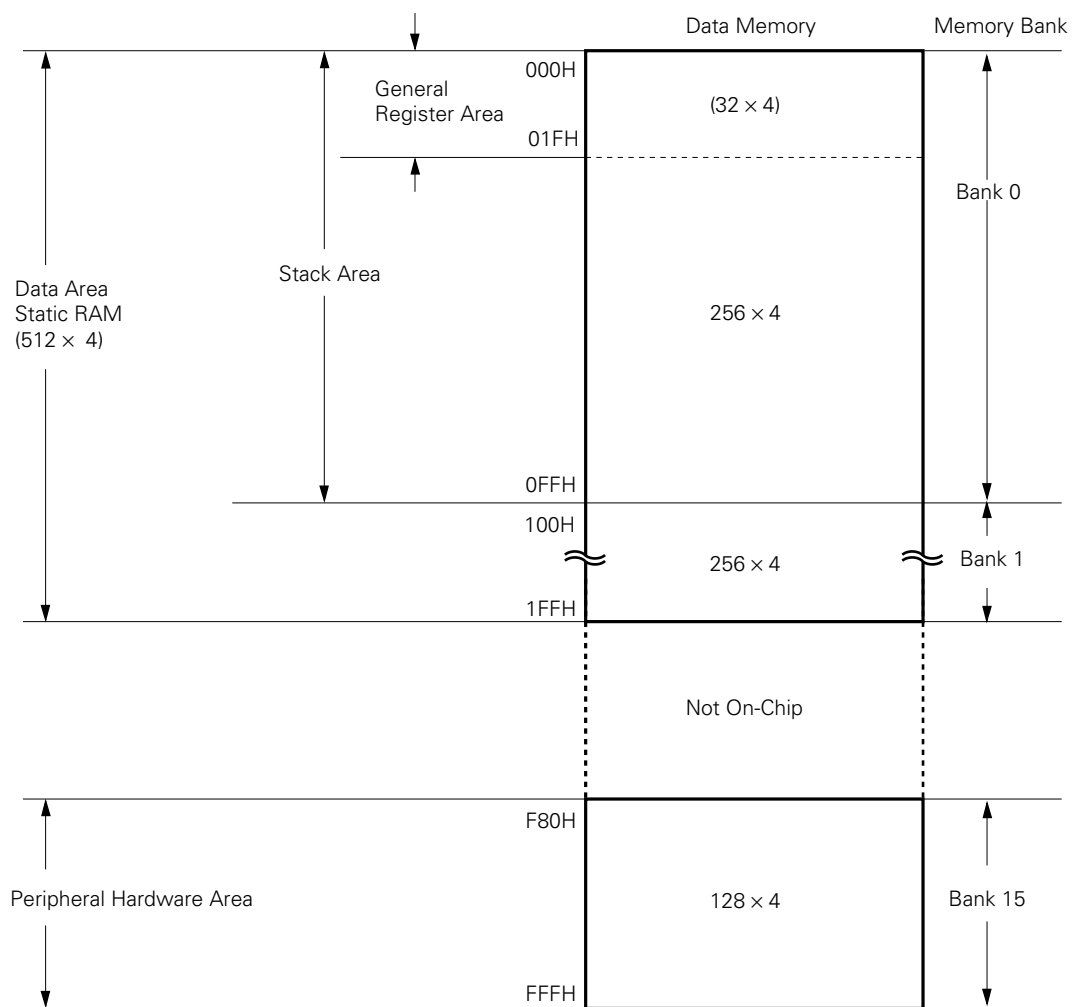
Remarks Apart from the above instructions, branching is possible to an address at which only the PC low-order 8 bits have been changed by the BR PCDE or BR PCXA instruction.

Fig. 4-3 Program Memory Map (μPD75116F)



Remarks Apart from the above instructions, branching is possible to an address at which only the PC low-order 8 bits have been changed by the BR PCDE or BR PCXA instruction.

Fig. 4-4 Data Memory Map



5. PERIPHERAL HARDWARE FUNCTIONS

5.1 DIGITAL INPUT/OUTPUT PORTS

There are the following three digital input/output ports.

- CMOS input (PORT0, PORT1) : 8
 - CMOS input/output (PORT2 to PORT9) : 32
 - N-ch open-drain input/output (PORT12 to PORT14) : 12
-
- Total : 52

Table 5-1 List of Input/Output Pin Manipulation Commands

Port Name	Function	Operation/Features	Remarks
PORT 0 PORT 1	4-bit input	Regardless of the operating mode of the shared pin, reading or test is always possible.	These pins are shared with SI, SO, SCK, INT0 to INT4.
PORT 3 PORT 6	4-bit input/output *	Can be set in the input or output bit-wise.	_____
PORT 2 PORT 4 PORT 5 PORT 7 PORT 8 PORT 9		Can be set in the input or output mode as a 4-bit unit. Ports 4 and 5, 6 and 7, and 8 and 9 are paired and data input/output is possible as an 8-bit unit.	Port 2, PT00, PT01, and PCL share the same pins.
PORT12 PORT13 PORT14		Can be set to input or output mode as a 4-bit unit. Ports 12 and 13 are paired and data input/output is possible as an 8-bit unit.	On-chip pull-up resistor specifiable bit-wise by mask option.

* Can drive a LED directly.

5.2 CLOCK GENERATOR

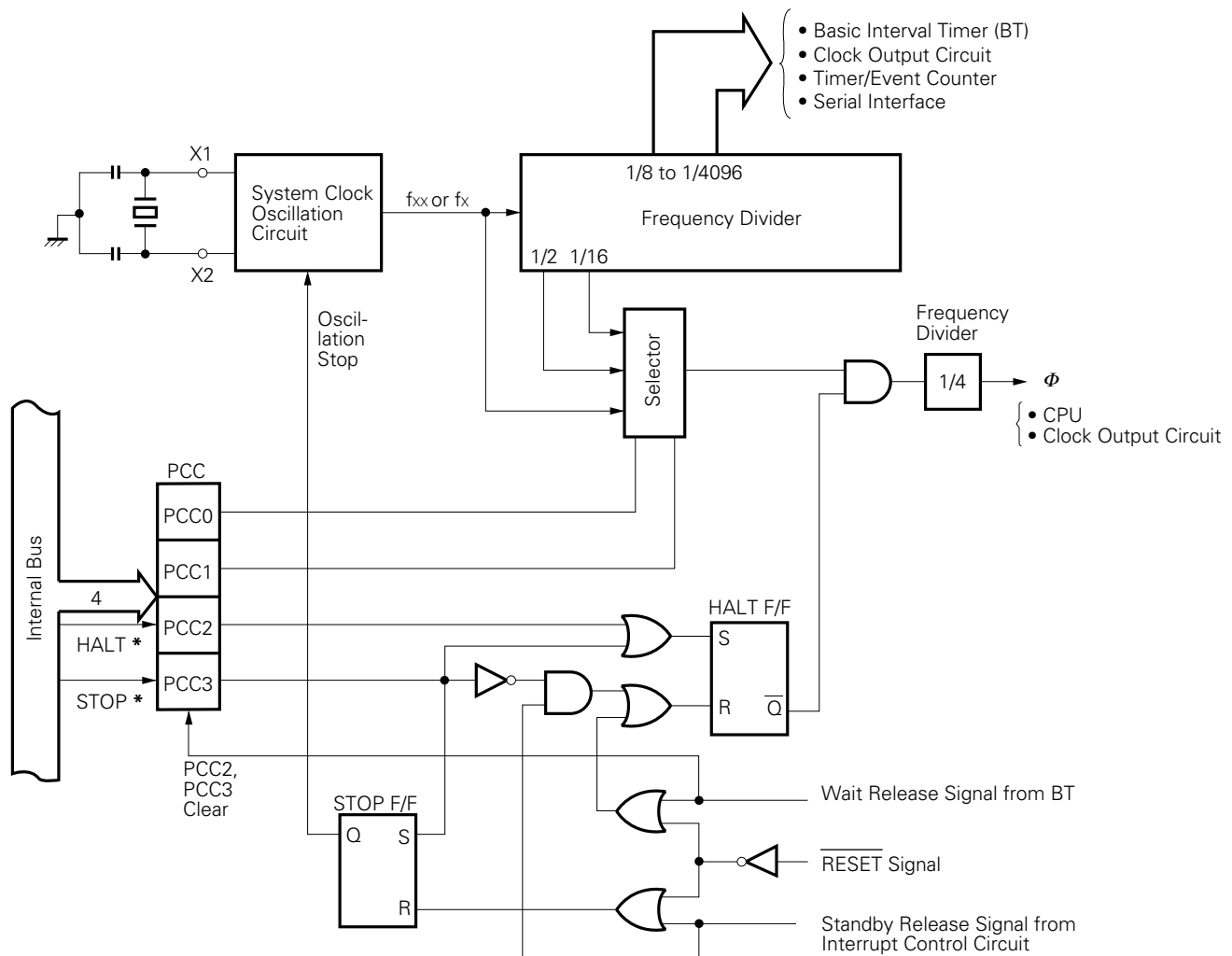
(1) Clock generator configuration

This is the circuit which generates various kinds of clock supplied to the CPU and peripheral hardware to control the CPU operating mode.

This circuit can also change the instruction execution time.

- 0.95 μ s/1.91 μ s/15.3 μ s (4.19 MHz operation)

Fig. 5-1 Clock Generator Block Diagram



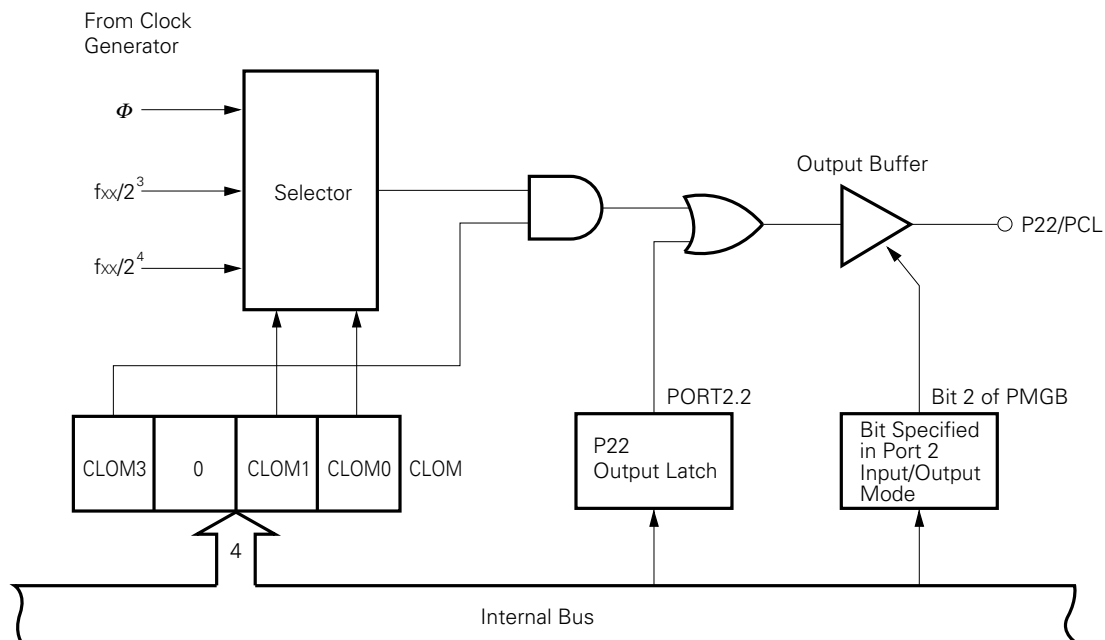
- Remarks**
1. fxx = Crystal/ceramic oscillator frequency
 2. fx = External clock frequency
 3. Φ = CPU Clock
 4. * indicates instruction execution
 5. PCC : Processor clock control register
 6. One Φ clock cycle (t_{cy}) is one machine cycle. See "AC CHARACTERISTICS" in 12. "ELECTRICAL SPECIFICATIONS" for t_{cy} .

5.3 CLOCK OUTPUT CIRCUIT

The clock output circuit is a circuit which outputs a clock pulse from P22/PCL and is used to supply clock pulses to remote control outputs or peripheral LSI's.

- Clock output (PCL) : ϕ , 524 kHz, 262 kHz (4.19 MHz operation)

Fig. 5-2 Configuration of Clock Output Circuit

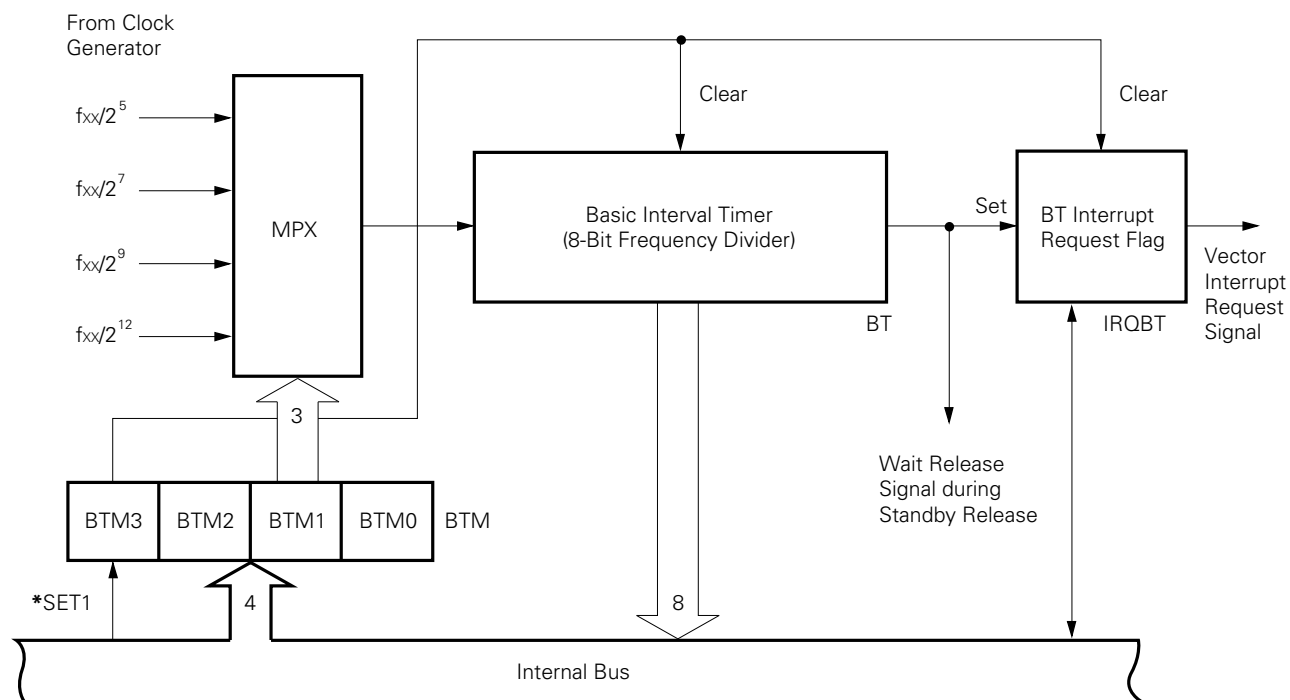


5.4 BASIC INTERVAL TIMER

The basic interval timer includes the following functions.

- It operates as an interval timer which generates reference time interrupts.
- It can be applied as a watchdog timer which detects when a program is out of control.
- Selects and counts wait times when the standby mode is released.
- It reads count contents.

Fig. 5-3 Basic Interval Timer Configuration



Remarks * indicates instruction execution.

5.5 TIMER/EVENT COUNTER

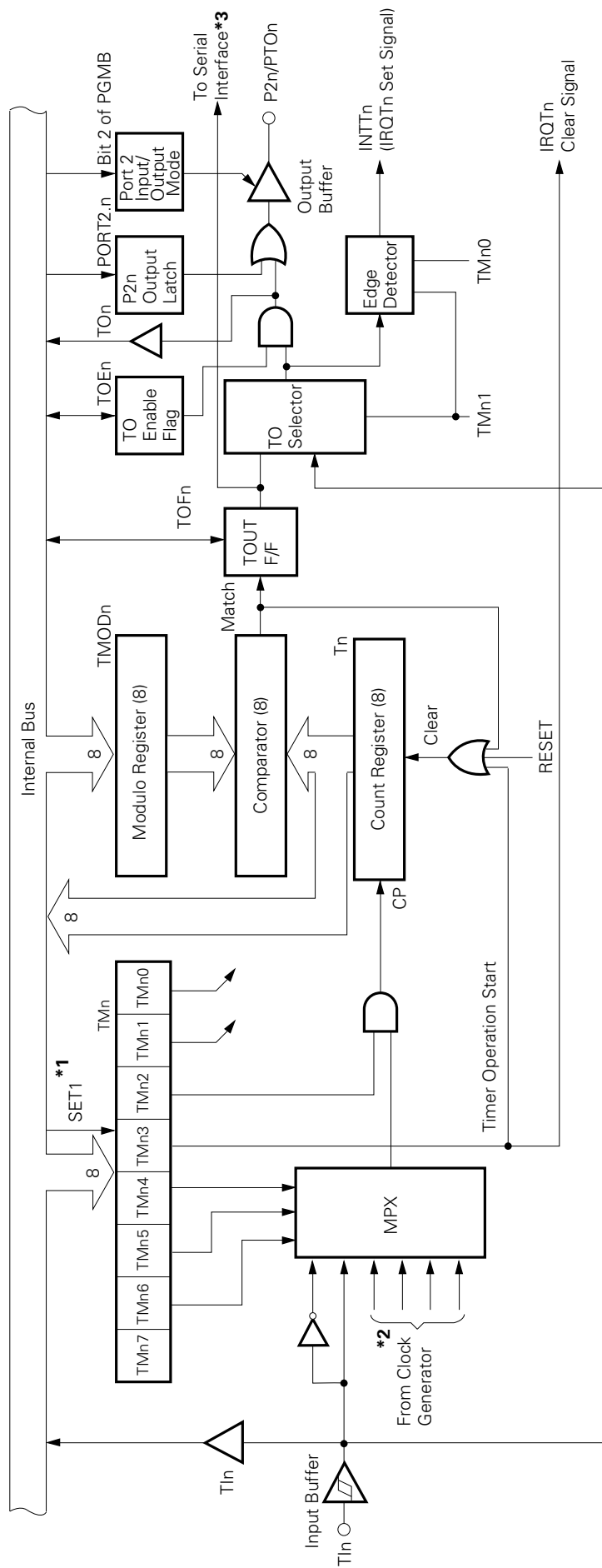
The μPD75116F incorporates two internal timer/event counter channels.

Timer/event counter channel 0 and channel 1 differ only in selectable count pulse (CP) and clock supply function to serial interface and are the same in other configurations and functions.

The functions of the timer/event counter are as follows.

- Operates as a programmable interval timer.
- Outputs square waves in the desired frequency to the PTO_n pin.
- Operates as an event counter.
- Use of TIn pin as an external interrupt input pin.
- Divides the TIn pin input into N divisions and outputs it to the PTO_n pin (frequency divider operation).
- Supplies a serial shift clock to the serial interface circuit. (channel 0 only)
- Count status read function.

Fig. 5-4 Timer/Event Counter Block Diagram (n = 0, 1)



* 1. SET1 : Instruction execution.

2. For details, see Fig. 5-1.

3. The serial interface signal is output only from timer/event counter channel 0.

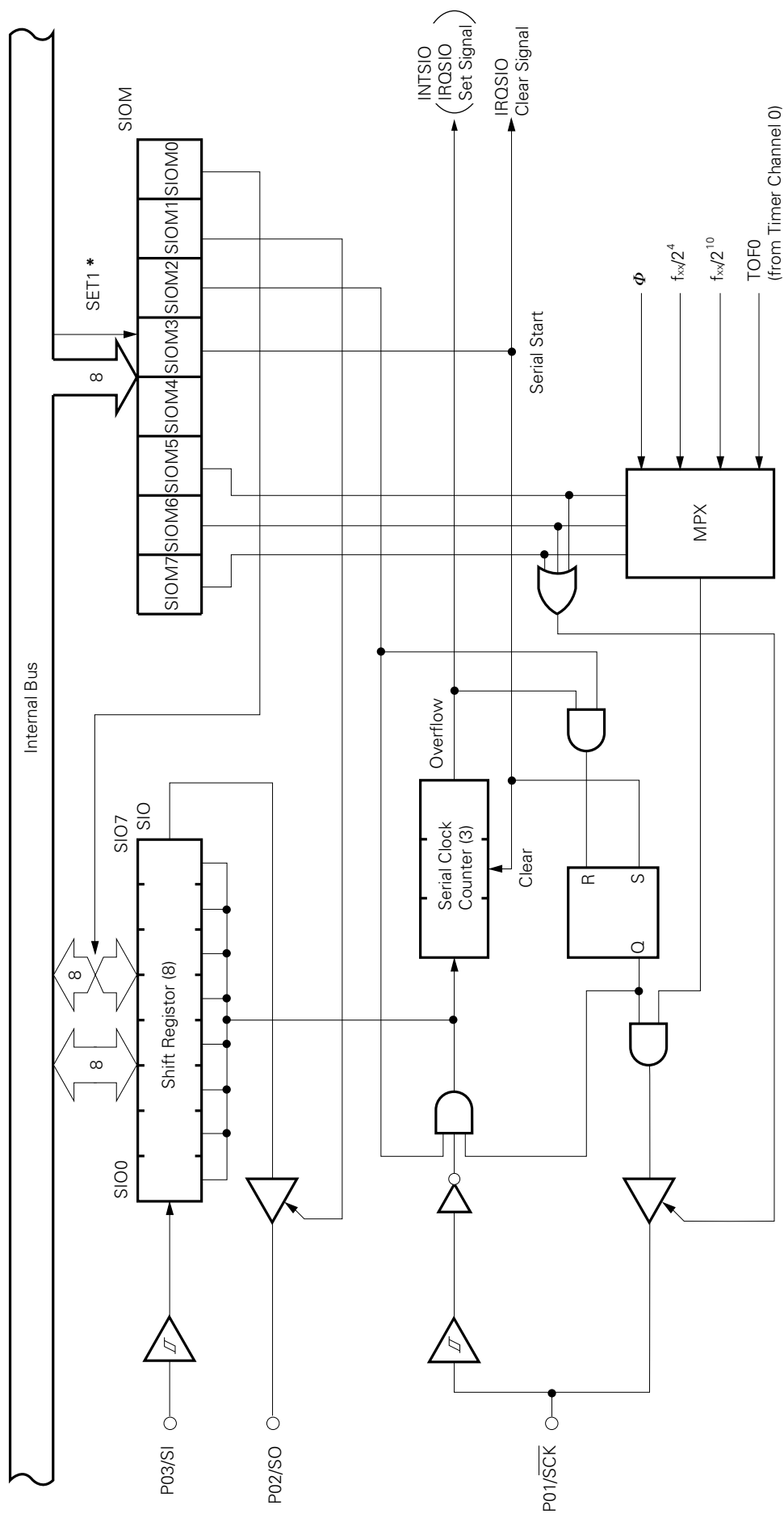
5.6 SERIAL INTERFACE

The μ PD75116F incorporates the clocked 8-bit serial interface. There are the following two modes of serial interface.

- 3-wire serial I/O mode (MSB-first/LSB-first switchable)
- Operation stop mode

In the 3-wire serial I/O mode, the μ PD75116F can be connected with the 75X series, 78K series and various kinds of I/O devices.

Fig. 5-5 Serial Interface Block Diagram



* SET1 : instruction execution

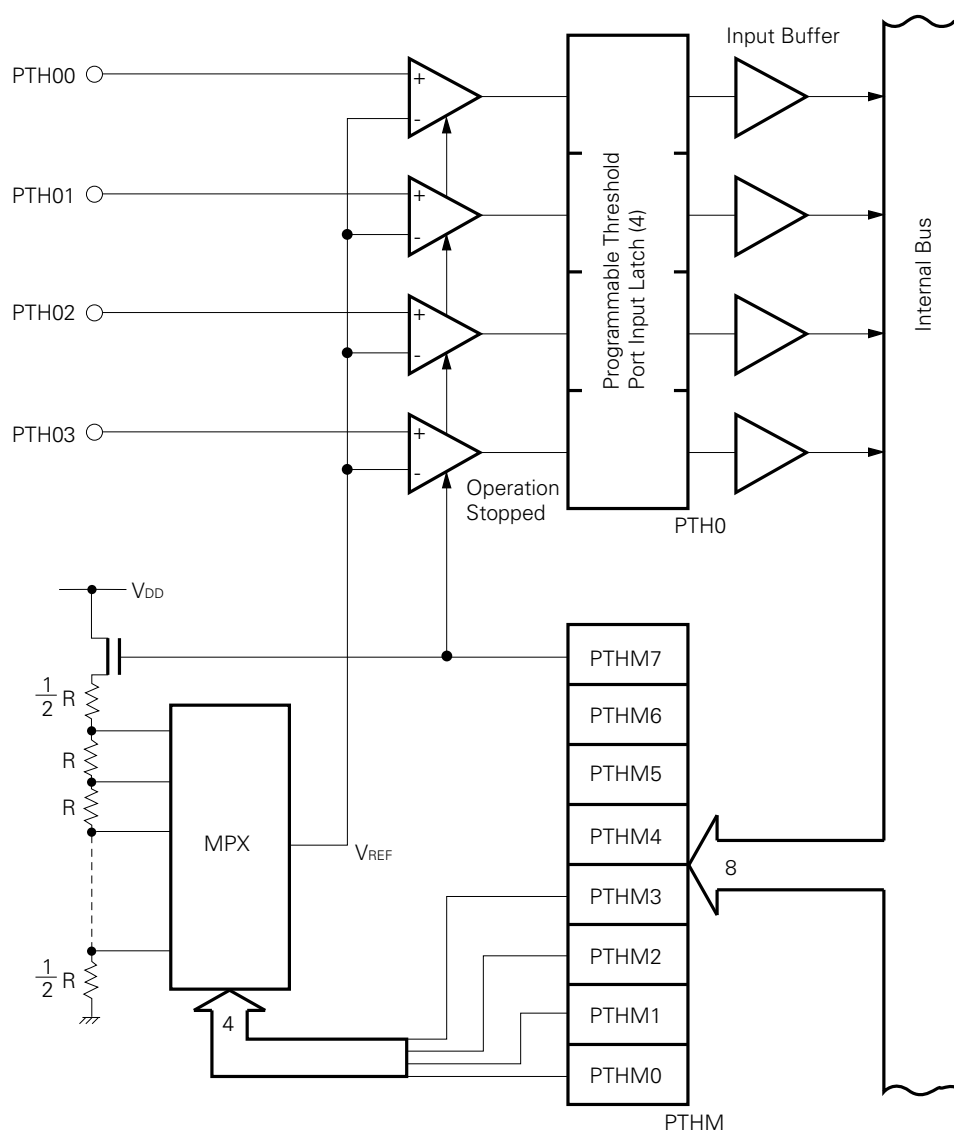
5.7 PROGRAMMABLE THRESHOLD PORT (ANALOG INPUT PORT)

The μ PD75116F is provided with 4-bit analog input pins (PTH00 to PTH03) for which the threshold voltage can be changed. These pins have a configuration as shown in Fig. 5-6.

The threshold voltage (V_{REF}) can be selected in 16 ways ($V_{DD} \times \frac{0.5}{16} \sim V_{DD} \times \frac{15.5}{16}$) and analog signals can be directly input.

This port can also be used as a digital signal input port by selecting $V_{DD} \times 7.5/16$ as V_{REF} .

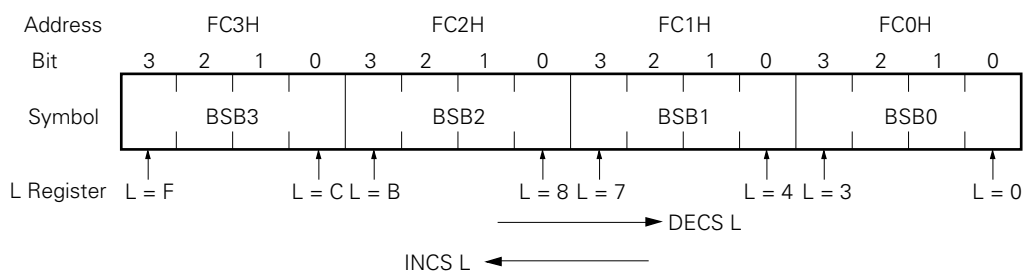
Fig. 5-6 Programmable Threshold Port Block Diagram



5.8 BIT SEQUENTIAL BUFFER 16 BITS

Bit manipulation of the bit sequential buffer is the bit manipulation special data memory. Since, in particular, the bit manipulation can easily be performed by changing sequentially address and bit specification, it is convenient when processing data comprising a large number of bits bit-wise.

Fig. 5-7 Bit Sequential Buffer Format



Remarks In pmem. @L addressing, the specified bit moves according to the L register.

6. INTERRUPT FUNCTION

The μPD75116F has 7 interrupt sources. Multiple interrupts with priority is are also possible.
Two test sources are also provided. The test sources are edge detection testable inputs.

Table 6-1 Interrupt Sources

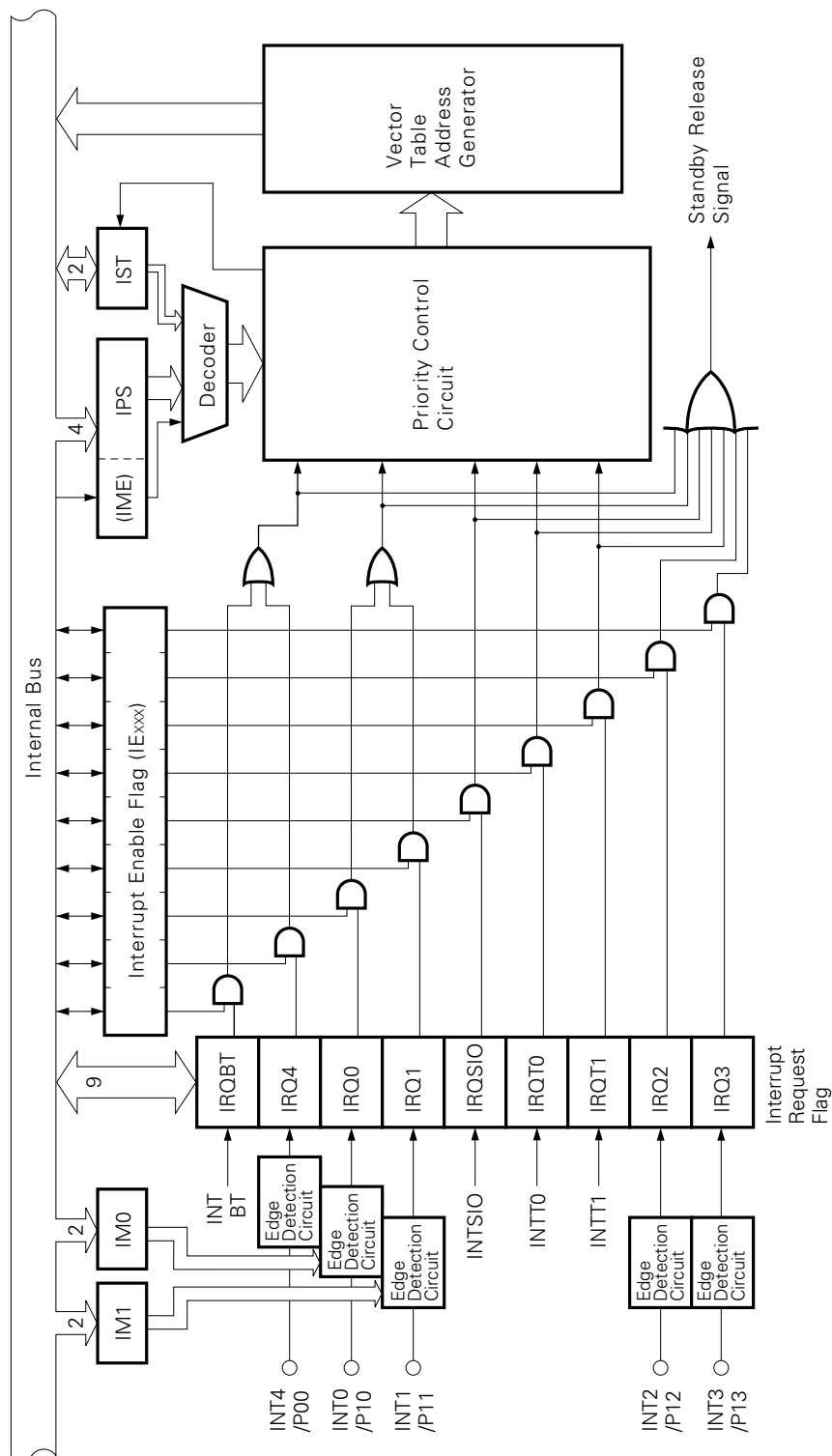
Interrupt Source		Internal/External	Interrupt Order*1	Vector Interrupt Request Signal (Vector Table Address)
INTBT (standard time interval signal from basic interval timer)		Internal	1	VRQ1 (0002H)
INT4 (both rising edge and falling edge detection)		External		
INT0	(rising edge and falling edge detection selection)	External	2	VRQ2 (0004H)
INT1		External		
INTSIO (serial data transfer end signal)		Internal	3	VRQ3 (0006H)
INTT0 (match signal from timer/event counter# 0 or TI0 input edge detection)		Internal/external	4	VRQ4 (0008H)
INTT1 (match signal from timer/event counter# 1 or TI1 input edge detection)		Internal/external	5	VRQ5 (000AH)
INT2*2 (rising edge detection)		External	Testable input signal (Set IRQ2 and IRQ3)	
INT3*2 (rising edge detection)				

- * 1. The interrupt order is the priority order when multiple interrupt requests are generated simultaneously.
2. INT2 and INT3 are of test sources . These are affected by interrupt enable flags in the same way as interrupt sources, but do not generate vector interrupts.

The μPD75116F interrupt control circuit has the following functions:

- Hardware control vector interrupt function that can control interrupt acceptance by interrupt enable flag (IExxx) and interrupt master enable flag (IME).
- Arbitrary setting of interrupt start address.
- Multiple interruption function by which priority can be specified using the interrupt priority selection register (IPS).
- Interrupt request flag (IRQxxx) test function (interrupt generation confirmation by software possible).
- Standby mode release (selection of interrupt that releases the standby mode by interrupt enable flag possible).

Fig. 6-1 Interrupt Control Circuit Block Diagram



7. STANDBY FUNCTION

To reduce the power consumption during program wait, the μ PD75116F has two standby modes (STOP mode and HALT mode).

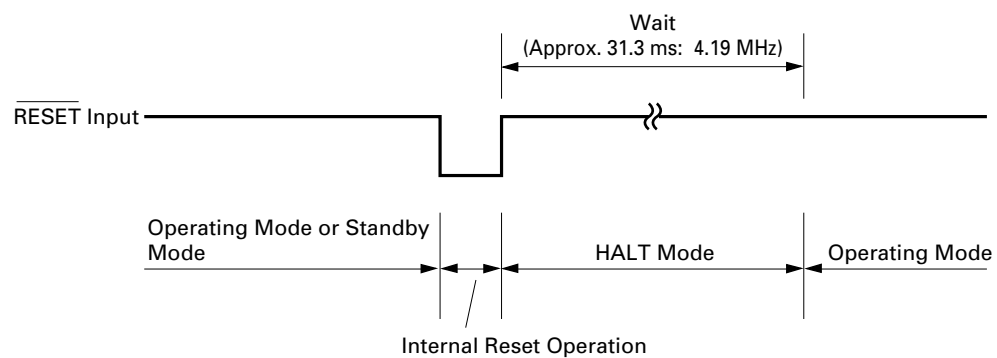
Table 7-1 Standby Mode Setting and Operation Status

		STOP Mode	HALT Mode
Setting instruction		STOP instruction	HALT instruction
Operation Status	Clock generator circuit	System clock oscillation stopped	Only CPU clock Φ stopped
	Basic interval timer	Operation stopped	Operable (IRQBT set at reference time intervals)
	Serial interface	Operation possible only when the external SCK input and T00 output (when timer/event counter 0 is external T10 input) are selected as a serial clock	Operation possible if a clock other than Φ is specified as a serial clock
	Timer/event counter	Operable only when T1n pin input specified as count clock	Operation possible
	Clock output circuit	Operation stopped	Except CPU clock Φ , output possible.
	External interrupt	Operation of INT0 to INT4 possible	
	CPU	Operation stopped	Operation stopped
Release signal		Interrupt request signal from operable hardware enabled by interrupt enable flag, or RESET input	

8. RESET FUNCTION

The reset operation timing is shown in Fig. 8-1.

Fig. 8-1 Reset Operation by $\overline{\text{RESET}}$ Input



The state of hardware after reset operation is as shown in Table 8-1.

Table 8-1 Status of Each Hardware after Resetting

Hardware		$\overline{\text{RESET}}$ Input in Standby Mode	$\overline{\text{RESET}}$ Input during Operation
Program counter (PC)	μ PD75108F	Low-order 5 bits of program memory address 0000H are set in PC ₁₂ to PC ₈ and the contents of address 0001H are set in PC ₇ to PC ₀ .	Same as left
	μ PD75112F μ PD75116F	Low-order 6 bits of program memory address 0000H are set in PC ₁₃ to PC ₈ and the contents of address 0001H are set in PC ₇ to PC ₀ .	
PSW	Carry flag (CY)	Held	Undefined
	Skip flag (SK0 to SK2)	0	0
	Interrupt status flag (IST0, IST1)	0	0
	Bank enable flag (MBE, RBE)	Sets program memory address 0000H bit 6 and bit 7 to RBE and MBE, respectively.	Same as left
Stack pointer (SP)		Undefined	Undefined
Data memory (RAM)		Held*	Undefined
General register (X, A, H, L, D, E, B, C)		Held	Undefined
Bank selection register (MBS, RBS)		0, 0	0, 0
Basic interval timer	Counter (BT)	Undefined	Undefined
	Mode register (BTM)	0	0
Timer/event counter (n = 0, 1)	Counter (Tn)	0	0
	Modulo register (TMODn)	FFH	FFH
	Mode register (TMn)	0	0
	TOEn, TOFn	0, 0	0, 0
Serial interface	Shift register (SIO)	Held	Undefined
	Mode register (SIOM)	0	0
Clock generator, clock output circuit	Processor clock control register (PCC)	0	0
	Clock output mode register (CLOM)	0	0
Interrupt	Interrupt request flag (IRQ _{xxx})	Reset (0)	Reset (0)
	Interrupt enable flag (IE _{xxx})	0	0
	Priority selection register (IPS)	0	0
	INT0, 1 mode registers (IM0, IM1)	0, 0	0, 0
Digital port	Output buffer	OFF	OFF
	Output latch	Clear (0)	Clear (0)
	I/O mode register (PMGA, B, C)	0	0
Analog port	PTH00 to 03 input latch	Undefined	Undefined
	Mode register (PTHM)	0	0
Bit sequential buffer (BSB0 to BSB3)		0	0

* Data of data memory addresses 0F8H to 0FDH becomes undefined by $\overline{\text{RESET}}$ input.

9. INSTRUCTION SET

(1) Operand identifier and description

The operand is described in the operand field of each instruction in accordance with the description for the operand identifier of the instruction. (For details, refer to **RA75X Assembler Package User's Manual Language Volume (EEU-730)**.) When there are multiple elements in the description, one of the elements is selected. Upper case letters and symbols (+,-) are keywords and are described unchanged.

Various register or flag symbols can be used as a label instead of mem, fmem, pmem, bit, etc. (For details, refer to **μPD75116 User's Manual (IEM-922)**.) However, there are restrictions on the labels for which fmem and pmem can be used.

Identifier	Description	
reg	X, A, B, C, D, E, H, L	
reg1	X, B, C, D, E, H, L	
rp	XA, BC, DE, HL	
rp1	BC, DE, HL	
rp2	BC, DE	
rp'	XA, BC, DE, HL, XA', BC', DE', HL'	
rp'1	BC, DE, HL, XA', BC', DE', HL'	
rpa	HL, HL+, HL-, DE, DL	
rpa1	DE, DL	
n4	4-bit immediate data or label	
n8	8-bit immediate data or label	
mem	8-bit immediate data or label*	
bit	2-bit immediate data or label	
fmem	FB0H to FBFH, FF0H to FFFH immediate data or label	
pmem	FC0H to FFFH immediate data or label	
addr	μPD75108F	0000H to 1F7FH immediate data or label
	μPD75112F	0000H to 2F7FH immediate data or label
	μPD75116F	0000H to 3F7FH immediate data or label
caddr	12-bit immediate data or label	
faddr	11-bit immediate data or label	
taddr	20H to 7FH immediate data (however, bit0 = 0) or label	
PORTn	PORT 0 to PORT 9, PORT12 to PORT14	
IExxx	IEBT, IESIO, IET0, IET1, IE0 to IE4	
RBn	RB0 to RB3	
MBn	MB0, MB1, MB15	

* In the case of the 8-bit data processing, an even address only can be described for mem.

(2) Operation description legend

A	: A register; 4-bit accumulator
B	: B register
C	: C register
D	: D register
E	: E register
H	: H register
L	: L register
X	: X register
XA	: Register pair (XA); 8-bit accumulator
BC	: Register pair (BC)
DE	: Register pair (DE)
HL	: Register pair (HL)
XA'	: Extension register pair (XA')
BC'	: Extension register pair (BC')
DE'	: Extension register pair (DE')
HL'	: Extension register pair (HL')
PC	: Program counter
SP	: Stack pointer
CY	: Carry flag; bit accumulator
PSW	: Program status word
MBE	: Memory bank enable flag
RBE	: Register bank enable flag
PORT _n	: Port _n (n = 0 to 9, 12 to 14)
IME	: Interrupt master enable flag
IPS	: Interrupt priority selection register
IE _{xxx}	: Interrupt enable flag
RBS	: Register bank selection register
MBS	: Memory bank selection register
PCC	: Processor clock control register
.	: Address, bit delimiter
(xx)	: Contents addressed by xx
xxH	: Hexadecimal data

(3) Description of addressing area field symbols

*1	MB = MBE • MBS (MBS = 0, 1, 15)	Data memory addressing
*2	MB = 0	
*3	MBE = 0 : MB = 0 (00H to 7FH) MB = 15 (80H to FFH) MBE = 1 : MB = MBS (MBS = 0, 1, 15)	
*4	MB = 15, fmem = FB0H to FBFH, FF0H to FFFH	
*5	MB = 15, pmem = FC0H to FFFH	
*6	μ PD75108F : addr = 0000H to 1F7FH μ PD75112F : addr = 0000H to 2F7FH μ PD75116F : addr = 0000H to 3F7FH	Program memory addressing
*7	addr = (Current PC) –15 to (Current PC) + 16	
*8	μ PD75108F : caddr = 0000H to 0FFFH (PC ₁₂ = 0) or = 1000H to 1F7FH (PC ₁₂ = 1) μ PD75112F : caddr = 0000H to 0FFFH (PC ₁₃ , PC ₁₂ = 00B) or = 1000H to 1FFFH (PC ₁₃ , PC ₁₂ = 01B) or = 2000H to 2F7FH (PC ₁₃ , PC ₁₂ = 10B) μ PD75116F : caddr = 0000H to 0FFFH (PC ₁₃ , PC ₁₂ = 00B) or = 1000H to 1FFFH (PC ₁₃ , PC ₁₂ = 01B) or = 2000H to 2FFFH (PC ₁₃ , PC ₁₂ = 10B) or = 3000H to 3F7FH (PC ₁₃ , PC ₁₂ = 11B)	
*9	faddr = 0000H to 07FFH	
*10	taddr = 0020H to 007FH	

- Remarks**
1. MB indicates the accessible memory bank.
 2. For *2, MB = 0 without regard to MBE and MBS.
 3. For *4 and *5, MB = 15 without regard to MBE and MBS.
 4. *6 to *10 indicate the addressable area.

(4) Explanation of machine cycle field

S shows the number of machine cycles required when skip is performed by an instruction with skip. The value of S changes as follows:

- No skip S = 0
- When instruction to be skipped is 1-byte or 2-byte instruction S = 1
- When instruction to be skipped is 3-byte instruction (BR !addr, CALL !addr instructions) S = 2

Note One machine cycle is required to skip a GETI instruction.

One machine cycle is equivalent to one cycle (= tcy) of the CPU clock ϕ . Three times can be selected by PCC setting.

Instruction Group	Mnemonic	Operands	Bytes	Machine Cycles	Operation	Addressing Area	Skip Condition
Transfer	MOV	A, #n4	1	1	$A \leftarrow n4$		Stack A
		reg1, #n4	2	2	$reg1 \leftarrow n4$		
		XA, #n8	2	2	$XA \leftarrow n8$		Stack A
		HL, #n8	2	2	$HL \leftarrow n8$		Stack B
		rp2, #n8	2	2	$rp2 \leftarrow n8$		
		A, @HL	1	1	$A \leftarrow (HL)$	*1	
		A, @HL+	1	2 + S	$A \leftarrow (HL)$, then $L \leftarrow L + 1$	*1	L = 0
		A, @HL-	1	2 + S	$A \leftarrow (HL)$, then $L \leftarrow L - 1$	*1	L = FH
		A, @rpa1	1	1	$A \leftarrow (rpa1)$	*2	
		XA, @HL	2	2	$XA \leftarrow (HL)$	*1	
		@HL, A	1	1	$(HL) \leftarrow A$	*1	
		@HL, XA	2	2	$(HL) \leftarrow XA$	*1	
		A, mem	2	2	$A \leftarrow (mem)$	*3	
		XA, mem	2	2	$XA \leftarrow (mem)$	*3	
		mem, A	2	2	$(mem) \leftarrow A$	*3	
		mem, XA	2	2	$(mem) \leftarrow XA$	*3	
		A, reg	2	2	$A \leftarrow reg$		
		XA, rp'	2	2	$XA \leftarrow rp'$		
		reg1, A	2	2	$reg1 \leftarrow A$		
		rp'1, XA	2	2	$rp'1 \leftarrow XA$		
	XCH	A, @HL	1	1	$A \leftrightarrow (HL)$	*1	
		A, @HL+	1	2 + S	$A \leftrightarrow (HL)$, then $L \leftarrow L + 1$	*1	L = 0
		A, @HL-	1	2 + S	$A \leftrightarrow (HL)$, then $L \leftarrow L - 1$	*1	L = FH
		A, @rpa1	1	1	$A \leftrightarrow (rpa1)$	*2	
		XA, @HL	2	2	$XA \leftrightarrow (HL)$	*1	
		A, mem	2	2	$A \leftrightarrow (mem)$	*3	
		XA, mem	2	2	$XA \leftrightarrow (mem)$	*3	
		A, reg1	1	1	$A \leftrightarrow reg1$		
		XA, rp'	2	2	$XA \leftrightarrow rp'$		
Table Reference	MOVT	XA, @PCDE	1	3	• μPD75108F $XA \leftarrow (PC_{12-8} + DE)_{ROM}$		
					• μPD75112F, 75116F $XA \leftarrow (PC_{13-8} + DE)_{ROM}$		
		XA, @PCXA	1	3	• μPD75108F $XA \leftarrow (PC_{12-8} + XA)_{ROM}$		
					• μPD75112F, 75116F $XA \leftarrow (PC_{13-8} + XA)_{ROM}$		

Instruction Group	Mnemonic	Operands	Bytes	Machine Cycles	Operation	Addressing Area	Skip Condition
Bit transfer	MOV1	CY, fmem.bit	2	2	$CY \leftarrow (fmem.bit)$	*4	
		CY, pmem.@L	2	2	$CY \leftarrow (pmem_{7-2} + L_{3-2}.bit(L_{1-0}))$	*5	
		CY, @H+mem.bit	2	2	$CY \leftarrow (H + mem_{3-0}.bit)$	*1	
		fmem.bit, CY	2	2	$(fmem.bit) \leftarrow CY$	*4	
		pmem.@L, CY	2	2	$(pmem_{7-2} + L_{3-2}.bit(L_{1-0})) \leftarrow CY$	*5	
		@H+mem.bit, CY	2	2	$(H + mem_{3-0}.bit) \leftarrow CY$	*1	
Operations	ADDS	A, #n4	1	1 + S	$A \leftarrow A + n4$		carry
		XA, #n8	2	2 + S	$XA \leftarrow XA + n8$		carry
		A, @HL	1	1 + S	$A \leftarrow A + (HL)$	*1	carry
		XA, rp'	2	2 + S	$XA \leftarrow XA + rp'$		carry
		rp'1, XA	2	2 + S	$rp'1 \leftarrow rp'1 + XA$		carry
	ADDC	A, @HL	1	1	$A, CY \leftarrow A + (HL) + CY$	*1	
		XA, rp'	2	2	$XA, CY \leftarrow XA + rp' + CY$		
		rp'1, XA	2	2	$rp'1, CY \leftarrow rp'1 + XA + CY$		
	SUBS	A, @HL	1	1 + S	$A \leftarrow A - (HL)$	*1	borrow
		XA, rp'	2	2 + S	$XA \leftarrow XA - rp'$		borrow
		rp'1, XA	2	2 + S	$rp'1 \leftarrow rp'1 - XA$		borrow
	SUBC	A, @HL	1	1	$A, CY \leftarrow A - (HL) - CY$	*1	
		XA, rp'	2	2	$XA, CY \leftarrow XA - rp' - CY$		
		rp'1, XA	2	2	$rp'1, CY \leftarrow rp'1 - XA - CY$		
	AND	A, #n4	2	2	$A \leftarrow A \wedge n4$		
		A, @HL	1	1	$A \leftarrow A \wedge (HL)$	*1	
		XA, rp'	2	2	$XA \leftarrow XA \wedge rp'$		
		rp'1, XA	2	2	$rp'1 \leftarrow rp'1 \wedge XA$		
	OR	A, #n4	2	2	$A \leftarrow A \vee n4$		
		A, @HL	1	1	$A \leftarrow A \vee (HL)$	*1	
		XA, rp'	2	2	$XA \leftarrow XA \vee rp'$		
		rp'1, XA	2	2	$rp'1 \leftarrow rp'1 \vee XA$		
	XOR	A, #n4	2	2	$A \leftarrow A \vee n4$		
		A, @HL	1	1	$A \leftarrow A \vee (HL)$	*1	
		XA, rp'	2	2	$XA \leftarrow XA \vee rp'$		
		rp'1, XA	2	2	$rp'1 \leftarrow rp'1 \vee XA$		

Instruction Group	Mnemonic	Operands	Bytes	Machine Cycles	Operation	Addressing Area	Skip Condition
Accumulator manipulation	RORC	A	1	1	$CY \leftarrow A_0, A_3 \leftarrow CY, A_{n-1} \leftarrow A_n$		
	NOT	A	2	2	$A \leftarrow \bar{A}$		
Increment/decrement	INCS	reg	1	1 + S	$reg \leftarrow reg + 1$		reg = 0
		rp1	1	1 + S	$rp1 \leftarrow rp1 + 1$		rp1 = 00H
		@HL	2	2 + S	$(HL) \leftarrow (HL) + 1$	*1	(HL) = 0
		mem	2	2 + S	$(mem) \leftarrow (mem) + 1$	*3	(mem) = 0
	DECS	reg	1	1 + S	$reg \leftarrow reg - 1$		reg = FH
		rp'	2	2 + S	$rp' \leftarrow rp' - 1$		rp' = FFH
Comparison	SKE	reg, #n4	2	2 + S	Skip if reg = n4		reg = n4
		@HL, #n4	2	2 + S	Skip if (HL) = n4	*1	(HL) = n4
		A, @HL	1	1 + S	Skip if A = (HL)	*1	A = (HL)
		XA, @HL	2	2 + S	Skip if XA = (HL)	*1	XA = (HL)
		A, reg	2	2 + S	Skip if A = reg		A = reg
		XA, rp'	2	2 + S	Skip if XA = rp'		XA = rp'
Carry flag manipulation	SET1	CY	1	1	$CY \leftarrow 1$		
	CLR1	CY	1	1	$CY \leftarrow 0$		
	SKT	CY	1	1 + S	Skip if CY = 1		CY = 1
	NOT1	CY	1	1	$CY \leftarrow \bar{CY}$		
Memory bit manipulation	SET1	mem.bit	2	2	$(mem.bit) \leftarrow 1$	*3	
		fmem.bit	2	2	$(fmem.bit) \leftarrow 1$	*4	
		pmem.@L	2	2	$(pmem_{7-2} + L_{3-2}.bit(L_{1-0})) \leftarrow 1$	*5	
		@H + mem.bit	2	2	$(H + mem_{3-0}.bit) \leftarrow 1$	*1	
	CLR1	mem.bit	2	2	$(mem.bit) \leftarrow 0$	*3	
		fmem.bit	2	2	$(fmem.bit) \leftarrow 0$	*4	
		pmem.@L	2	2	$(pmem_{7-2} + L_{3-2}.bit(L_{1-0})) \leftarrow 0$	*5	
		@H + mem.bit	2	2	$(H + mem_{3-0}.bit) \leftarrow 0$	*1	
	SKT	mem.bit	2	2 + S	Skip if (mem.bit) = 1	*3	(mem.bit) = 1
		fmem.bit	2	2 + S	Skip if (fmem.bit) = 1	*4	(fmem.bit) = 1
		pmem.@L	2	2 + S	Skip if $(pmem_{7-2} + L_{3-2}.bit(L_{1-0})) = 1$	*5	(pmem.@L) = 1
		@H + mem.bit	2	2 + S	Skip if $(H + mem_{3-0}.bit) = 1$	*1	(@H + mem.bit) = 1
	SKF	mem.bit	2	2 + S	Skip if (mem.bit) = 0	*3	(mem.bit) = 0
		fmem.bit	2	2 + S	Skip if (fmem.bit) = 0	*4	(fmem.bit) = 0
		pmem.@L	2	2 + S	Skip if $(pmem_{7-2} + L_{3-2}.bit(L_{1-0})) = 0$	*5	(pmem.@L) = 0
		@H + mem.bit	2	2 + S	Skip if $(H + mem_{3-0}.bit) = 0$	*1	(@H + mem.bit) = 0
	SKTCLR	fmem.bit	2	2 + S	Skip if (fmem.bit) = 1 and clear	*4	(fmem.bit) = 1
		pmem.@L	2	2 + S	Skip if $(pmem_{7-2} + L_{3-2}.bit(L_{1-0})) = 1$ and clear	*5	(pmem.@L) = 1
		@H + mem.bit	2	2 + S	Skip if $(H + mem_{3-0}.bit) = 1$ and clear	*1	(@H + mem.bit) = 1

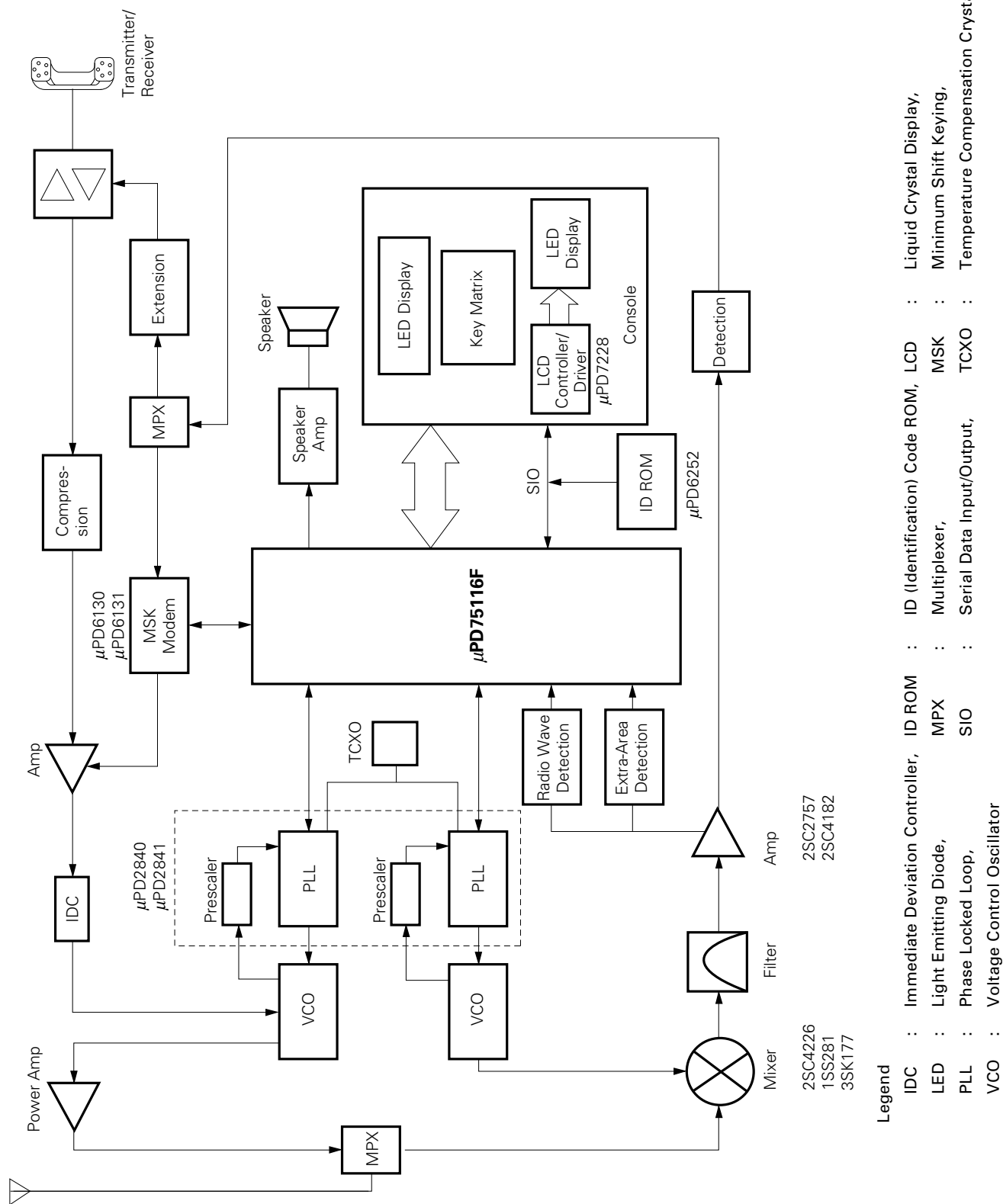
Instruction Group	Mnemonic	Operands	Bytes	Machine Cycles	Operation	Addressing Area	Skip Condition
Memory bit manipulation	AND1	CY, fmem.bit	2	2	$CY \leftarrow CY \wedge (\text{fmem.bit})$	*4	
		CY, pmem.@L	2	2	$CY \leftarrow CY \wedge (\text{pmem}_{7-2} + L_{3-2}.\text{bit} (L_{1-0}))$	*5	
		CY, @H + mem.bit	2	2	$CY \leftarrow CY \wedge (H + \text{mem}_{3-0}.\text{bit})$	*1	
	OR1	CY, fmem.bit	2	2	$CY \leftarrow CY \vee (\text{fmem.bit})$	*4	
		CY, pmem.@L	2	2	$CY \leftarrow CY \vee (\text{pmem}_{7-2} + L_{3-2}.\text{bit} (L_{1-0}))$	*5	
		CY, @H + mem.bit	2	2	$CY \leftarrow CY \vee (H + \text{mem}_{3-0}.\text{bit})$	*1	
	XOR1	CY, fmem.bit	2	2	$CY \leftarrow CY \nabla (\text{fmem.bit})$	*4	
		CY, pmem.@L	2	2	$CY \leftarrow CY \nabla (\text{pmem}_{7-2} + L_{3-2}.\text{bit} (L_{1-0}))$	*5	
		CY, @H + mem.bit	2	2	$CY \leftarrow CY \nabla (H + \text{mem}_{3-0}.\text{bit})$	*1	
Branch	BR	addr	—	—	• μPD75108F $PC_{12-0} \leftarrow \text{addr}$ (The assembler selects the optimum instruction from among the BR !addr, BRCB !caddr, and BR \$addr instructions.) • μPD75112F, 75116F $PC_{13-0} \leftarrow \text{addr}$ (The assembler selects the optimum instruction from among the BR !addr, BRCB !caddr, and BR \$addr instructions.)	*6	
		!addr	3	3	• μPD75108F $PC_{12-0} \leftarrow \text{addr}$ • μPD75112F, 75116F $PC_{13-0} \leftarrow \text{addr}$	*6	
		\$addr	1	2	• μPD75108F $PC_{12-0} \leftarrow \text{addr}$ • μPD75112F, 75116F $PC_{13-0} \leftarrow \text{addr}$	*7	
	BRCB	!caddr	2	2	• μPD75108F $PC_{12-0} \leftarrow PC_{12} + \text{caddr}_{11-0}$ • μPD75112F, 75116F $PC_{13-0} \leftarrow PC_{13}, PC_{12} + \text{caddr}_{11-0}$	*8	
		PCDE	2	3	• μPD75108F $PC_{12-0} \leftarrow PC_{12-8} + DE$ • μPD75112F, 75116F $PC_{13-0} \leftarrow PC_{13-8} + DE$		
	BR	PCXA	2	3	• μPD75108F $PC_{12-0} \leftarrow PC_{12-8} + XA$ • μPD75112F, 75116F $PC_{13-0} \leftarrow PC_{13-8} + XA$		
		!addr	3	3	• μPD75108F $(SP-4) (SP-1) (SP-2) \leftarrow PC_{11-0}$ $(SP-3) \leftarrow MBE, RBE, 0, PC_{12}$ $PC_{12-0} \leftarrow \text{addr}, SP \leftarrow SP-4$ • μPD75112F, 75116F $(SP-4) (SP-1) (SP-2) \leftarrow PC_{11-0}$ $(SP-3) \leftarrow MBE, RBE, PC_{13}, PC_{12}$ $PC_{13-0} \leftarrow \text{addr}, SP \leftarrow SP-4$	*6	
	CALL	!addr	3	3	• μPD75108F $(SP-4) (SP-1) (SP-2) \leftarrow PC_{11-0}$ $(SP-3) \leftarrow MBE, RBE, 0, PC_{12}$ $PC_{12-0} \leftarrow \text{addr}, SP \leftarrow SP-4$ • μPD75112F, 75116F $(SP-4) (SP-1) (SP-2) \leftarrow PC_{11-0}$ $(SP-3) \leftarrow MBE, RBE, PC_{13}, PC_{12}$ $PC_{13-0} \leftarrow \text{addr}, SP \leftarrow SP-4$	*6	
		!addr	3	3	• μPD75108F $(SP-4) (SP-1) (SP-2) \leftarrow PC_{11-0}$ $(SP-3) \leftarrow MBE, RBE, 0, PC_{12}$ $PC_{12-0} \leftarrow \text{addr}, SP \leftarrow SP-4$ • μPD75112F, 75116F $(SP-4) (SP-1) (SP-2) \leftarrow PC_{11-0}$ $(SP-3) \leftarrow MBE, RBE, PC_{13}, PC_{12}$ $PC_{13-0} \leftarrow \text{addr}, SP \leftarrow SP-4$	*6	
		!addr	3	3	• μPD75108F $(SP-4) (SP-1) (SP-2) \leftarrow PC_{11-0}$ $(SP-3) \leftarrow MBE, RBE, 0, PC_{12}$ $PC_{12-0} \leftarrow \text{addr}, SP \leftarrow SP-4$ • μPD75112F, 75116F $(SP-4) (SP-1) (SP-2) \leftarrow PC_{11-0}$ $(SP-3) \leftarrow MBE, RBE, PC_{13}, PC_{12}$ $PC_{13-0} \leftarrow \text{addr}, SP \leftarrow SP-4$	*6	
Subroutine stack control	CALL	!addr	3	3	• μPD75108F $(SP-4) (SP-1) (SP-2) \leftarrow PC_{11-0}$ $(SP-3) \leftarrow MBE, RBE, 0, PC_{12}$ $PC_{12-0} \leftarrow \text{addr}, SP \leftarrow SP-4$ • μPD75112F, 75116F $(SP-4) (SP-1) (SP-2) \leftarrow PC_{11-0}$ $(SP-3) \leftarrow MBE, RBE, PC_{13}, PC_{12}$ $PC_{13-0} \leftarrow \text{addr}, SP \leftarrow SP-4$	*6	

Instruction Group	Mnemonic	Operands	Bytes	Machine Cycles	Operation	Addressing Area	Skip Condition
Subroutine stack control	CALLF	!faddr	2	2	• μPD75108F $(SP - 4) (SP - 1) (SP - 2) \leftarrow PC_{11-0}$ $(SP - 3) \leftarrow MBE, RBE, 0, PC_{12}$ $PC_{12-0} \leftarrow 00, faddr, SP \leftarrow SP - 4$	*9	
					• μPD75112F, 75116F $(SP - 4) (SP - 1) (SP - 2) \leftarrow PC_{11-0}$ $(SP - 3) \leftarrow MBE, RBE, PC_{13}, PC_{12}$ $PC_{13-0} \leftarrow 000, faddr, SP \leftarrow SP - 4$		
	RET		1	3	• μPD75108F $MBE, RBE, \times, PC_{12} \leftarrow (SP + 1)$ $PC_{11-0} \leftarrow (SP) (SP + 3) (SP + 2)$ $SP \leftarrow SP + 4$		
					• μPD75112F, 75116F $MBE, RBE, PC_{13}, PC_{12} \leftarrow (SP + 1)$ $PC_{11-0} \leftarrow (SP) (SP + 3) (SP + 2)$ $SP \leftarrow SP + 4$		
	RETS		1	3 + S	• μPD75108F $MBE, RBE, \times, PC_{12} \leftarrow (SP + 1)$ $PC_{11-0} \leftarrow (SP) (SP + 3) (SP + 2)$ $SP \leftarrow SP + 4, \text{ then skip unconditionally}$		Unconditional
					• μPD75112F, 75116F $MBE, RBE, PC_{13}, PC_{12} \leftarrow (SP + 1)$ $PC_{11-0} \leftarrow (SP) (SP + 3) (SP + 2)$ $SP \leftarrow SP + 4, \text{ then skip unconditionally}$		
	RETI		1	3	• μPD75108F $MBE, RBE, \times, PC_{12} \leftarrow (SP + 1)$ $PC_{11-0} \leftarrow (SP) (SP + 3) (SP + 2)$ $PSW \leftarrow (SP + 4) (SP + 5), SP \leftarrow SP + 6$		
					• μPD75112F, 75116F $MBE, RBE, PC_{13}, PC_{12} \leftarrow (SP + 1)$ $PC_{11-0} \leftarrow (SP) (SP + 3) (SP + 2)$ $PSW \leftarrow (SP + 4) (SP + 5), SP \leftarrow SP + 6$		
	PUSH	rp	1	1	$(SP - 1) (SP - 2) \leftarrow rp, SP \leftarrow SP - 2$		
		BS	2	2	$(SP - 1) \leftarrow MBS, (SP - 2) \leftarrow RBS, SP \leftarrow SP - 2$		
Interrupt control	EI		2	2	IME (IPS.3) $\leftarrow 1$		
		IExxx	2	2	IExxx $\leftarrow 1$		
	DI		2	2	IME (IPS.3) $\leftarrow 0$		
		IExxx	2	2	IExxx $\leftarrow 0$		

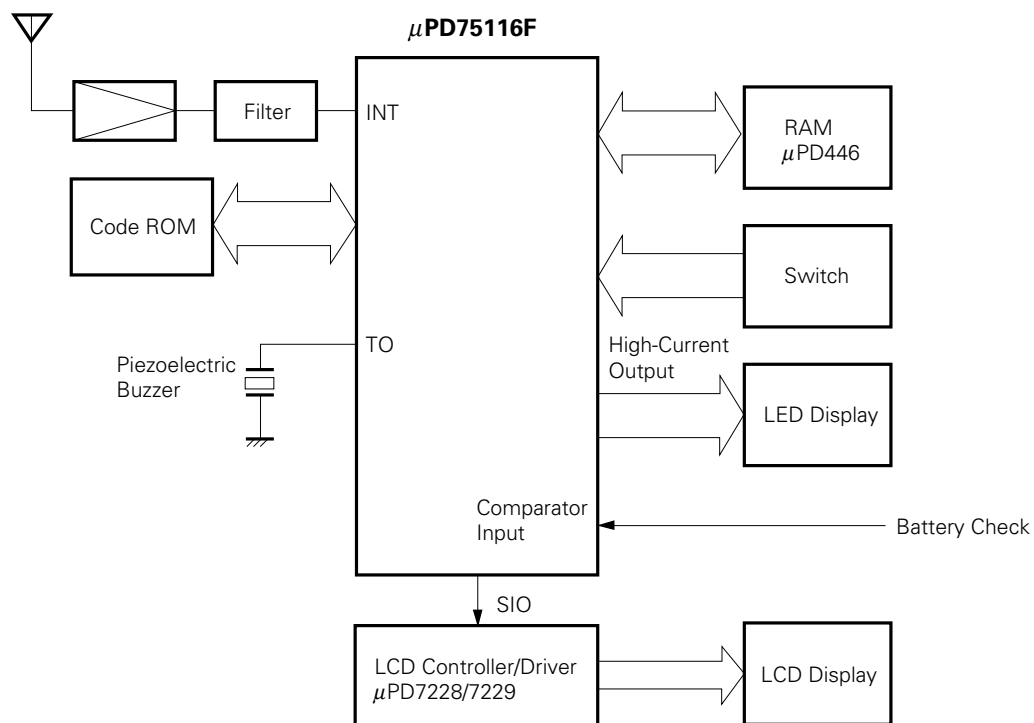
Instruction Group	Mnemonic	Operands	Bytes	Machine Cycles	Operation	Addressing Area	Skip Condition
Input/output	IN ^{*1}	A, PORT _n	2	2	$A \leftarrow \text{PORT}_n \quad (n = 0 \text{ to } 9, 12 \text{ to } 14)$		
		XA, PORT _n	2	2	$XA \leftarrow \text{PORT}_{n+1}, \text{PORT}_n \quad (n = 4, 6, 8, 12)$		
	OUT ^{*1}	PORT _n , A	2	2	$\text{PORT}_n \leftarrow A \quad (n = 2 \text{ to } 9, 12 \text{ to } 14)$		
		PORT _n , XA	2	2	$\text{PORT}_{n+1}, \text{PORT}_n \leftarrow XA \quad (n = 4, 6, 8, 12)$		
CPU control	HALT		2	2	Set HALT Mode ($\text{PCC}.2 \leftarrow 1$)		
	STOP		2	2	Set STOP Mode ($\text{PCC}.3 \leftarrow 1$)		
	NOP		1	1	No Operation		
Special	SELL	RB _n	2	2	$\text{RBS} \leftarrow n \quad (n = 0 \text{ to } 3)$		
		MB _n	2	2	$\text{MBS} \leftarrow n \quad (n = 0, 1, 15)$		
	GETI ^{*2}	taddr	1	3	• μPD75108F TBR Instruction $\text{PC}_{12-0} \leftarrow (\text{taddr})_{4-0} \leftarrow (\text{taddr} + 1)$	*10	
					TCALL Instruction $(\text{SP} - 4) (\text{SP} - 1) (\text{SP} - 2) \leftarrow \text{PC}_{11-0}$ $(\text{SP} - 3) \leftarrow \text{MBE}, \text{RBE}, 0, \text{PC}_{12}$ $\text{PC}_{12-0} \leftarrow (\text{taddr})_{4-0} \leftarrow (\text{taddr} + 1)$ $\text{SP} \leftarrow \text{SP} - 4$		
					Other than TBR and TCALL Instruction Execution of an instruction addressed at (taddr) and (taddr + 1)		Conforms to referenced instruction.
					• μPD75112F, 75116F TBR Instruction $\text{PC}_{13-0} \leftarrow (\text{taddr})_{5-0} \leftarrow (\text{taddr} + 1)$		
					TCALL Instruction $(\text{SP} - 4) (\text{SP} - 1) (\text{SP} - 2) \leftarrow \text{PC}_{11-0}$ $(\text{SP} - 3) \leftarrow \text{MBE}, \text{RBE}, 0, \text{PC}_{13}, \text{PC}_{12}$ $\text{PC}_{13-0} \leftarrow (\text{taddr})_{5-0} \leftarrow (\text{taddr} + 1)$ $\text{SP} \leftarrow \text{SP} - 4$		
					Other than TBR and TCALL Instruction Execution of an instruction addressed at (taddr) and (taddr + 1)		Conforms to referenced instruction.

- * 1. When executing the IN/OUT instruction, <MBE = 0> or <MBE = 1, MBS = 15> must be set.
 2. The TBR or TCALL instruction is a GETI instruction table definition assembler pseudo-instruction.

10.1 CORDLESS TELEPHONE (SUBSET)



10.2 DISPLAY PAGER



11. MASK OPTION SELECTION

The μ PD75116F has the following mask option to select whether or not a pull-up resistor is incorporated.

Pin	Mask Option
P120 to P123	Pull-up resistor can be incorporated bit-wise.
P130 to P133	
P140 to P143	

12. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

PARAMETER	SYMBOL	TEST CONDITIONS		RATING	UNIT
Supply voltage	V _{DD}			−0.3 to +5.5	V
Input voltage	V _{I1}	Except ports 12, 13 and 14		−0.3 to V _{DD} +0.3	V
	V _{I2} *1	Ports 12 to 14	Internal pull-up resistor	−0.3 to V _{DD} +0.3	V
			Open-drain	−0.3 to +11	V
Output voltage	V _O			−0.3 to V _{DD} +0.3	V
Output current high	I _{OH}	One pin		−15	mA
		All pins		−30	mA
Output current low	I _{OL} *2	One pin	Peak value	30	mA
			Effective value	15	mA
		Total of ports 0, 2 to 4, 12 to 14	Peak value	100	mA
			Effective value	60	mA
		Total of ports 5 to 9	Peak value	100	mA
			Effective value	60	mA
Operating temperature	T _{opt}			−40 to +60	°C
Storage temperature	T _{stg}			−65 to +150	°C

- * 1. When a voltage exceeding 10V is applied to ports 12, 13 and 14, the power supply impedance (pull-up resistor) should be 50KΩ or more.
2. Effective value should be calculated: [Effective value] = [Peak value] × $\sqrt{\text{duty}}$

Note Product quality may suffer if the absolute maximum rating is exceeded for even a single parameter or even momentarily.

The absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions which ensure that the absolute maximum ratings are not exceeded.

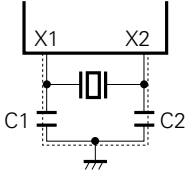
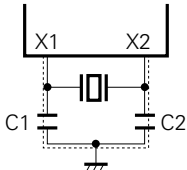
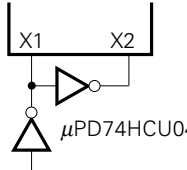
12.1 WHEN $T_a = -40$ to $+50$ °C, $V_{DD} = 2.7$ to 5.0 V

OPERATING VOLTAGE ($T_a = -40$ to $+50$ °C)

PARAMETER	TEST CONDITIONS	MIN.	MAX.	UNIT
CPU*1		*2	5.0	V
Programmable threshold port (comparator input)		4.5	5.0	V
Other hardware*1		2.7	5.0	V

- * 1. Except system clock oscillation circuit, programmable threshold port.
2. The operable supply voltage range depends on the cycle time. See "AC CHARACTERISTICS".

OSCILLATION CIRCUIT CHARACTERISTICS ($T_a = -40$ to $+50$ °C, $V_{DD} = 2.7$ to 5.0 V)

RESONATOR	RECOMMENDED CONSTANT	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Ceramic resonator		Oscillator frequency (f_{xx})*1	V_{DD} = Oscillation voltage range	2.0		5.0*3	MHz
		Oscillation stabilization time*2	After V_{DD} reaches MIN. of oscillation voltage range			4	ms
Crystal resonator		Oscillator frequency (f_{xx})*1		2.0	4.19	5.0*3	MHz
		Oscillation stabilization time*2	$V_{DD} = 4.5$ to 5.0 V			10	ms
						30	ms
External clock		X1 input frequency (f_x)*1		2.0		5.0*3	MHz
		X1 input high-/low-level width (t_{XH} , t_{XL})		100		250	ns

- * 1. Oscillator frequency and X1 input frequency indicate oscillation circuit characteristics only. See AC CHARACTERISTICS for instruction execution time.
2. The oscillation stabilization time is the time required for oscillation to stabilize after V_{DD} reaches MIN. of oscillation voltage range or the STOP mode is released.
3. When the oscillator frequency is $4.19 \text{ MHz} < f_{xx} \leq 5.0 \text{ MHz}$, PCC = 0011 should not be selected as the instruction execution time. If PCC = 0011 is selected, one machine cycle is less than $0.95 \mu\text{s}$ and the rated MIN. value of $0.95 \mu\text{s}$ is not observed.

Note When the clock oscillator is used, the following should be noted concerning wiring in the area in the figure enclosed by a dotted line to prevent the influence of wiring capacitance, etc. ★

- The wiring should be kept as short as possible.
- No other signal lines should be crossed.
- Keep away from lines carrying a high fluctuating current.
- The oscillator capacitor grounding point should always be at the same potential as V_{SS} . Do not connect to a ground pattern carrying a high current.
- A signal should be not taken from the oscillator.

RECOMMENDED OSCILLATION CIRCUIT CONSTANT
RECOMMENDED CERAMIC RESONATOR (Ta = -40 to +50 °C)

MANUFACTURER	PRODUCT NAME	EXTERNAL CAPACITANCE [pF]		OSCILLATION VOLTAGE RANGE [V]	
		C1	C2	MIN.	MAX.
Murata Mfg.	CSA 2.00MG	30	30	2.7	5.0
	CSA 4.19MG	30	30	3.0	5.0
	CSA 4.19MGU	30	30	2.7	5.0
	CST 4.19T	—	—	3.0	5.0
Kyocera	KBR-2.0MS	100	100	3.0	5.0
	KBR-4.0MS	33	33	3.0	5.0
	KBR-4.19MS	33	33	3.0	5.0
	KBR-4.9152M	33	33	3.0	5.0

RECOMMENDED CRYSTAL RESONATOR (Ta = -20 to +50 °C)

MANUFACTURER	PRODUCT NAME	EXTERNAL CAPACITANCE [pF]		OSCILLATION VOLTAGE RANGE [V]	
		C1	C2	MIN.	MAX.
Kinseki	HC-49/U	22	22	2.7	5.0

DC CHARACTERISTICS (Ta = -40 to +50 °C, VDD = 2.7 to 5.0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT		
Input voltage high	V _{IH1}	Other than below		0.7 V _{DD}		V _{DD}	V		
	V _{IH2}	Ports 0,1,Ti0, 1, $\overline{\text{RESET}}$		0.8 V _{DD}		V _{DD}	V		
	V _{IH3}	Ports 12 and 14	Internal pull-up resistor	0.7 V _{DD}		V _{DD}	V		
			Open-drain	0.7 V _{DD}		12	V		
	V _{IH4}	X1, X2		V _{DD} – 0.5		V _{DD}	V		
Input voltage low	V _{IL1}	Other than below		0		0.3 V _{DD}	V		
	V _{IL2}	Ports 0,1,Ti0, 1, $\overline{\text{RESET}}$		0		0.2 V _{DD}	V		
	V _{IL3}	X1, X2		0		0.4	V		
Output voltage high	V _{OH}	V _{DD} = 4.5 to 5.0 V, I _{OH} = –1 mA		V _{DD} – 1.0			V		
		I _{OH} = –100 μA		V _{DD} – 0.5			V		
Output voltage low	V _{OL}	V _{DD} = 4.5 to 5.0 V	Ports 0, 2 to 9, I _{OL} = 15 mA		0.35	2.0	V		
			Ports 12 to 14, I _{OL} = 10 mA		0.35	2.0	V		
		V _{DD} = 4.5 to 5.0 V, I _{OL} = 1.6 mA				0.4	V		
		I _{OL} = 400 μA				0.5	V		
Input leakage current high	I _{LIH1}	V _{IN} = V _{DD}	Other than below			3	μA		
	I _{LIH2}		X1, X2			20	μA		
	I _{LIH3}	V _{IV} = 10 V	Ports 12 to 14 (open-drain)			20	μA		
Input leakage current low	I _{LIL1}	V _{IN} = 0 V	Except X1, X2			–3	μA		
	I _{LIL2}		X1, X2			–20	μA		
Output leakage current high	I _{LOH1}	V _{OUT} = V _{DD}	Other than below			3	μA		
	I _{LOH2}	V _{OUT} = 10 V	Ports 12 to 14 (open-drain)			20	μA		
Output leakage current low	I _{LOL}	V _{OUT} = 0 V				–3	μA		
Internal pull-up resistor (mask option)	R _L	Ports 12 to 14	V _{DD} = 4.5 to 5.0 V	15	40	70	kΩ		
				10		80	kΩ		
Supply current*1	I _{DD1}	4.19 MHz Crystal oscillation C1 = C2 = 22 pF	V _{DD} = 4.5 to 5.0 V*2			3	9	mA	
			V _{DD} = 3 V ±10 %*3			0.55	1.5	mA	
	I _{DD2}		HALT mode	V _{DD} = 4.5 to 5.0 V			600	1800	μA
				V _{DD} = 3 V ±10 %			200	600	μA
	I _{DD3}		STOP mode, V _{DD} = 3 V ±10 %				0.1	10	μA

- * 1. Excluding current flowing in the internal pull-up resistors and comparator circuit.
2. When the processor clock control register (PCC) is set to 0011 for operation in the high-speed mode.
3. When the PCC register is set to 0000 for operation in the low-speed mode.

CAPACITANCE ($T_a = 25\text{ }^{\circ}\text{C}$, $V_{DD} = 0\text{ V}$)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	f = 1 MHz Unmeasured pins returned to 0 V			15	pF
Output capacitance	C_{OUT}				15	pF
Input/output capacitance	C_{IO}				15	pF

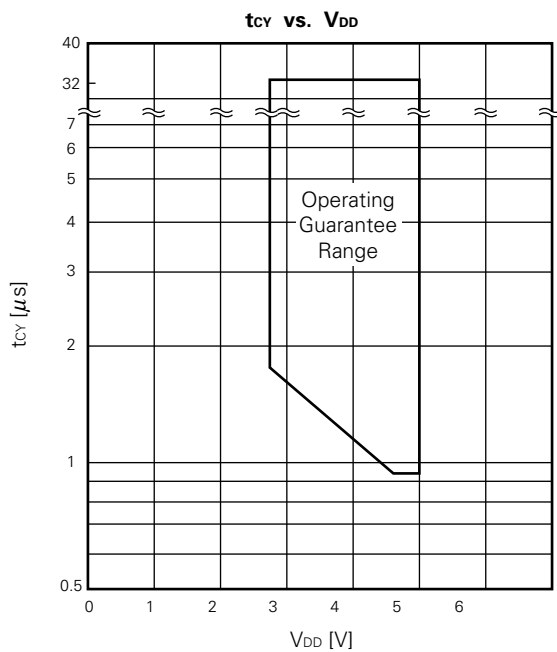
COMPARATOR CHARACTERISTICS ($T_a = -40\text{ to }+50\text{ }^{\circ}\text{C}$, $V_{DD} = 4.5\text{ to }5.0\text{ V}$)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Compare accuracy	V_{ACOMP}				± 100	mV
Threshold voltage	V_{TH}		0		V_{DD}	V
PTH input voltage	V_{IPTH}		0		V_{DD}	V
Comparator circuit current consumption		PTHM7 set to "1"		1		mA

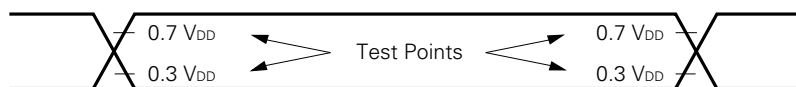
AC CHARACTERISTICS (Ta = -40 to +50 °C, VDD = 2.7 to 5.0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
CPU clock cycle time* (Minimum instruction execution time = 1 machine cycle)	tcy	VDD = 4.5 to 5.0 V		0.95		32	μs
				1.91		32	μs
TI0, TI1 input frequency	fTI	VDD = 4.5 to 5.0 V		0		1	MHz
				0		275	kHz
TI0, TI1 input high/ low-level width	tTIH,	VDD = 4.5 to 5.0 V		0.48			μs
	tTIL			1.8			μs
SCK cycle time	tKCY	VDD = 4.5 to 5.0 V	Input	0.8			μs
			Output	0.95			μs
			Input	3.2			μs
			Output	3.8			μs
SCK high/low-level width	tKH,	VDD = 4.5 to 5.0 V	Input	0.4			μs
			Output	tKCY/2 - 50			ns
	tKL		Input	1.6			μs
			Output	tKCY/2 - 150			ns
SI setup time (to SCK↑)	tSIK			100			ns
SI hold time (from SCK↑)	tKSI			400			ns
SO output delay time from SCK↓	tKSO	VDD = 4.5 to 5.0 V				300	ns
						1000	ns
INT0 to INT4 High/low-level width	tINTH, tINTL			5			μs
RESET low-level width	tRSL			5			μs

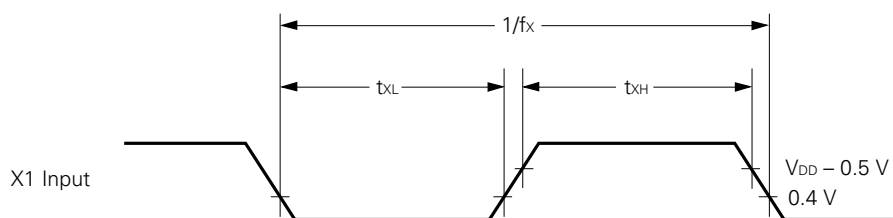
- * The CPU clock ϕ cycle time is determined by the oscillation frequency of the connected resonator and the setting of the processor clock control register (PCC). The graph on the right shows the characteristic for cycle time t_{CY} supply current V_{DD} during system clock operation.



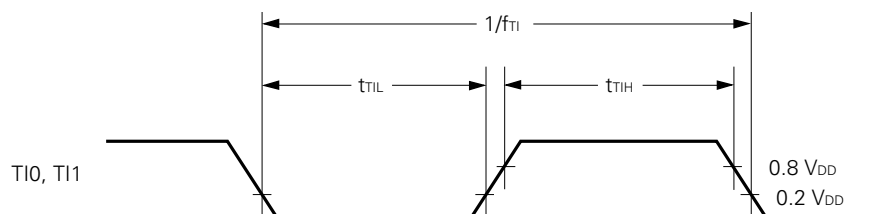
AC Timing Test Point (Except ports 0, 1, T10, T11, X1, X2, $\overline{\text{RESET}}$)



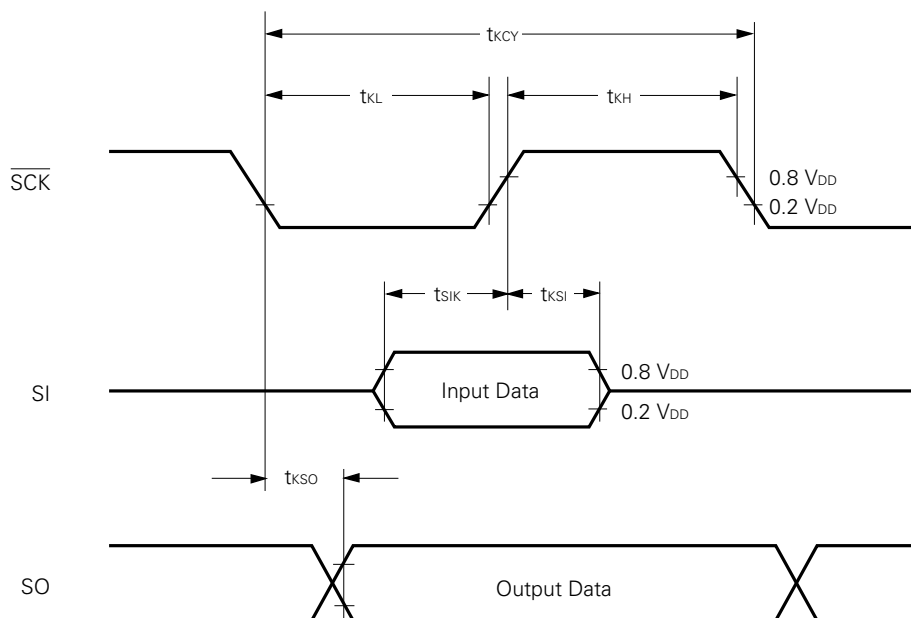
Clock Timing



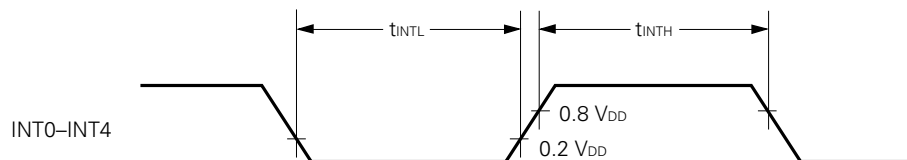
T10, T11 Input Timing



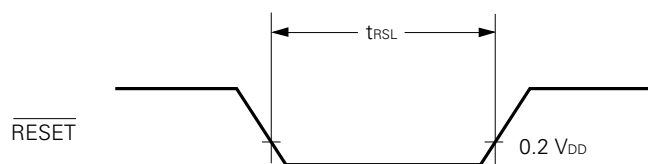
Serial Transfer Timing



Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



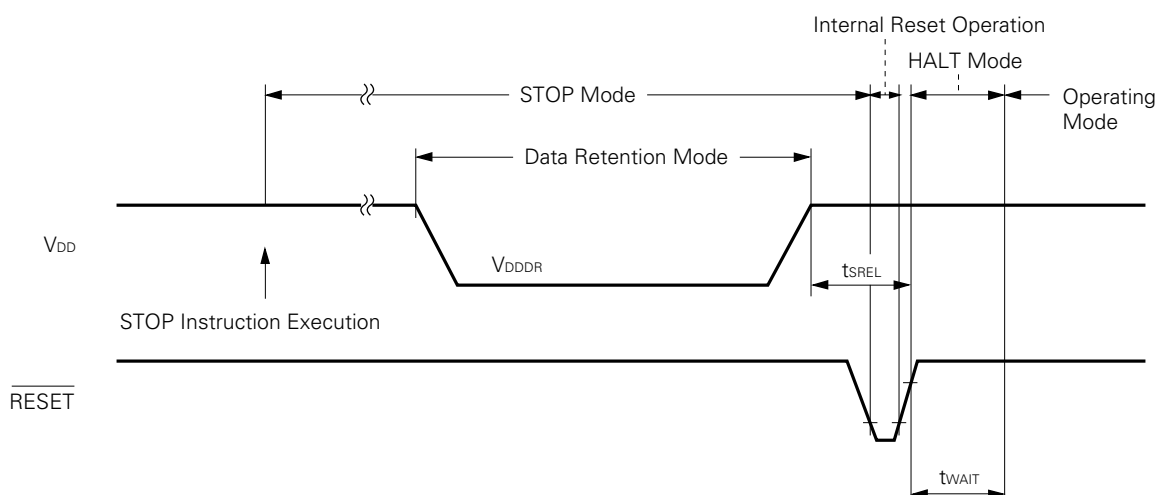
DATA MEMORY STOP MODE LOW SUPPLY VOLTAGE DATA RETENTION CHARACTERISTICS (Ta = -40 to +50 °C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data retention supply voltage	V _{DDDR}		2.0		5.0	V
Data retention supply current*1	I _{DDDR}	V _{DDDR} = 2.0 V		0.1	10	μA
Release signal set time	t _{SREL}		0			μs
Oscillation stabilization time*2	t _{WAIT}	Release by $\overline{\text{RESET}}$		2 ¹⁷ /f _{xx}		ms
		Release by interrupt request		*3		ms

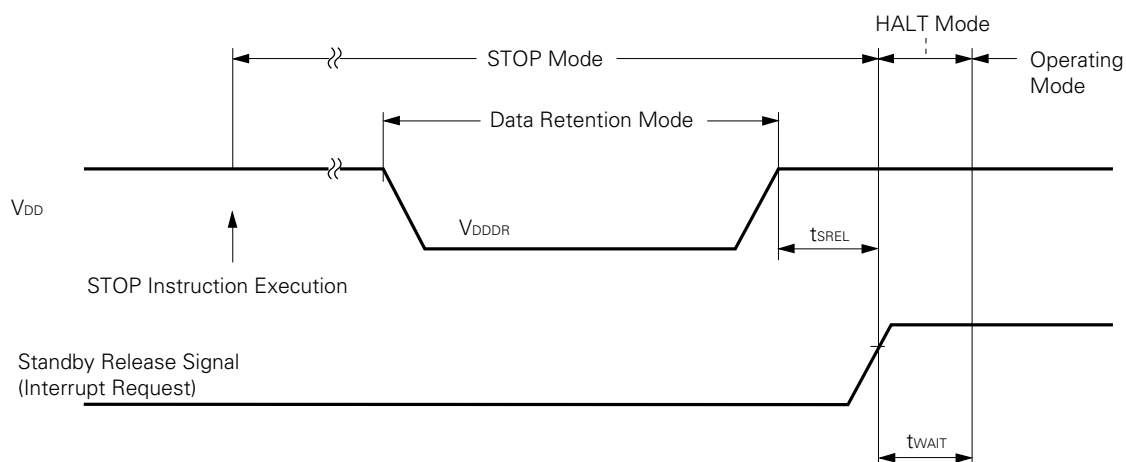
- * 1. Excluding current flowing in the internal pull-up resistors and comparator circuit.
 2. The oscillation stabilization wait time is the time during which CPU operation is stopped to prevent unstable operation when oscillation is started.
 3. Depends on the basic interval timer mode register (BTM) setting (see table below).

BTM3	BTM2	BTM1	BTM0	WAIT TIME (Figures in parentheses are for operation at f _{xx} = 4.19 MHz)
—	0	0	0	2 ²⁰ /f _{xx} (approx. 250 ms)
—	0	1	1	2 ¹⁷ /f _{xx} (approx. 31.3 ms)
—	1	0	1	2 ¹⁵ /f _{xx} (approx. 7.82 ms)
—	1	1	1	2 ¹³ /f _{xx} (approx. 1.95 ms)

Data Retention Timing (STOP mode release by $\overline{\text{RESET}}$)



Data Retention Timing (Standby release signal: STOP mode release by interrupt signal)



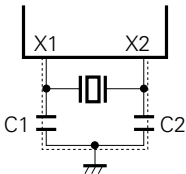
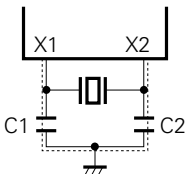
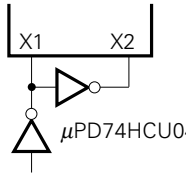
12.2 WHEN $T_a = -40$ to $+60$ °C, $V_{DD} = 2.8$ to 5.0 V

OPERATING VOLTAGE ($T_a = -40$ to $+60$ °C)

PARAMETER	TEST CONDITIONS	MIN.	MAX.	UNIT
CPU*1		*2	5.0	V
Programmable threshold port (comparator input)		4.5	5.0	V
Other hardware*1		2.8	5.0	V

- * 1. Except system clock oscillation circuit, programmable threshold port.
 2. The operable supply voltage range depends on the cycle time. See "AC CHARACTERISTICS".

OSCILLATION CIRCUIT CHARACTERISTICS ($T_a = -40$ to $+60$ °C, $V_{DD} = 2.8$ to 5.0 V)

RESONATOR	RECOMMENDED CONSTANT	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Ceramic resonator		Oscillator frequency (f_{xx})*1	$V_{DD} =$ Oscillation voltage range	2.0		5.0*3	MHz
		Oscillation stabilization time*2	After V_{DD} reaches MIN. of oscillation voltage range			4	ms
Crystal resonator		Oscillator frequency (f_{xx})*1		2.0	4.19	5.0*3	MHz
		Oscillation stabilization time*2	$V_{DD} = 4.5$ to 5.0 V			10	ms
						30	ms
External clock		X1 input frequency (f_x)*1		2.0		5.0*3	MHz
		X1 input high-/low-level width (t_{XH} , t_{XL})		100		250	ns

- * 1. Oscillator frequency and X1 input frequency indicate oscillation circuit characteristics only. See AC CHARACTERISTICS for instruction execution time.
 2. The oscillation stabilization time is the time required for oscillation to stabilize after V_{DD} reaches MIN. of oscillation voltage range, or the STOP mode is released.
 3. When the oscillator frequency is $4.19 \text{ MHz} < f_{xx} \leq 5.0 \text{ MHz}$, PCC = 0011 should not be selected as the instruction execution time. If PCC = 0011 is selected, one machine cycle is less than $0.95 \mu\text{s}$ and the rated MIN. value of $0.95 \mu\text{s}$ is not observed.

Note When the clock oscillator is used, the following should be noted concerning wiring in the area in the figure ★ enclosed by a dotted line to prevent the influence of wiring capacitance, etc.

- The wiring should be kept as short as possible.
- No other signal lines should be crossed.
- Keep away from lines carrying a high fluctuating current.
- The oscillator capacitor grounding point should always be at the same potential as V_{SS} . Do not connect to a ground pattern carrying a high current.
- A signal should be not taken from the oscillator.

RECOMMENDED OSCILLATION CIRCUIT CONSTANT
RECOMMENDED CERAMIC RESONATOR (Ta = -40 to +60 °C)

MANUFACTURER	PRODUCT NAME	EXTERNAL CAPACITANCE [pF]		OSCILLATION VOLTAGE RANGE [V]	
		C1	C2	MIN.	MAX.
Murata Mfg.	CSA 2.00MG	30	30	2.7	5.0
	CSA 4.19MG	30	30	3.0	5.0
	CSA 4.19MGU	30	30	2.7	5.0
	CST 4.19T	—	—	3.0	5.0
Kyocera	KBR-2.0MS	100	100	3.0	5.0
	KBR-4.0MS	33	33	3.0	5.0
	KBR-4.19MS	33	33	3.0	5.0
	KBR-4.9152M	33	33	3.0	5.0

RECOMMENDED CRYSTAL RESONATOR (Ta = -20 to +60 °C)

MANUFACTURER	PRODUCT NAME	EXTERNAL CAPACITANCE [pF]		OSCILLATION VOLTAGE RANGE [V]	
		C1	C2	MIN.	MAX.
Kinseki	HC-49/U	22	22	2.7	5.0

DC CHARACTERISTICS (Ta = -40 to +60 °C, VDD = 2.8 to 5.0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT		
Input voltage high	V _{IH1}	Other than below		0.7 V _{DD}		V _{DD}	V		
	V _{IH2}	Ports 0,1,TI0, 1, $\overline{\text{RESET}}$		0.8 V _{DD}		V _{DD}	V		
	V _{IH3}	Ports 12 to 14	Internal pull-up resistor	0.7 V _{DD}		V _{DD}	V		
			Open-drain	0.7 V _{DD}		10	V		
	V _{IH4}	X1, X2		V _{DD} – 0.5		V _{DD}	V		
Input voltage low	V _{IL1}	Other than below		0		0.3 V _{DD}	V		
	V _{IL2}	Ports 0,1,TI0, 1, $\overline{\text{RESET}}$		0		0.2 V _{DD}	V		
	V _{IL3}	X1, X2		0		0.4	V		
Output voltage high	V _{OH}	V _{DD} = 4.5 to 5.0 V, I _{OH} = –1 mA		V _{DD} – 1.0			V		
		I _{OH} = –100 μA		V _{DD} – 0.5			V		
Output voltage low	V _{OL}	V _{DD} = 4.5 to 5.0 V	Ports 0, 2 to 9, I _{OL} = 15 mA		0.35	2.0	V		
			Ports 12 to 14, I _{OL} = 10 mA		0.35	2.0	V		
		V _{DD} = 4.5 to 5.0 V, I _{OL} = 1.6 mA				0.4	V		
		I _{OL} = 400 μA				0.5	V		
Input leakage current high	I _{LIH1}	V _{IN} = V _{DD}	Other than below			3	μA		
	I _{LIH2}		X1, X2			20	μA		
	I _{LIH3}	V _{IV} = 10 V	Ports 12 to 14 (open-drain)			20	μA		
Input leakage current low	I _{LIL1}	V _{IN} = 0 V	Except X1, X2			–3	μA		
	I _{LIL2}		X1, X2			–20	μA		
Output leakage current high	I _{LOH1}	V _{OUT} = V _{DD}	Other than below			3	μA		
	I _{LOH2}	V _{OUT} = 10 V	Ports 12 to 14 (open-drain)			20	μA		
Output leakage current low	I _{LOL}	V _{OUT} = 0 V				–3	μA		
Internal pull-up resistor (mask option)	R _L	Ports 12 to 14	V _{DD} = 4.5 to 5.0 V	15	40	70	kΩ		
				10		80	kΩ		
Supply current*1	I _{DD1}	4.19 MHz Crystal oscillation C1 = C2 = 22 pF	V _{DD} = 4.5 to 5.0 V*2			3	9	mA	
			V _{DD} = 2.8 to 3.3 V*3			0.55	1.5	mA	
	I _{DD2}		HALT mode	V _{DD} = 4.5 to 5.0 V			600	1800	μA
				V _{DD} = 2.8 to 3.3 V			200	600	μA
	I _{DD3}	STOP mode, V _{DD} = 2.8 to 3.3 V				0.1	10	μA	

- * 1. Excluding current flowing in the internal pull-up resistors and comparator circuit.
2. When the processor clock control register (PCC) is set to 0011 for operation in the high-speed mode.
3. When the PCC register is set to 0000 for operation in the low-speed mode.

CAPACITANCE ($T_a = 25\text{ }^{\circ}\text{C}$, $V_{DD} = 0\text{ V}$)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	$f = 1\text{ MHz}$ Unmeasured pins returned to 0 V			15	pF
Output capacitance	C_{OUT}				15	pF
Input/output capacitance	C_{IO}				15	pF

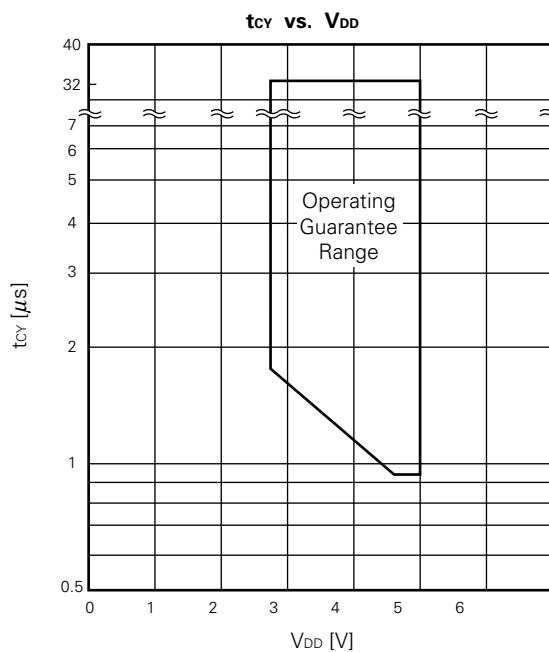
COMPARATOR CHARACTERISTICS ($T_a = -40\text{ to }+60\text{ }^{\circ}\text{C}$, $V_{DD} = 4.5\text{ to }5.0\text{ V}$)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Compare accuracy	V_{ACOMP}				± 100	mV
Threshold voltage	V_{TH}		0		V_{DD}	V
PTH input voltage	V_{IPTH}		0		V_{DD}	V
Comparator circuit current consumption		PTHM7 set to "1"		1		mA

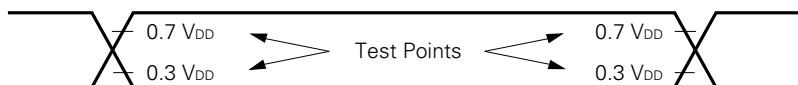
AC CHARACTERISTICS (Ta = -40 to +60 °C, VDD = 2.8 to 5.0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
CPU clock cycle time* (Minimum instruction execution time = 1 machine cycle)	tcy	VDD = 4.5 to 5.0 V		0.95		32	μs
				1.91		32	μs
TI0, TI1 input frequency	fTI	VDD = 4.5 to 5.0 V		0		1	MHz
				0		275	kHz
TI0, TI1 input high/ low-level width	tTIH, tTIL	VDD = 4.5 to 5.0 V		0.48			μs
				1.8			μs
SCK cycle time	tkcy	VDD = 4.5 to 5.0 V	Input	0.8			μs
			Output	0.95			μs
			Input	3.2			μs
			Output	3.8			μs
SCK high/low-level width	tkH, tkL	VDD = 4.5 to 5.0 V	Input	0.4			μs
			Output	tkcy/2 - 50			ns
			Input	1.6			μs
			Output	tkcy/2 - 150			ns
SI setup time (to SCK↑)	tsik			100			ns
SI hold time (from SCK↑)	tkSI			400			ns
SO output delay time from SCK↓	tkSO	VDD = 4.5 to 5.0 V				300	ns
						1000	ns
INT0 to INT4 High/low-level width	tINTH, tINTL			5			μs
RESET low-level width	trSL			5			μs

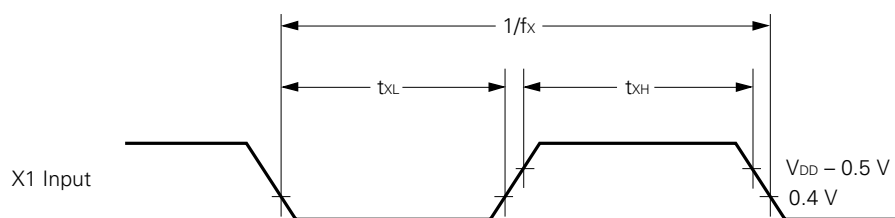
- * The CPU clock ϕ cycle time is determined by the oscillation frequency of the connected resonator and the setting of the processor clock control register (PCC). The graph on the right shows the characteristic for cycle time t_{CY} supply current V_{DD} during system clock operation.



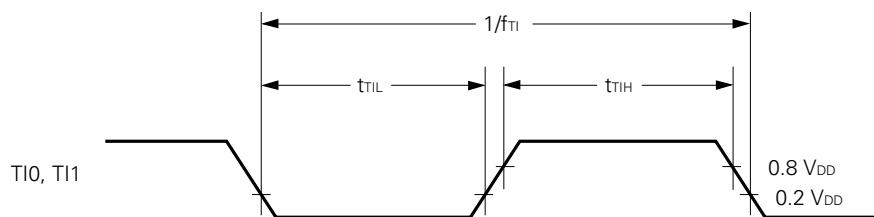
AC Timing Test Point (Except ports 0, 1, T10, T11, X1, X2, $\overline{\text{RESET}}$)



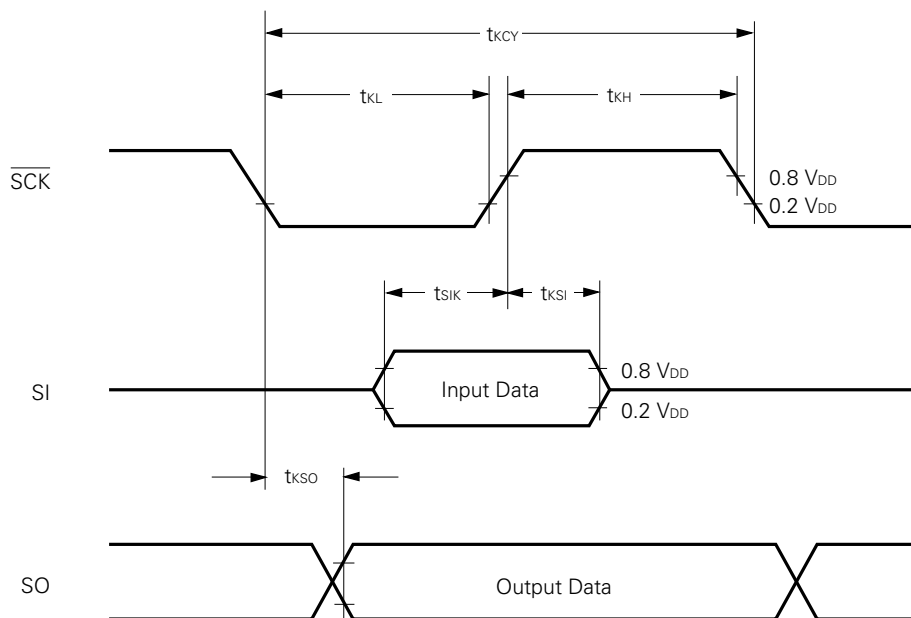
Clock Timing



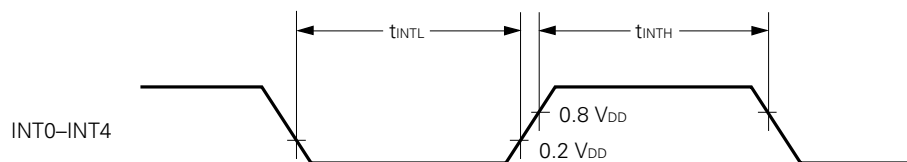
T10, T11 Input Timing



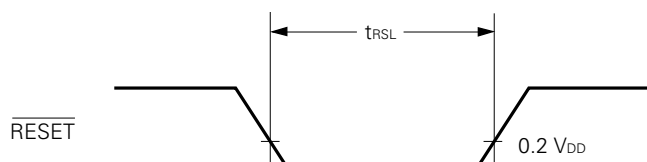
Serial Transfer Timing



Interrupt Input Timing



RESET Input Timing



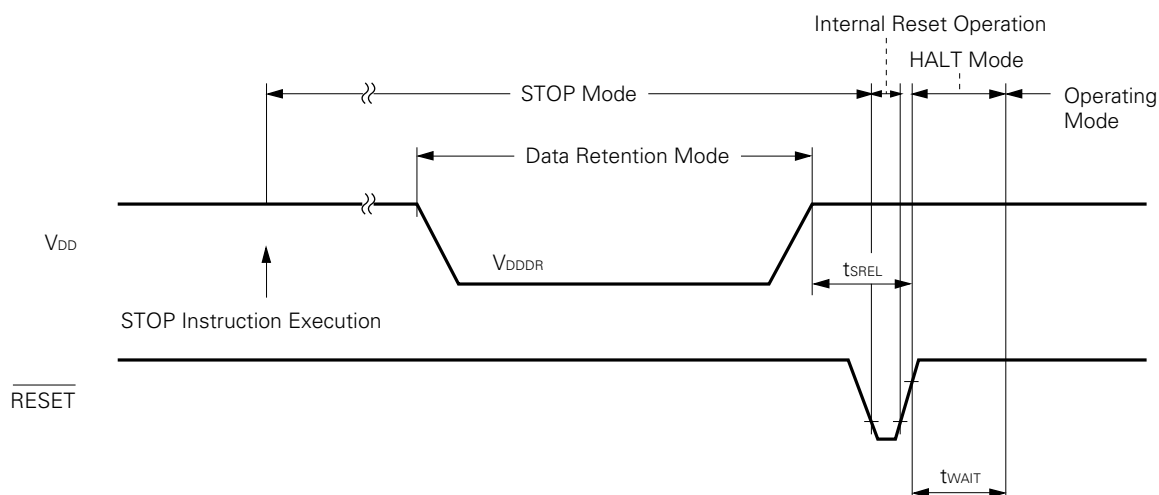
DATA MEMORY STOP MODE LOW SUPPLY VOLTAGE DATA RETENTION CHARACTERISTICS (Ta = -40 to +60 °C)

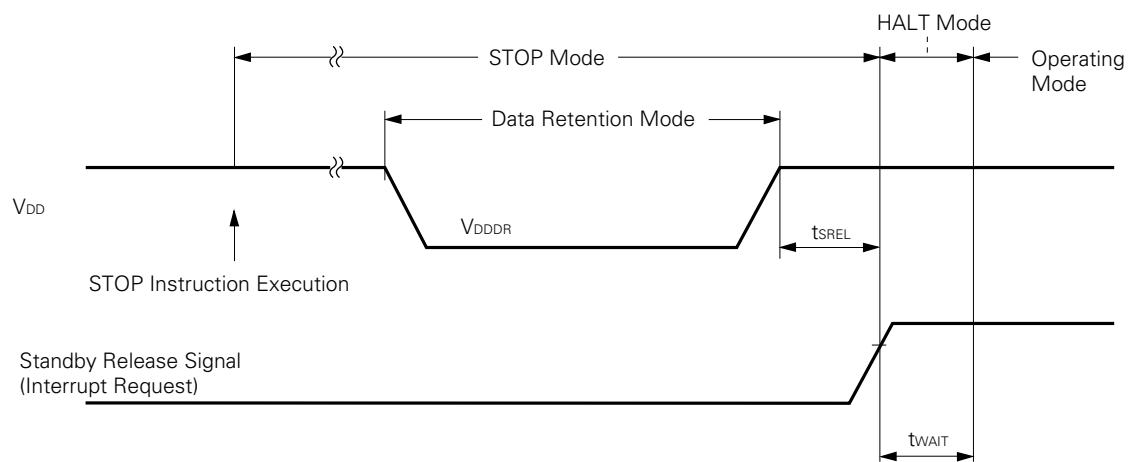
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data retention supply voltage	V _{DDDR}		2.0		5.0	V
Data retention supply current*1	I _{DDDR}	V _{DDDR} = 2.0 V		0.1	10	μA
Release signal set time	t _{SREL}		0			μs
Oscillation stabilization time*2	t _{WAIT}	Release by $\overline{\text{RESET}}$		2 ¹⁷ /f _{xx}		ms
		Release by interrupt request		*3		ms

- * 1. Excluding current flowing in the internal pull-up resistors and comparator circuit.
 2. The oscillation stabilization wait time is the time during which CPU operation is stopped to prevent unstable operation when oscillation is started.
 3. Depends on the basic interval timer mode register (BTM) setting (see table below).

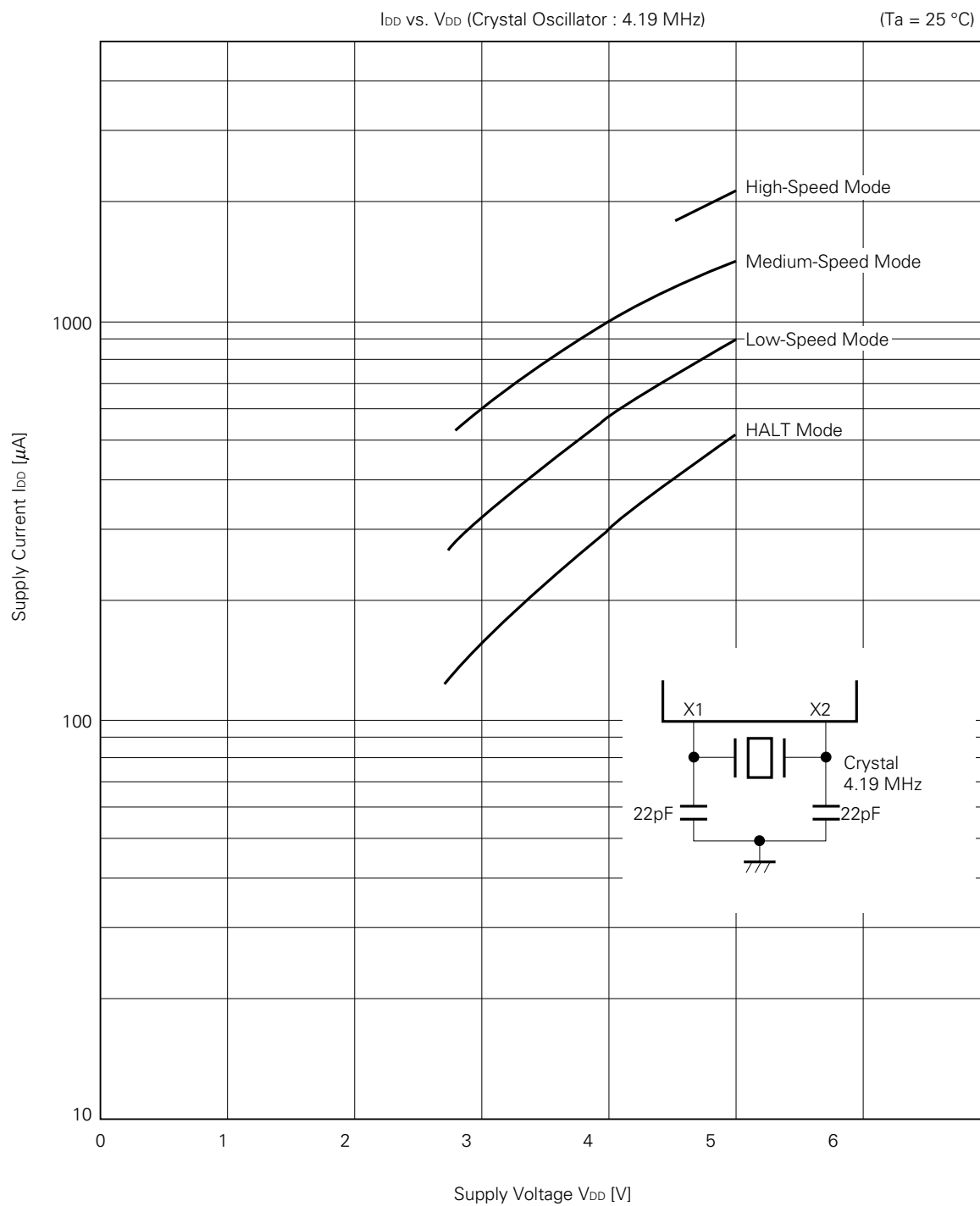
BTM3	BTM2	BTM1	BTM0	WAIT TIME (Figures in parentheses are for operation at f _{xx} = 4.19 MHz)
—	0	0	0	2 ²⁰ /f _{xx} (approx. 250 ms)
—	0	1	1	2 ¹⁷ /f _{xx} (approx. 31.3 ms)
—	1	0	1	2 ¹⁵ /f _{xx} (approx. 7.82 ms)
—	1	1	1	2 ¹³ /f _{xx} (approx. 1.95 ms)

Data Retention Timing (STOP mode release by $\overline{\text{RESET}}$)

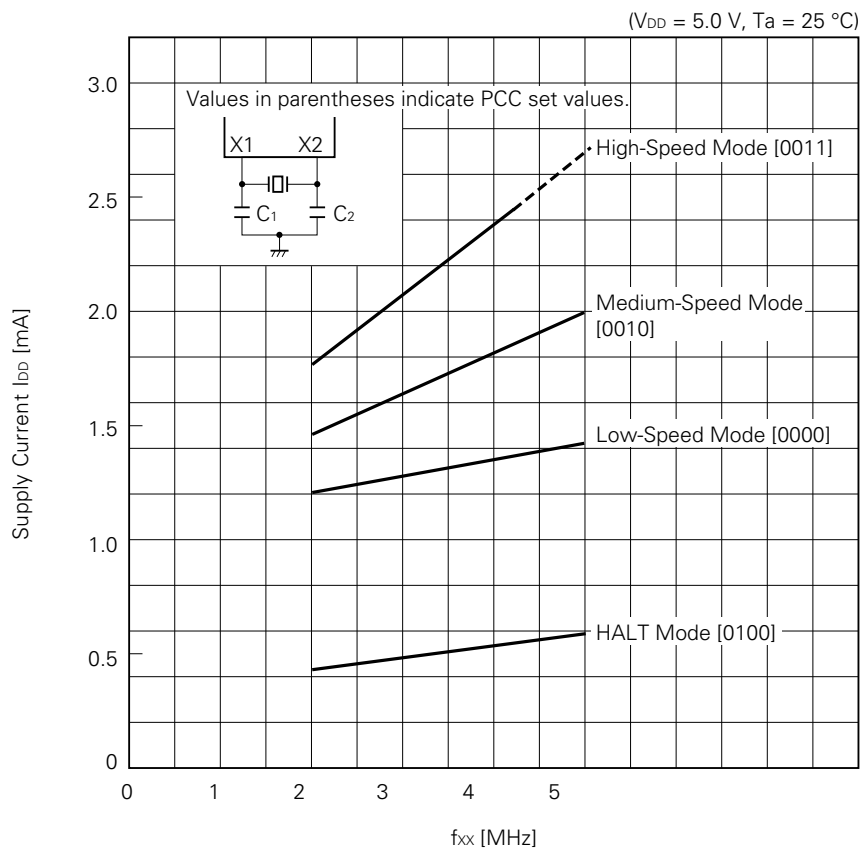


Data Retention Timing (Standby release signal: STOP mode release by interrupt signal)

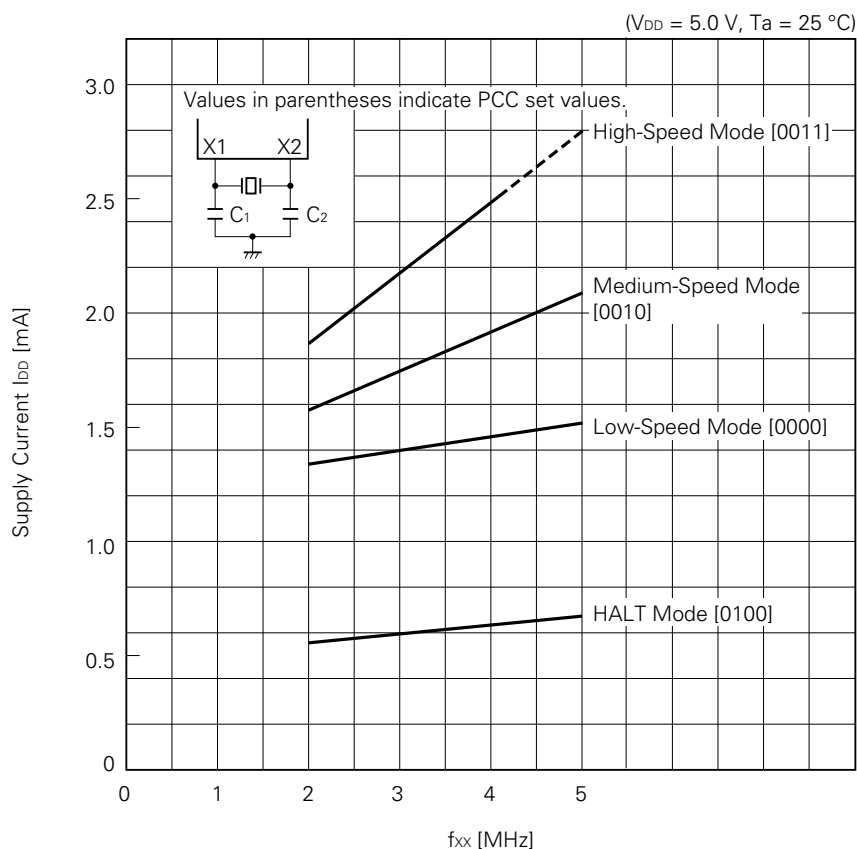
13. CHARACTERISTIC CURVES (REFERENCE)



I_{DD} vs. f_{XX} Characteristic Examples (Crystal Oscillation)

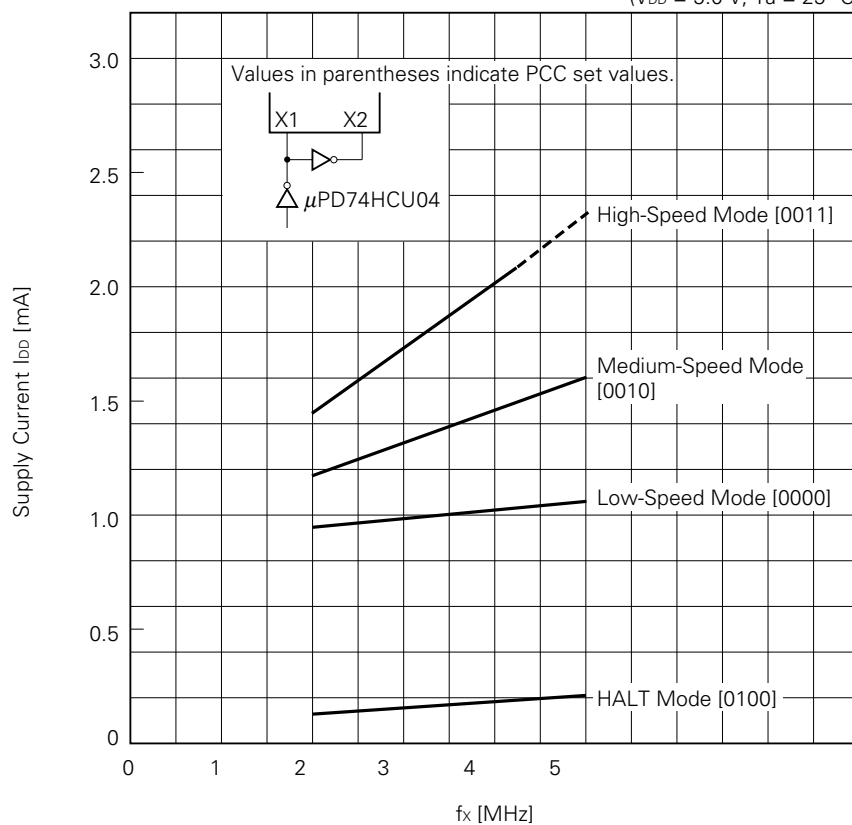


I_{DD} vs. f_{XX} Characteristic Examples (Ceramic Oscillation)



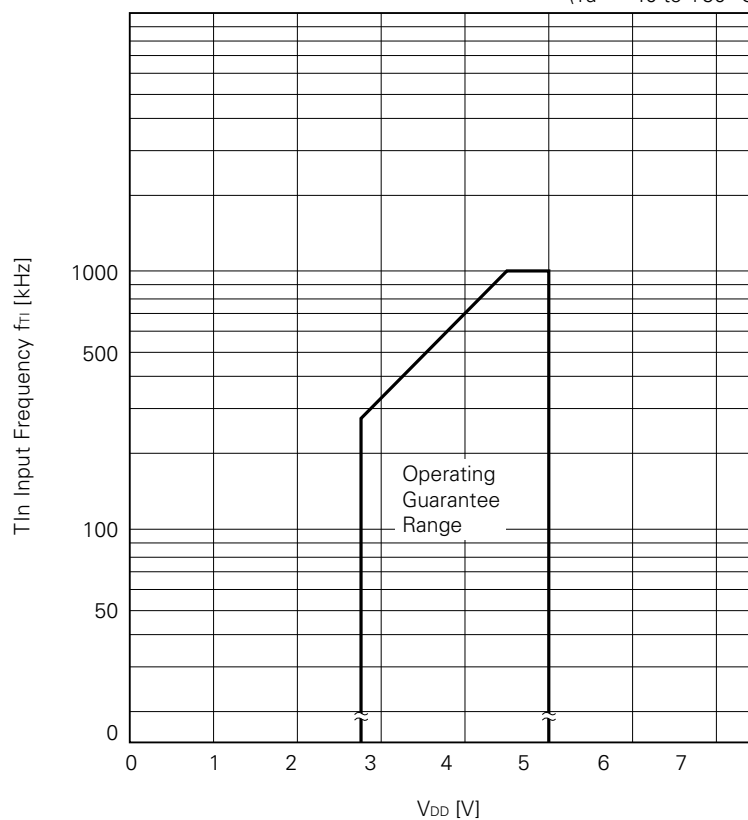
I_{DD} vs. f_x Characteristic Examples (External Clock)

($V_{DD} = 5.0\text{ V}$, $T_a = 25\text{ }^\circ\text{C}$)



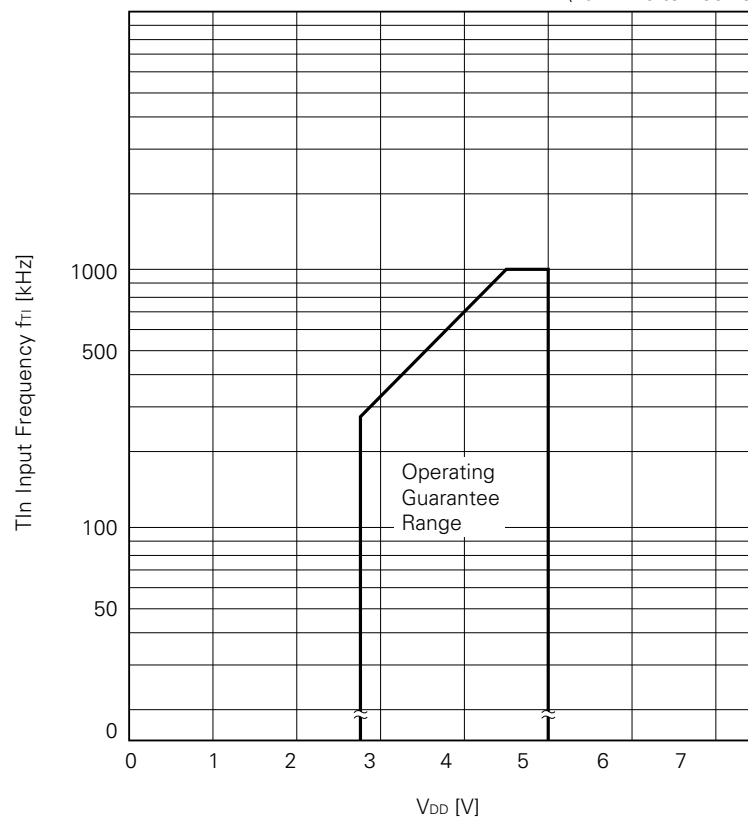
f_{Ti} vs. V_{DD} Characteristic

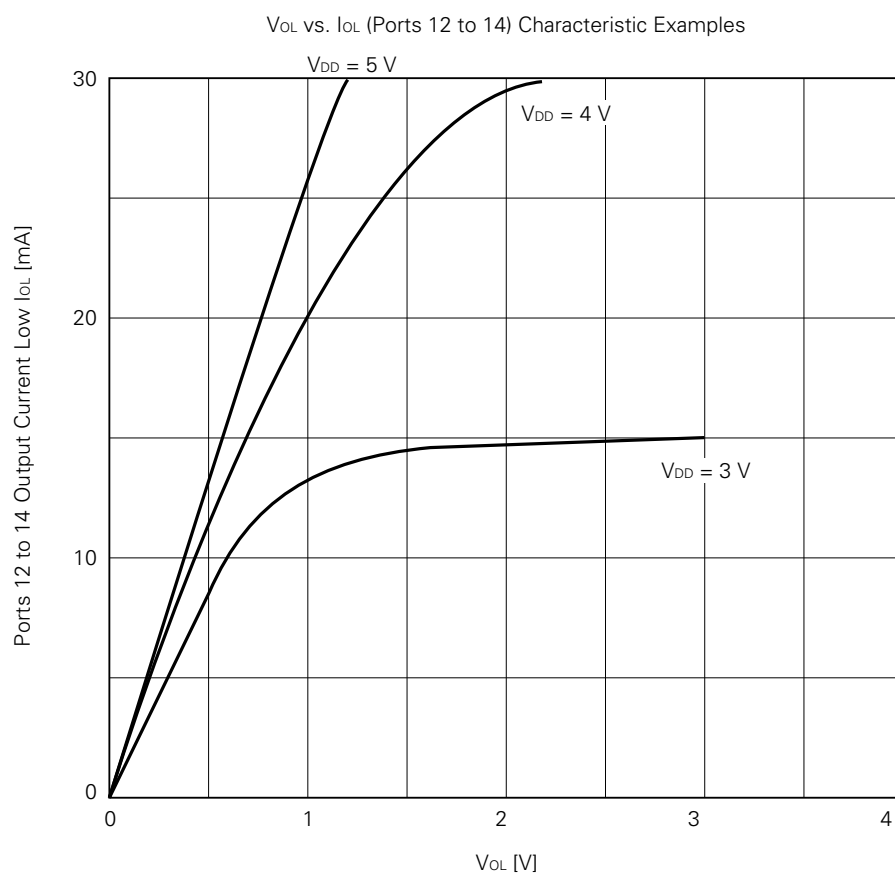
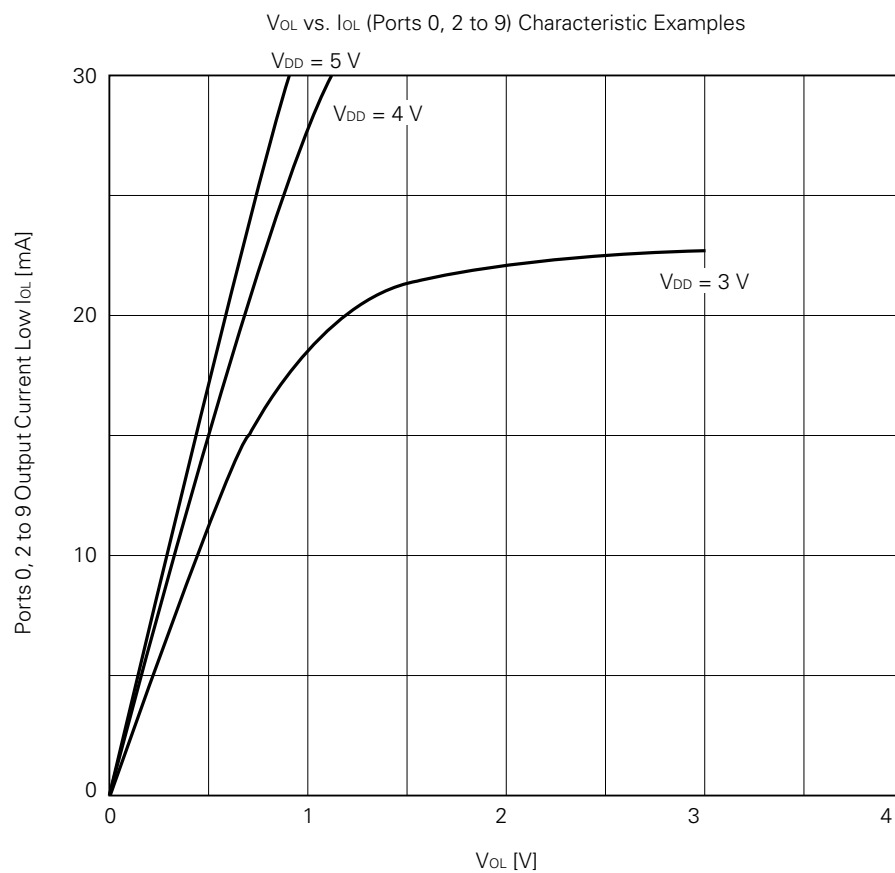
($T_a = -40$ to $+50$ °C)

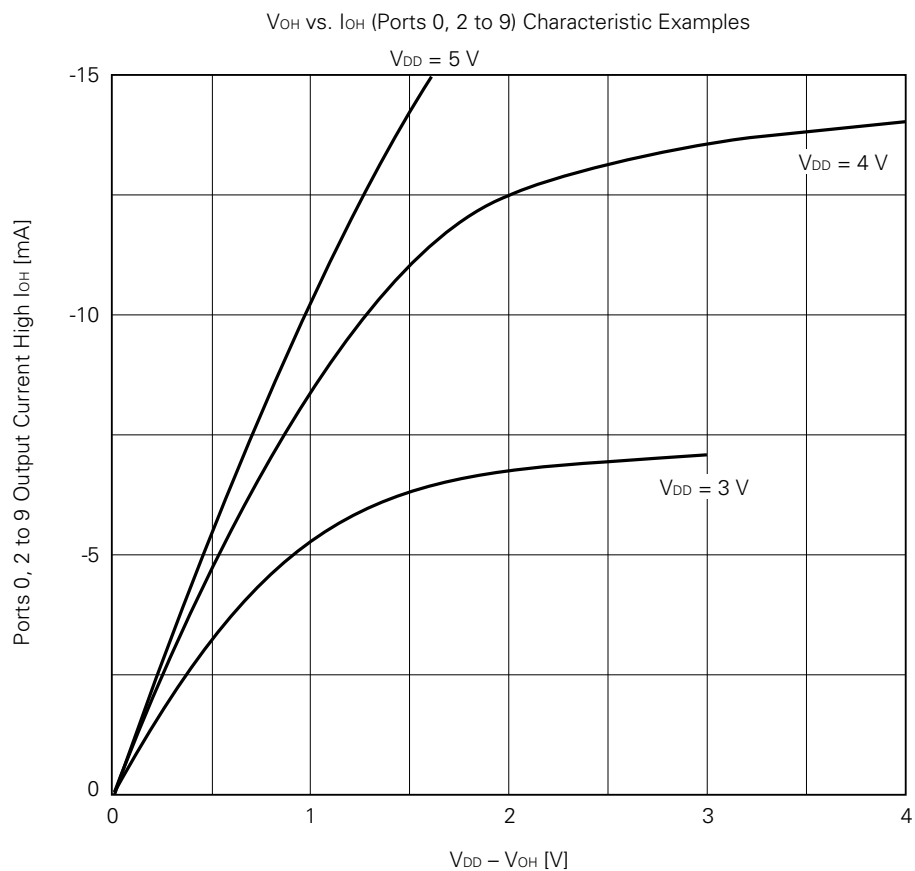


f_{Ti} vs. V_{DD} Characteristic

($T_a = -40$ to $+60$ °C)



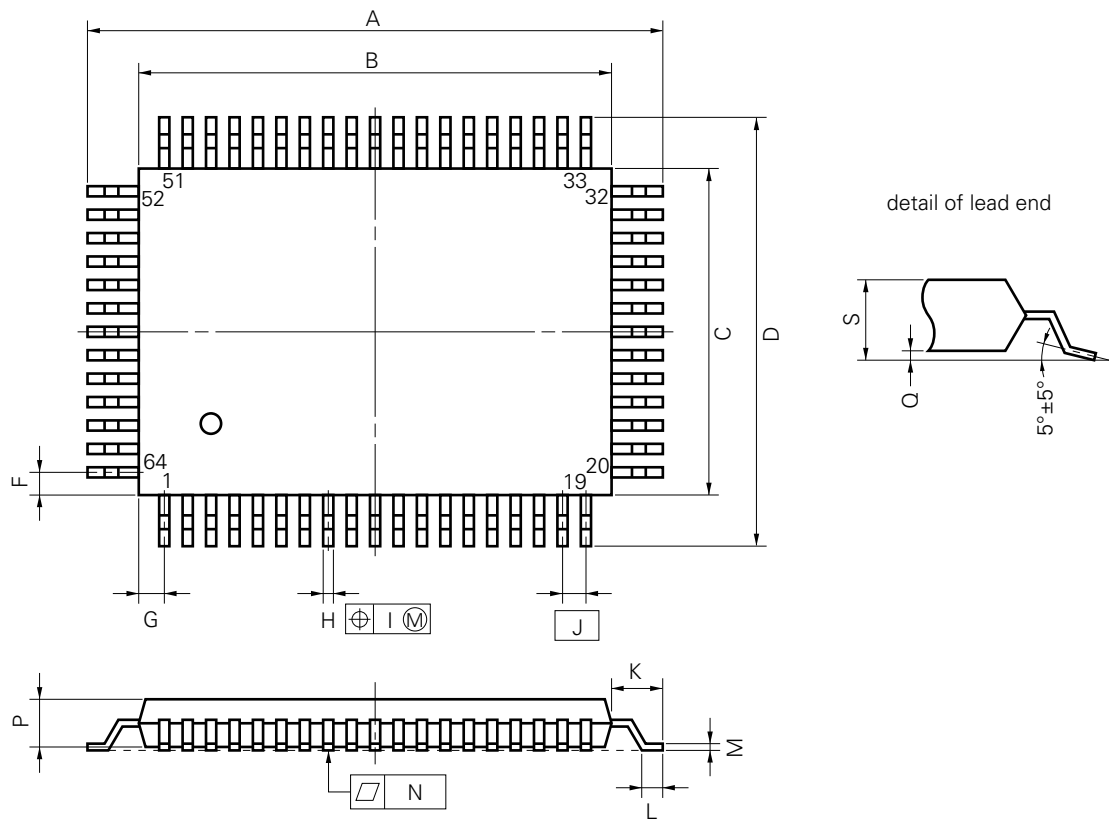




Remarks Characteristic curves not marked "Guarantee Range" indicate reference values.

14. PACKAGE INFORMATION

64-Pin Plastic QFP (14 × 20)



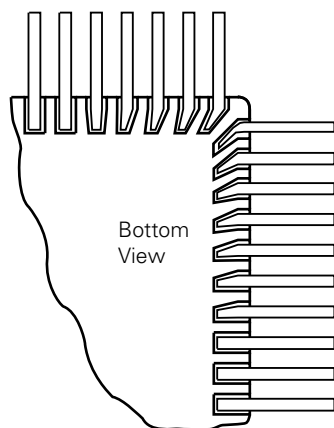
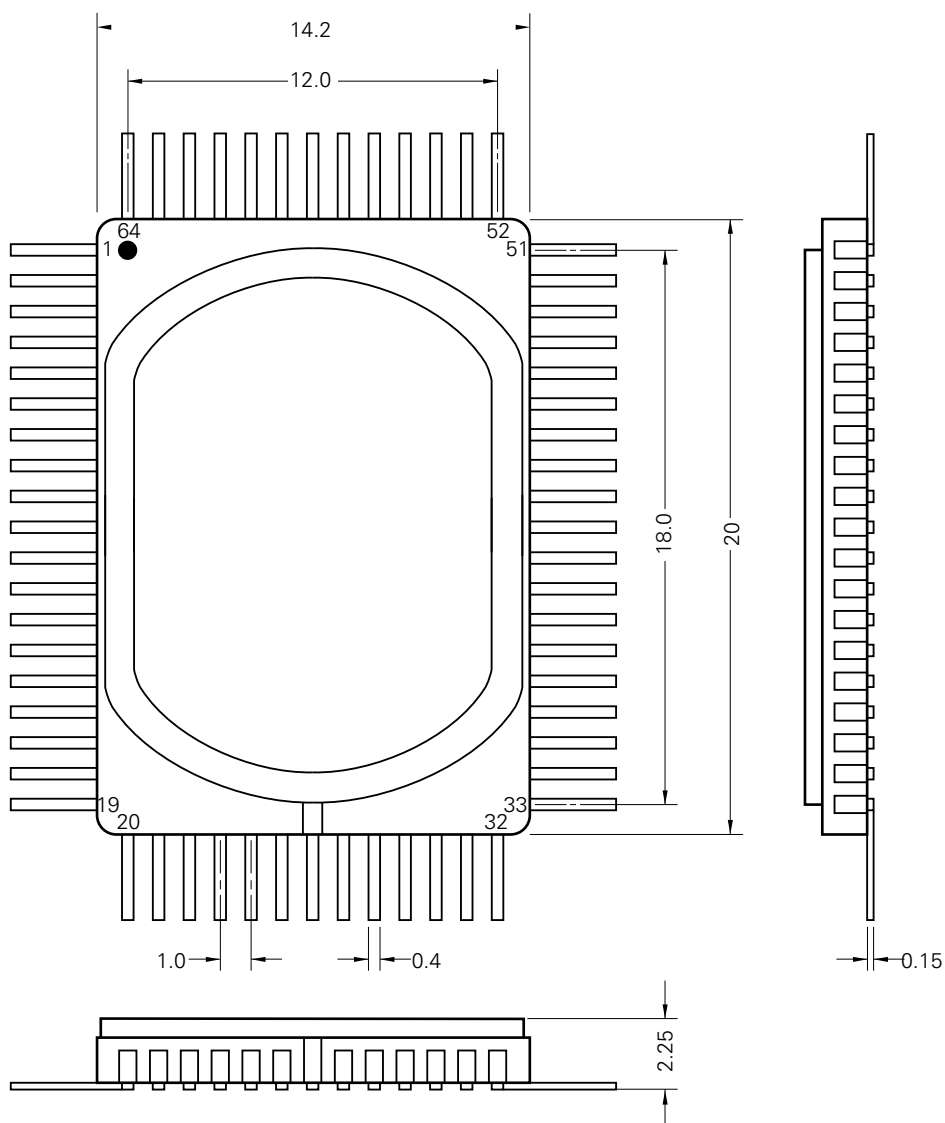
NOTE

Each lead centerline is located within 0.20 mm (0.008 inch) of its true position (T.P.) at maximum material condition.

P64GF-100-3B8,3BE,3BR-1

ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	0.795 ^{+0.009} _{-0.008}
C	14.0±0.2	0.551 ^{+0.009} _{-0.008}
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	1.0	0.039
H	0.40±0.10	0.016 ^{+0.004} _{-0.005}
I	0.20	0.008
J	1.0 (T.P.)	0.039 (T.P.)
K	1.8±0.2	0.071 ^{+0.008} _{-0.009}
L	0.8±0.2	0.031 ^{+0.009} _{-0.008}
M	0.15 ^{+0.10} _{-0.05}	0.006 ^{+0.004} _{-0.003}
N	0.12	0.005
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

64-Pin Ceramic QFP for ES (Reference Diagram)



- Caution**
1. Note that the metal cap is connected to pin 26, and is at the V_{SS} (GND) level.
 2. Note that the leads on the underside are formed at an angle.
 3. Cutting of the lead tips is not process-controlled, and therefore there is no standard lead length.

15. RECOMMENDED SOLDERING CONDITIONS

The μPD75116F should be soldered and mounted under the conditions recommended in the table below.

For details of recommended conditions, refer to **the information document "Semiconductor Device Mount Technology Manual" (IEI-1207)**.

For soldering methods and conditions other than those recommended below, contact our salesman.

Table 15-1 Surface Mount Type Soldering Conditions

μPD75108FGF-xxx-3BE : 64-Pin Plastic QFP (14 × 20 mm)

μPD75112FGF-xxx-3BE : 64-Pin Plastic QFP (14 × 20 mm)

μPD75116FGF-xxx-3BE : 64-Pin Plastic QFP (14 × 20 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature : 230 °C, Duration : 30 sec. max. (at 210 °C or above), Number of times : once	IR30-00-1
VPS	Package peak temperature : 215 °C, Duration : 40 sec. max. (at 200 °C or above), Number of times : once	VP15-00-1
Wave soldering	Solder bath temperature : 260 °C max., Duration : 10 sec. max., Number of times : once, Preheating temperature : 120 °C max. (package surface temperature)	WS60-00-1
Pin part heating	Pin part temperature : 300 °C max., Duration : 3 sec. max. (per device side)	Pin part heating

Note Use of more than one soldering method should be avoided (except in the case of pin part heating).

Notice

A version of this product with improved recommended soldering conditions is available. For details (improvements such as infrared reflow peak temperature extension (235 °C), number of times: twice, relaxation of time limit, etc.), contact NEC sales personnel.

★ APPENDIX A. FUNCTIONAL DIFFERENCES AMONG μPD751xx SERIES PRODUCTS

Product Name		μPD75104/106/108/112/116		μPD75104A/108A		μPD75108F/112F/116F	
Item							
ROM (byte)		4K/6K/8K/12K/16K (Mask ROM)		4K/8K (Mask ROM)		8K/12K/16K (Mask ROM)	
RAM (× 4 bits)		320/320/512/512/512		320/512		512	
Instruction set		75X High-End					
I/O port	Total	58					
	CMOS input	10	10 (Pull-up resistor mask option : 4)			10	
	CMOS input/output	32 (LED direct drive capability)	32 (Pull-up resistor mask option : 24, LED direct drive capability)			32 (LED direct drive capability)	
	N-ch open-drain input/output	12 (LED direct drive capability)					
	Withstand voltage	+12 V				+10 V	
	Pull-up resistor	Can be incorporated by mask option					
	Analog input	4 (4-bit precision)					
Power-on reset circuit		On-chip (Mask option)				None	
Power-on flag							
Operating voltage		2.7 to 6.0 V				2.7 to 5.0 V (Ta = −40 to +50 °C) 2.8 to 5.0 V	
Operating temperature range		−40 to +85 °C				−40 to +60 °C	
Minimum instruction execution time		0.95 μs (operating at 4.5 to 6.0 V) 3.8 μs (operating at 2.7 V)				0.95 μs (operating at 4.5 to 5.0 V) 1.91 μs (operating at 2.7V)	
Package *2		• 64-pin plastic shrink DIP • 64-pin plastic QFP(GF-3BE) • 64-pin plastic QFP (G-1B) : μPD75104/106/108 only		• 64-pin plastic QFP(GC-AB8) • 64-pin plastic QFP (G-22) : μPD75108A only		• 64-pin plastic QFP(GF-3BE)	

- * 1. 75X High-End can also be used by means of the 16K-byte mode/24K-byte mode switching function.
2. The following five types of plastic QFP are available.
- G-1B 14 × 20 × 2.05 mm, 1.0 mm pitch
 - GC-AB8 ... 14 × 14 × 2.55 mm, 0.8 mm pitch
 - GF-3BE 14 × 20 × 2.7 mm, 1.0 mm pitch
 - G-22 14 × 14 × 1.5 mm, 0.8 mm pitch
 - GK-7ET ... 12 × 12 × 1.45 mm, 0.65 mm pitch
3. Under development.

μPD75116H/117H	μPD75P108B	μPD75P116	μPD75P117H
16K/24K (Mask ROM)	8K (One-time PROM)		24K (One-time PROM)
768	512		768
75X High-End/Extended High-End	75X High-End		75X Extended High-End*1
58			
10			
32 (LED direct drive capability : 8)	32 (LED direct drive capability)		32 (LED direct drive capability : 8)
12	12 (LED direct drive capability)		12
+6 V	+12 V		+6 V
Can be incorporated by mask option	None		
4 (4-bit precision)			
None	None		
1.8 to 5.0 V	2.7 to 6.0 V	5 V ±10 %	1.8 to 5.0 V
−40 to +60 °C	−40 to +85 °C		−40 to +60 °C
0.95 μs (operating at 2.7 V) 1.91 μs (operating at 1.8 V)	0.95 μs (operating at 4.5 to 6.0 V) 3.8 μs (operating at 2.7 V)	0.95 μs (operating at 4.75 to 5.5 V)	0.95 μs (operating at 2.7 V) 1.91 μs (operating at 1.8 V)
• 64-pin plastic QFP (GC-AB8) • 64-pin plastic QFP (GK-7ET)	• 64-pin plastic shrink DIP • 64-pin plastic QFP (GF-3BE) • 64-pin ceramic shrink DIP with window	• 64-pin plastic shrink DIP • 64-pin plastic QFP (GF-3BE)	• 64-pin plastic QFP (GC-AB8) • 64-pin plastic QFP (GK-7ET)*3

★ APPENDIX B. DEVELOPMENT TOOLS

The following development tools are available for system development using the μ PD75116F.

Hardware	IE-75000-R*1 IE-75001-R	75X series in-circuit emulator
	IE-75000-R-EM*2	Emulation board for the IE-75000-R or IE-75001-R
	EP-75108GF-R EV-9200G-64	Emulation probe for the μ PD75116FGF. A 64-pin conversion socket (EV-9200G-64) is also provided.
	PG-1500	PROM programmer
	PA-75P116GF	PROM programmer adapter for the μ PD75P116GF, connected to the PG-1500.
Software	IE Control Program	Host machines • PC-9800 series (MS-DOS™ Ver. 3.30 to Ver. 5.00A*3) • IBM PC/AT™ (PC-DOS™ Ver.3.1)
	PG-1500 Controller	
	RA75X Relocatable Assembler	

- * 1. Maintenance product
 2. Not incorporated in the IE-75001-R.
 3. A task swapping function is provided in Ver. 5.00/5.00A, but this function cannot be used with this software.

Remarks Please refer to the **75X Series Selection Guide (IF-151)** for third party development tools.

APPENDIX C. RELATED DOCUMENTS



Device Related Documents

Document Name		Document Number
User's Manual		IEM-1260
Instruction Application Table		Not Available
Application Note	(I) Introductory Volume	IEM-1139
	(II) Remote Control Reception Volume	IEM-1281
	(III) Barcode Reader Volume	IEM-1265
	(IV) MSK Transmission/Reception IC Control Volume	IEM-1278
75X Series Selection Guide		IF-1027

Development Tools Documents

Document Name			Document Number
Hardware	IE-75000-R/IE-75001-R User's Manual		EEU-1455
	IE-75000-R-EM User's Manual		EEU-1294
	EP-75108GF-R User's Manual		EEU-1318
	PG-1500 User's Manual		EEU-1335
Software	RA75X Assembler Package User's Manual	Operation Volume	EEU-1346
		Language Volume	EEU-1343
	PG-1500 Controller User's Manual		EEU-1291

Other Documents

Document Name	Document Number
Package Manual	IEI-1213
Surface Mount Technology Manual	IEI-1207
Quality grade on NEC Semiconductor Devices	IEI-1209
NEC Semiconductor Device Reliability & Quality Control	Not Available
Electrostatic Discharge (ESD) Test	Not Available
Semiconductor Devices Quality Guide Guarantee Guide	MEI-1202
Microcomputer Related Products Guide Other Manufacturers Volume	Not Available

Note The information in these related documents is subject to change without notice. For design purpose, etc., be sure to use the latest ones.

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