



May 2004

## LM4856 Boomer® Audio Power Amplifier Series

### Integrated Audio Amplifier System

#### General Description

The LM4856 is an audio power amplifier system capable of delivering 1.1W (typ) of continuous average power into a mono 8Ω bridged-tied load (BTL) with 1% THD+N and 60mW (typ) per channel of continuous average power into stereo 32Ω single-ended (SE) loads with 0.5% THD+N, using a 5V power supply.

The LM4856 features a 32 step digital volume control and eight distinct output modes. The digital volume control and output modes are programmed through a two-wire I<sup>2</sup>C compatible control interface, that allows flexibility in routing and mixing audio channels.

The LM4856 is designed for cellular phone, PDA, and other portable handheld applications. It delivers high quality output power from a surface-mount package and requires only eight external components.

The industry leading micro SMD package only utilizes 2mm x 2.3mm of PCB space, making the LM4856 the most space efficient audio sub system available today.

#### Key Specifications

■ THD+N at 1kHz, 1.1W into 8Ω BTL	1.0% (typ)
■ THD+N at 1kHz, 60mW into 32Ω SE	0.5% (typ)
■ Single Supply Operation	2.6 to 5.0V

#### Features

- 1.1W (typ) output power with 8Ω mono BTL load
- 60mW (typ) output power with stereo 32Ω SE loads
- I<sup>2</sup>C programmable 32 step digital volume control
- Eight distinct output modes
- micro-SMD and LLP surface mount packaging
- "Click and Pop" suppression circuitry
- Thermal shutdown protection
- Low shutdown current (0.1uA, typ)

#### Applications

- Mobile Phones
- PDAs

#### Typical Application

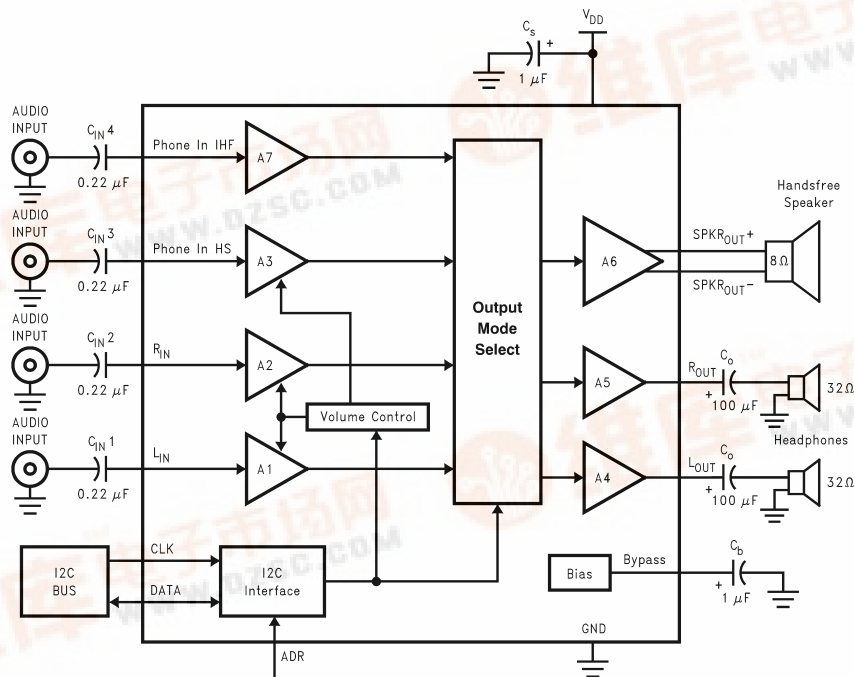
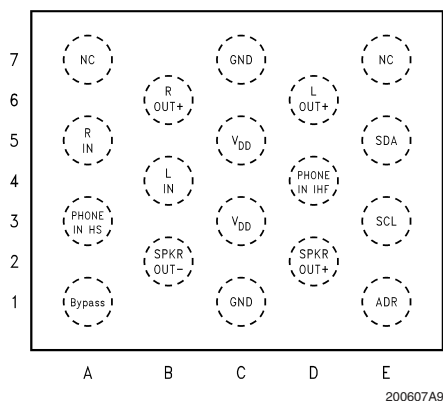


FIGURE 1. Typical Audio Amplifier Application Circuit

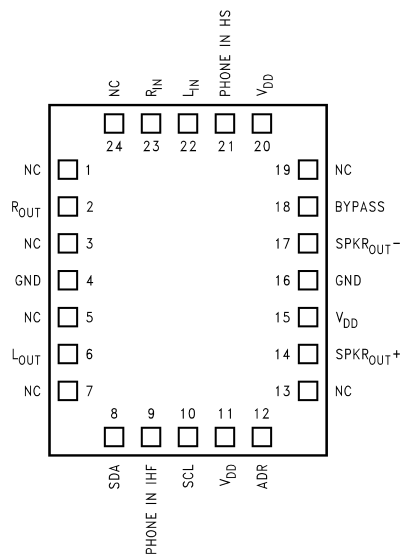


## Connection Diagrams



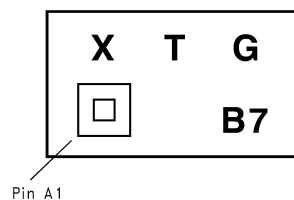
**Top View**  
(Bump-side down)  
Order Number LM4856ITL  
See NS Package Number TLA18AAA

### LLP Package



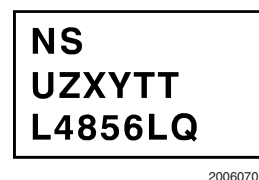
**Top View**  
Order Number LM4856LQ  
See NS Package Number LQA24A for Exposed-DAP LLP

### 18-Bump micro SMD Marking (ITL)



**Top View**  
X - Date Code  
T - Die Traceability  
G - Boomer Family  
B7 - LM4856ITL

### 18 Lead LLP Marking



**Top View**  
NS - Std NS Logo  
U - Wafer Fab Code  
Z - Assembly Plant Code  
XY - 2 Digit Date Code  
TT - Die Run Traceability  
L4856LQ - LM4856LQ

**Absolute Maximum Ratings** (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	6.0V
Storage Temperature	-65°C to +150°C
ESD Susceptibility (Note 4)	2.0kV
ESD Machine model (Note 7)	200V
Junction Temperature (T <sub>J</sub> )	150°C
Solder Information (Note 1)	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

## Thermal Resistance

$\theta_{JA}$ (typ) - LQA24A	42°C/W
$\theta_{JC}$ (typ) - LQA24A	3.0°C/W
$\theta_{JA}$ (typ) - TLA18AAA	48°C/W (Note 9)
$\theta_{JC}$ (typ) - TLA18AAA	23°C/W (Note 9)

**Operating Ratings** (Note 3)

Temperature Range	-40°C to 85°C
Supply Voltage V <sub>DD</sub>	2.6V ≤ V <sub>DD</sub> ≤ 5.0V

**Note 1:** See AN-450 "Surface Mounting and their effects on Product Reliability" for other methods of soldering surface mount devices.

**Electrical Characteristics** (Notes 3, 8)

The following specifications apply for V<sub>DD</sub> = 5.0V, T<sub>A</sub> = 25°C unless otherwise specified.

Symbol	Parameter	Conditions	LM4856		Units (Limits)
			Typical (Note 5)	Limits (Notes 6, 11)	
I <sub>DD</sub>	Supply Current	Output modes 1, 2, 3, 4, 5, 6, 7 V <sub>IN</sub> = 0V; No loads	7.5	11	mA (max)
		Output modes 1, 2, 3, 4, 5, 6, 7 V <sub>IN</sub> = 0V; Loaded ( <i>Figure 1</i> )	8.5	12	mA (max)
I <sub>SD</sub>	Shutdown Current	Output mode 0	0.1	2.0	μA (max)
V <sub>OS</sub>	Output Offset Voltage	V <sub>IN</sub> = 0V	5.0	40	mV (max)
P <sub>O</sub>	Output Power	SPKR <sub>OUT</sub> ; R <sub>L</sub> = 4Ω THD+N = 1%; f = 1kHz, LM4856LQ	1.5		W
		SPKR <sub>OUT</sub> ; R <sub>L</sub> = 8Ω THD+N = 1%; f = 1kHz	1.1	0.8	W (min)
		R <sub>OUT</sub> and L <sub>OUT</sub> ; R <sub>L</sub> = 32Ω THD+N = 0.5%; f = 1kHz	60	45	mW (min)
THD+N	Total Harmonic Distortion Plus Noise	SPKR <sub>OUT</sub> f = 20Hz to 20kHz P <sub>OUT</sub> = 400mW; R <sub>L</sub> = 8Ω	0.5		%
		R <sub>OUT</sub> and L <sub>OUT</sub> f = 20Hz to 20kHz P <sub>OUT</sub> = 15mW; R <sub>L</sub> = 32Ω	0.5		%
N <sub>OUT</sub>	Output Noise	A-weighted (Note 10)	29		μV
PSRR	Power Supply Rejection Ratio SPKR <sub>OUT</sub>	V <sub>RIPPLE</sub> = 200mV <sub>PP</sub> ; f = 217Hz, C <sub>B</sub> = 1.0μF All audio inputs terminated into 50Ω; Output referred Gain (BTL) = 12dB Output Mode 1, 3, 5, 7	58	54	dB (min)
	Power Supply Rejection Ratio R <sub>OUT</sub> and L <sub>OUT</sub>	V <sub>RIPPLE</sub> = 200mV <sub>PP</sub> ; f = 217Hz C <sub>B</sub> = 1.0μF All audio inputs terminated into 50Ω; Output referred Maximum gain setting			
		Output Mode 2, 3	68	59	dB (min)
		Output Mode 4, 5	60	54	dB (min)
		Output Mode 6, 7	56	51	dB (min)
V <sub>IH</sub>	Logic High Input Voltage			0.7 × V <sub>DD</sub>	V (min)
				V <sub>DD</sub>	V (max)

**Electrical Characteristics** (Notes 3, 8) (Continued)The following specifications apply for  $V_{DD} = 5.0V$ ,  $T_A = 25^\circ C$  unless otherwise specified.

Symbol	Parameter	Conditions	LM4856		Units (Limits)
			Typical (Note 5)	Limits (Notes 6, 11)	
$V_{IL}$	Logic Low Input Voltage			0.4 GND	V (max) V (min)
	Digital Volume Range ( $R_{IN}$ and $L_{IN}$ )	Input referred minimum gain	-34.5	-35.1 -33.9	dB (min) dB (max)
		Input referred maximum gain	12.0	11.4 12.6	dB (min) dB (max)
	Digital Volume Range (Phone_In_HS)	Input referred minimum gain	-40.5	-41.1 -39.9	dB (min) dB (max)
		Input referred maximum gain	6.0	5.4 6.6	dB (min) dB (max)
	Digital Volume Stepsize		1.5		dB
	Digital Volume Stepsize Error		$\pm 0.1$	$\pm 0.6$	dB ( max)
	Phone_In_IHF Volume	BTL gain from Phone_In _IHF to $SPKR_{OUT}$	12	11.4 12.6	dB (min) dB (max)
	Phone_In_IHF Mute Attenuation	Output Mode 2, 4, 6	100		dB
	Phone_In_IHF Input Impedance		20	15 25	k $\Omega$ (min) k $\Omega$ (max)
	Phone_In_HS Input Impedance	Maximum gain setting	33.5	25 42	k $\Omega$ (min) k $\Omega$ (max)
		Mininum gain setting	100	75 125	k $\Omega$ (min) k $\Omega$ (max)
	$R_{IN}$ and $L_{IN}$ Input Impedance	Maximum gain setting	20	15 25	k $\Omega$ (min) k $\Omega$ (max)
		Mininum gain setting	100	75 125	k $\Omega$ (min) k $\Omega$ (max)
$T_{SD}$	Thermal Shutdown Temperature		170	150	$^\circ C$ (min)
$t_1$	SCL (Clock) Period			2.5	$\mu s$ (min)
$t_2$	SDA to SCL Set-up Time			100	ns (min)
$t_3$	Data Out Stable Time			0	ns (min)
$t_4$	Start Condition Time			100	ns (min)
$t_5$	Stop Condition Time			100	ns (min)

## Electrical Characteristics (Notes 2, 8)

The following specifications apply for  $V_{DD} = 3.0V$ ,  $T_A = 25^\circ C$  unless otherwise specified.

Symbol	Parameter	Conditions	LM4856		Units (Limits)
			Typical (Note 5)	Limits (Notes 6, 11)	
$I_{DD}$	Supply Current	Output modes 1, 2, 3, 4, 5, 6, 7 $V_{IN} = 0V$ ; No loads	6.5	10	mA (max)
		Output modes 1, 2, 3, 4, 5, 6, 7 $V_{IN} = 0V$ ; Loaded ( <i>Figure 1</i> )	7	11	mA (max)
$I_{SD}$	Shutdown Current	Output mode 0	0.1	2.0	$\mu A$ (max)
$V_{OS}$	Output Offset Voltage	$V_{IN} = 0V$	5.0	40	mV (max)
$P_O$	Output Power	SPKR <sub>OUT</sub> ; $R_L = 4\Omega$ THD+N = 1%; $f = 1kHz$ , LM4856LQ	430		mW
		SPKR <sub>OUT</sub> ; $R_L = 8\Omega$ THD+N = 1%; $f = 1kHz$	340	300	mW (min)
		R <sub>OUT</sub> and L <sub>OUT</sub> ; $R_L = 32\Omega$ THD+N = 0.5%; $f = 1kHz$	22	18	mW (min)
THD+N	Total Harmonic Distortion Plus Noise	SPKR <sub>OUT</sub> $f = 20Hz$ to 20kHz $P_{OUT} = 150mW$ ; $R_L = 8\Omega$	0.5		%
		R <sub>OUT</sub> and L <sub>OUT</sub> $f = 20Hz$ to 20kHz $P_{OUT} = 10mW$ ; $R_L = 32\Omega$	0.5		%
$N_{OUT}$	Output Noise	A-weighted (Note 10)	29		$\mu V$
PSRR	Power Supply Rejection Ratio SPKR <sub>OUT</sub>	$V_{RIPPLE} = 200mV_{PP}$ ; $f = 217Hz$ , $C_B = 1.0\mu F$ All audio inputs terminated into 50 $\Omega$ ; Output referred Gain (BTL) = 12dB Output Mode 1, 3, 5, 7	58	55	dB (min)
	Power Supply Rejection Ratio R <sub>OUT</sub> and L <sub>OUT</sub>	$V_{RIPPLE} = 200mV_{PP}$ ; $f = 217Hz$ , $C_B = 1.0\mu F$ All audio inputs terminated into 50 $\Omega$ ; Output referred Maximum gain setting			
		Output Mode 2, 3	68	60	dB (min)
		Output Mode 4, 5	60	55	dB (min)
		Output Mode 6, 7	56	52	dB (min)
$V_{IH}$	Logic High Input Voltage			$0.7 \times V_{DD}$ $V_{DD}$	V (min) V (max)
$V_{IL}$	Logic Low Input Voltage			0.4 GND	V (max) V (min)

## Electrical Characteristics (Notes 2, 8) (Continued)

The following specifications apply for  $V_{DD} = 3.0V$ ,  $T_A = 25^\circ C$  unless otherwise specified.

Symbol	Parameter	Conditions	LM4856		Units (Limits)
			Typical (Note 5)	Limits (Notes 6, 11)	
	Digital Volume Range ( $R_{IN}$ and $L_{IN}$ )	Input referred minimum gain	-34.5	-35.1 -33.9	dB (min) dB (max)
		Input referred maximum gain	12.0	11.4 12.6	dB (min) dB (max)
	Digital Volume Range (Phone_In_HS)	Input referred minimum gain	-40.5	-41.1 -39.9	dB (min) dB (max)
		Input referred maximum gain	6.0	5.4 6.6	dB (min) dB (max)
	Digital Volume Stepsize		1.5		dB
	Digital Volume Stepsize Error		$\pm 0.1$	$\pm 0.6$	dB ( max)
	Phone_In_IHF Volume	BTL gain from Phone_In_IHF to $SPKR_{OUT}$	12	11.4 12.6	dB (min) dB (max)
	Phone_In_IHF Mute Attenuation	Output Mode 2, 4, 6	100		dB
	Phone_In_IHF Input Impedance		20	15 25	k $\Omega$ (min) k $\Omega$ (max)
	Phone_In_HS Input Impedance	Maximum gain setting	33.5	25 42	k $\Omega$ (min) k $\Omega$ (max)
		Minimum gain setting	100	75 125	k $\Omega$ (min) k $\Omega$ (max)
	$R_{IN}$ and $L_{IN}$ Input Impedance	Maximum gain setting	20	15 25	k $\Omega$ (min) k $\Omega$ (max)
		Minimum gain setting	100	75 125	k $\Omega$ (min) k $\Omega$ (max)
$T_{SD}$	Thermal Shutdown Temperature		170	150	$^\circ C$ (min)
$t_1$	SCL (Clock) Period			2.5	$\mu s$ (min)
$t_2$	SDA to SCL Set-up Time			100	ns (min)
$t_3$	Data Out Stable Time			0	ns (min)
$t_4$	Start Condition Time			100	ns (min)
$t_5$	Stop Condition Time			100	ns (min)

**Note 2:** Absolute Maximum Rating indicate limits beyond which damage to the device may occur.

**Note 3:** Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

**Note 4:** Human body model, 100pF discharged through a 1.5k $\Omega$  resistor.

**Note 5:** Typical specifications are specified at  $+25^\circ C$  and represent the most likely parametric norm.

**Note 6:** Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

**Note 7:** Machine Model ESD test is covered by specification EIAJ IC-121-1981. A 200pF cap is charged to the specified voltage, then discharged directly into the IC with no external series resistor (resistance of discharge path must be under 50 $\Omega$ ).

**Note 8:** All voltages are measured with respect to the ground pin, unless otherwise specified.

**Note 9:** The given  $\theta_{JA}$  and  $\theta_{JC}$  are for an LM4856 mounted on a demonstration board with a 4in<sup>2</sup> area of 1oz printed circuit board copper ground plane.

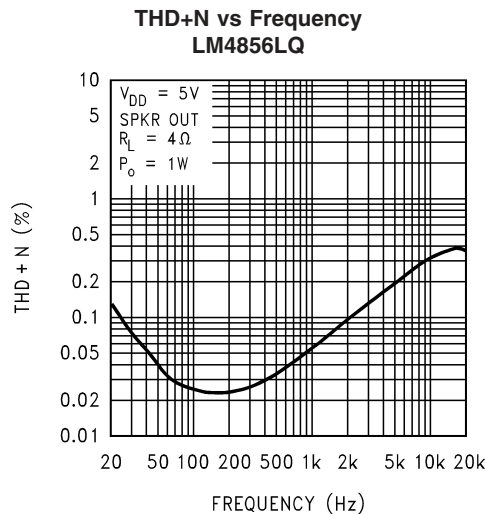
**Note 10:** Please refer to the Output Noise vs Output Mode table in the Typical Performance Characteristics section for more details.

**Note 11:** Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis.

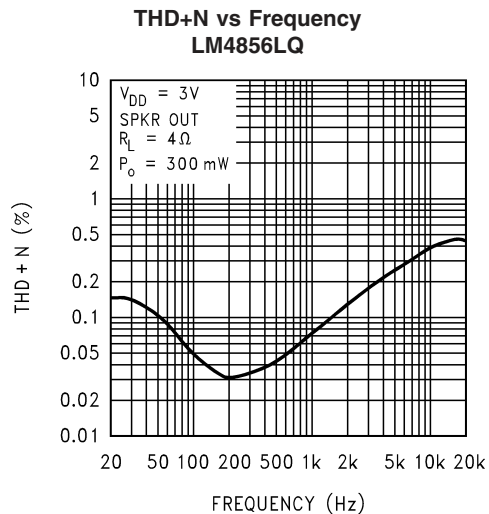
## External Components Description

Components	Functional Description
1. $C_{IN}$	This is the input coupling capacitor. It blocks the DC voltage and couples the input signal to the amplifier's input terminals. $C_{IN}$ also creates a highpass filter with the internal resistor $R_i$ (Input Impedance) at $f_c = 1/(2\pi R_i C_{IN})$ .
2. $C_S$	This is the supply bypass capacitor. It filters the supply voltage applied to the $V_{DD}$ pin and helps maintain the LM4856's PSRR.
3. $C_B$	This is the BYPASS pin capacitor. It filters the $V_{DD} / 2$ voltage and helps maintain the LM4856's PSRR.

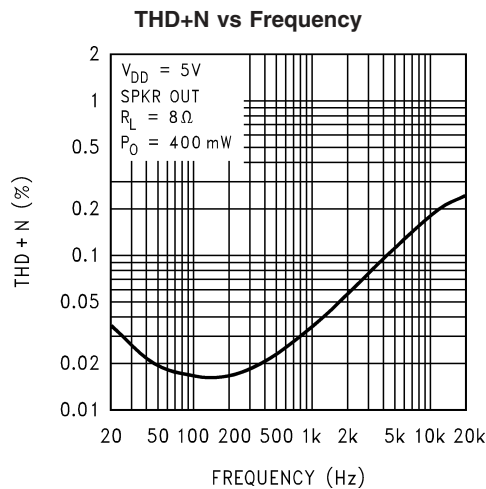
## Typical Performance Characteristics



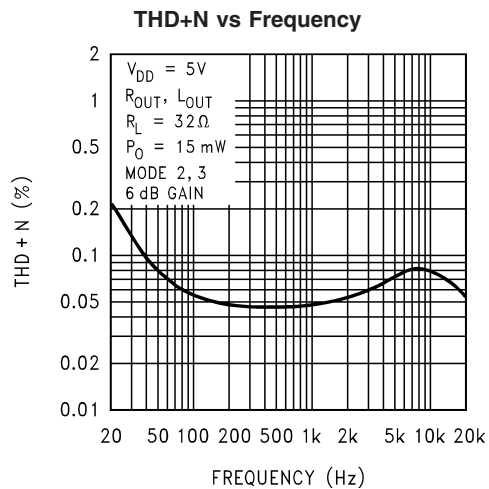
200607F0



200607F1

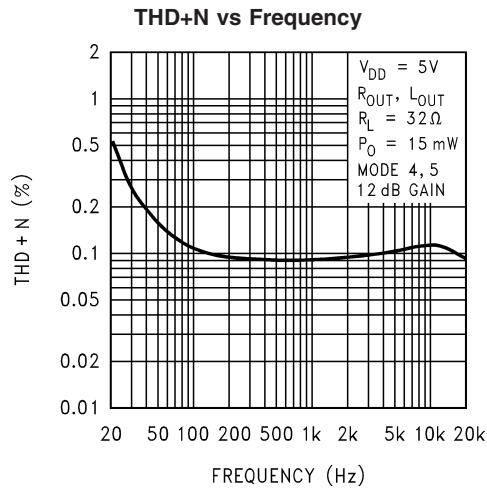


200607B1

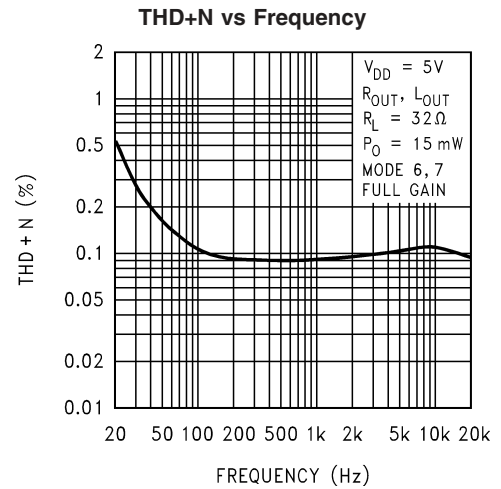


200607G6

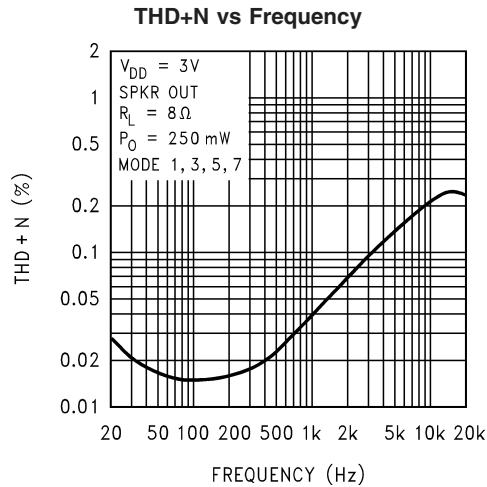
# Typical Performance Characteristics (Continued)



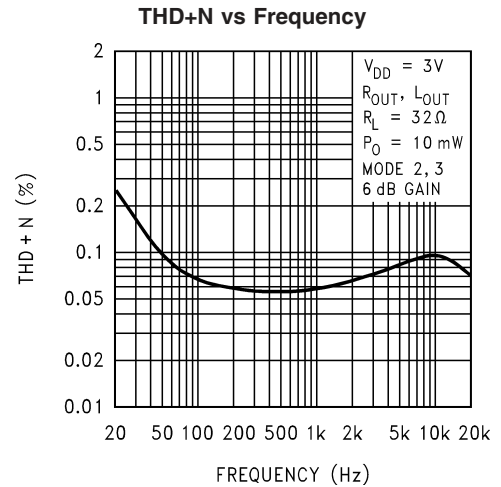
200607G7



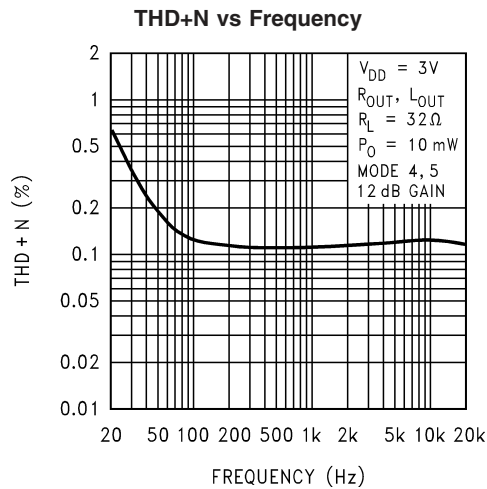
200607G8



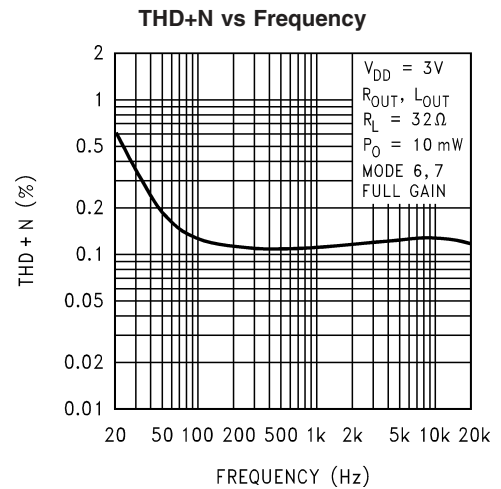
200607B5



200607G9



200607H0

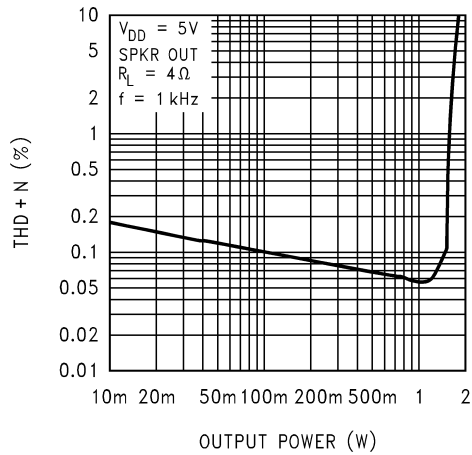


200607H1

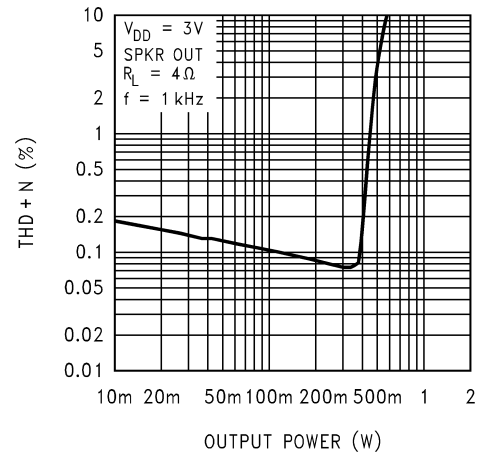


# Typical Performance Characteristics (Continued)

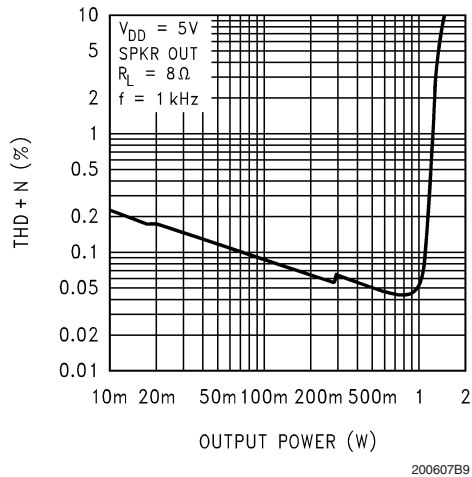
**THD+N vs Output Power**  
**LM4856LQ**



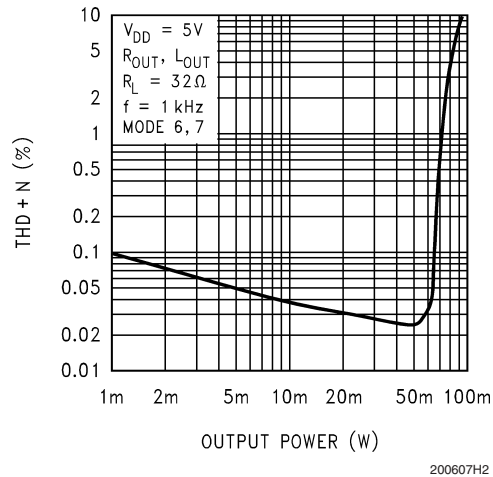
**THD+N vs Output Power**  
**LM4856LQ**



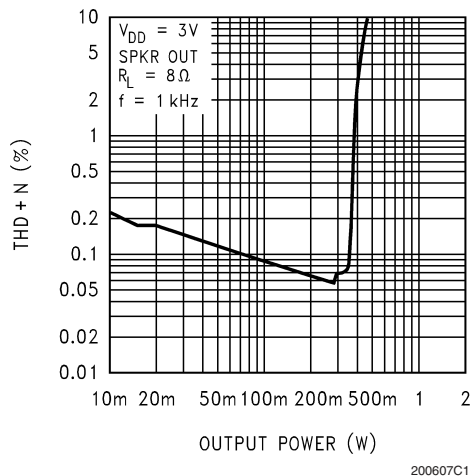
**THD+N vs Output Power**



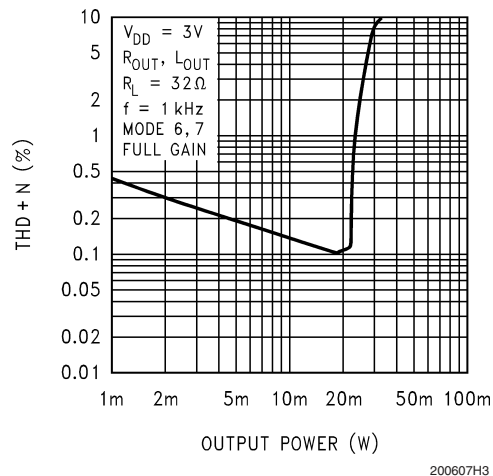
**THD+N vs Output Power**



**THD+N vs Output Power**

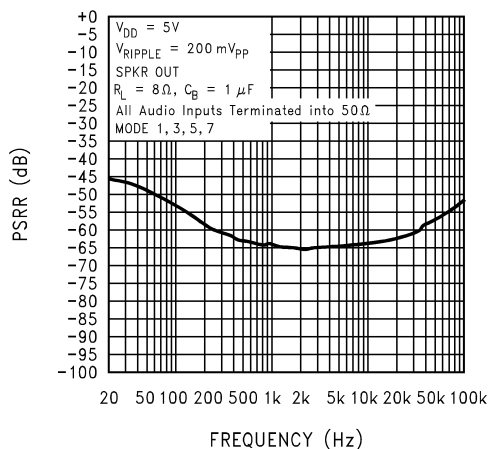


**THD+N vs Output Power**



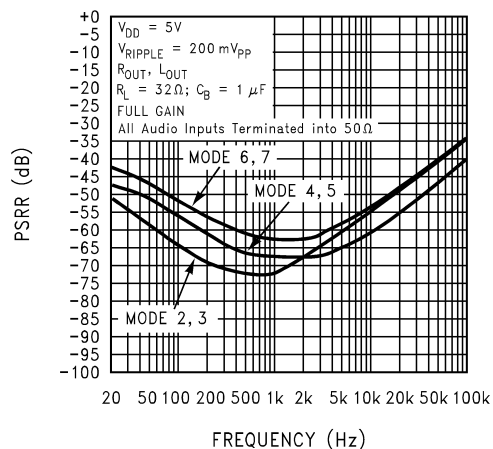
# Typical Performance Characteristics (Continued)

## Power Supply Rejection Ratio



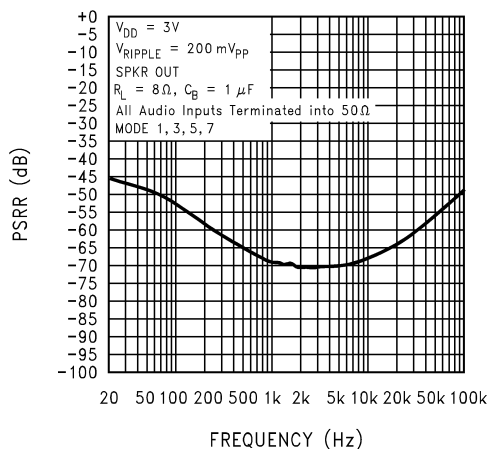
200607C3

## Power Supply Rejection Ratio



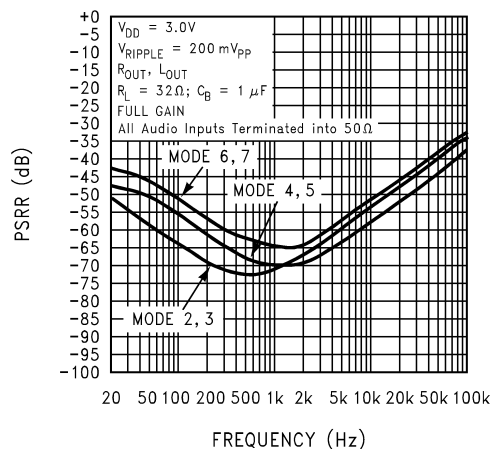
200607H4

## Power Supply Rejection Ratio



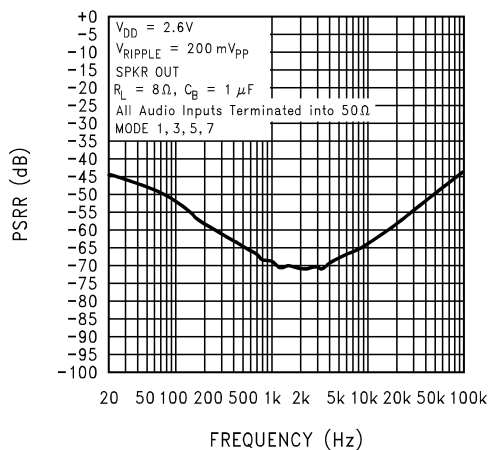
200607C5

## Power Supply Rejection Ratio



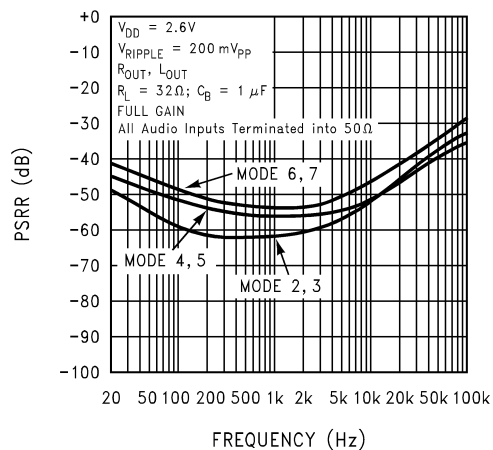
200607H5

## Power Supply Rejection Ratio



200607C7

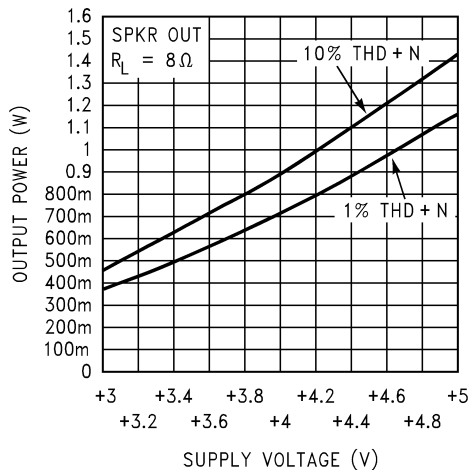
## Power Supply Rejection Ratio



200607H6

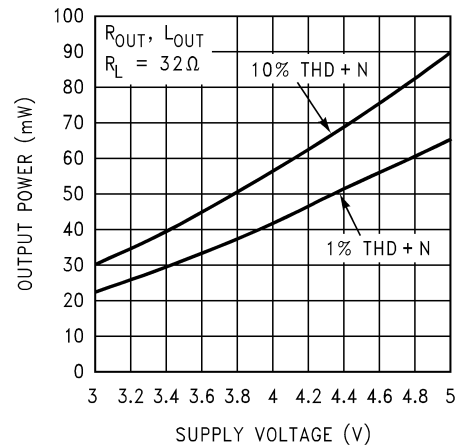
# Typical Performance Characteristics (Continued)

## Output Power vs Supply Voltage



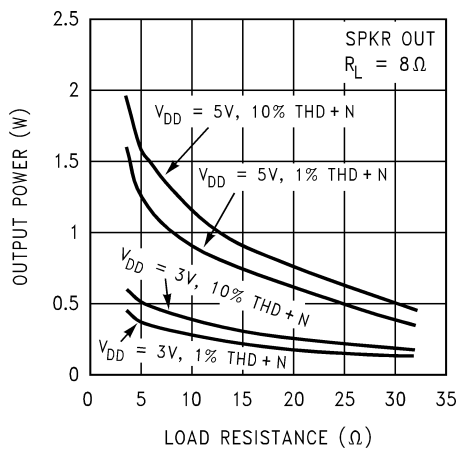
200607D7

## Output Power vs Supply Voltage



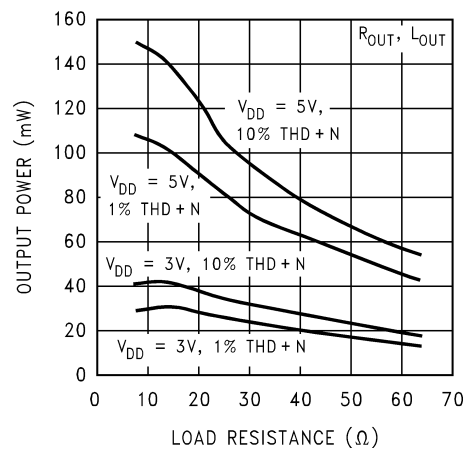
200607H7

## Output Power vs Load Resistance



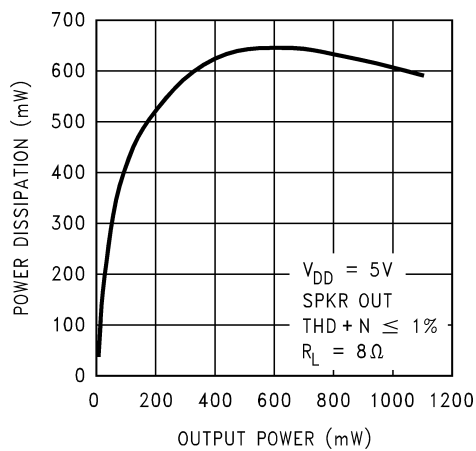
200607D9

## Output Power vs Load Resistance



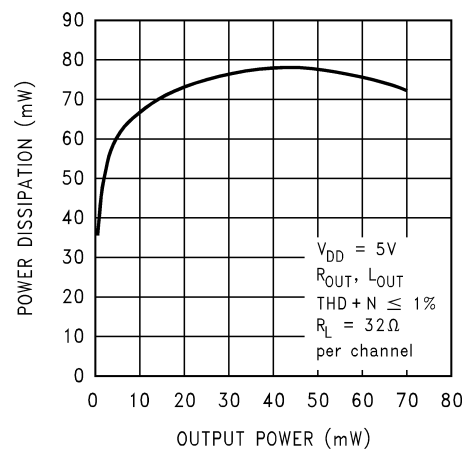
200607H8

## Power Dissipation vs Output Power



200607E1

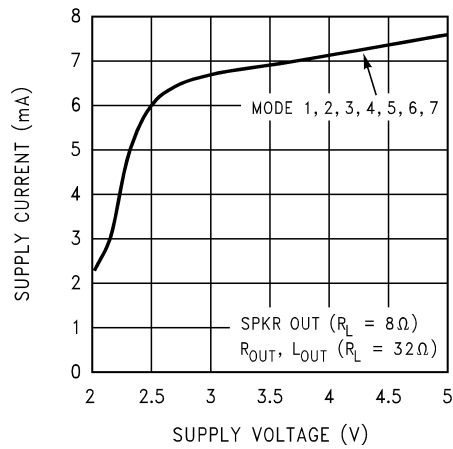
## Power Dissipation vs Output Power



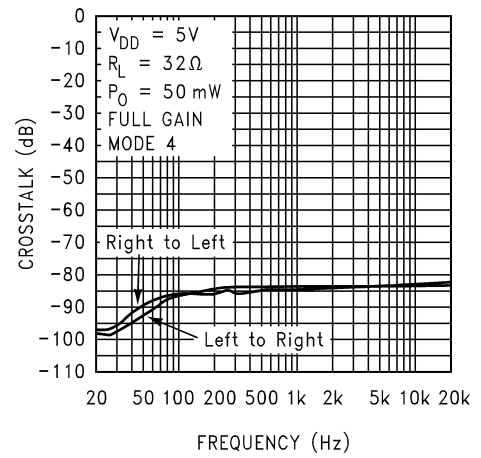
200607H9

# Typical Performance Characteristics (Continued)

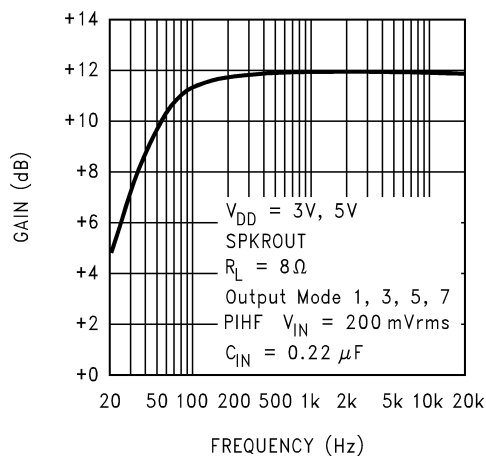
## Supply Current vs Supply Voltage



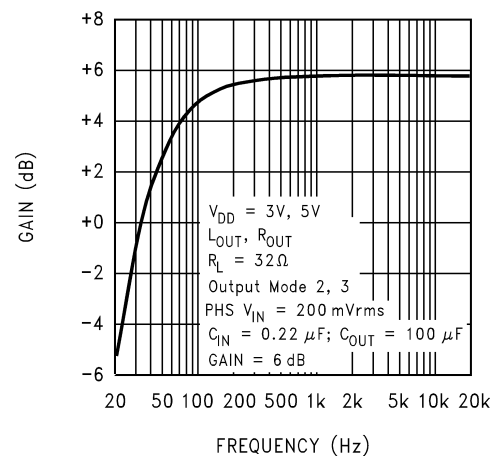
## Channel Separation



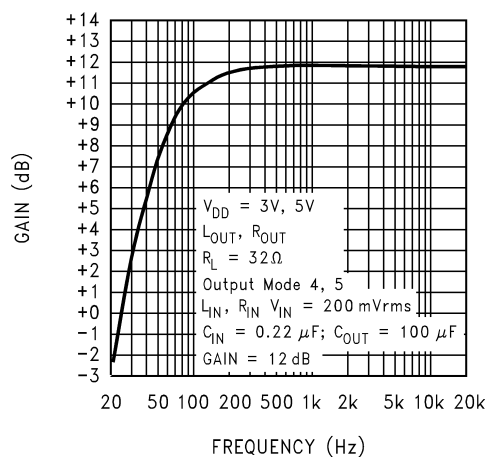
## Frequency Response



## Frequency Response



## Frequency Response



## Typical Performance Characteristics (Continued)

Output Noise vs Output Mode ( $V_{DD} = 3V, 5V$ )

Output Mode	SPKROUT Output Noise ( $\mu V$ )	LOUT/ROUT Output Noise ( $\mu V$ )
1	29	X
2	X	14 ( $G1 = 0dB$ ) 18 ( $G1 = 6dB$ )
3	29	14 ( $G1 = 0dB$ ) 18 ( $G1 = 6dB$ )
4	X	17 ( $G2 = 0dB$ ) 43 ( $G2 = 12dB$ )
5	29	17 ( $G2 = 0dB$ ) 43 ( $G2 = 12dB$ )
6	X	22 ( $G2 = 0dB$ ) 30 ( $G1 = 0dB$ ) 47 ( $G1 = 6dB$ )
7	29	22 ( $G2 = 0dB$ ) 30 ( $G1 = 0dB$ ) 47 ( $G1 = 6dB$ )

$G1$  = gain from  $P_{HS}$  to LOUT/ROUT

$G2$  = gain from LIN/RIN to LOUT/ROUT

A - weighted filter used

## Application Information

### I<sup>2</sup>C PIN DESCRIPTION

SDA: This is the serial data input pin.

SCL: This is the clock input pin.

ADR: This is the address select input pin.

### I<sup>2</sup>C INTERFACE

The LM4856 uses a serial bus, which conforms to the I<sup>2</sup>C protocol, to control the chip's functions with two wires: clock and data. The clock line is uni-directional. The data line is bi-directional (open-collector) with a pullup resistor (typically 10k $\Omega$ ). The maximum clock frequency specified by the I<sup>2</sup>C standard is 400kHz. In this discussion, the master is the controlling microcontroller and the slave is the LM4856.

The I<sup>2</sup>C address for the LM4856 is determined using the ADR pin. The LM4856's two possible I<sup>2</sup>C chip addresses are of the form 110110X<sub>1</sub>0 (binary), where the X<sub>1</sub> = 0, if ADR is logic low; and X<sub>1</sub> = 1, if ADR is logic high. If the I<sup>2</sup>C interface is used to address a number of chips in a system and the LM4856's chip address can be changed to avoid address conflicts.

The timing diagram for the I<sup>2</sup>C is shown in Figure 2. The data is latched in on the stable high level of the clock and the data line should be held high when not in use. The timing diagram is broken up into six major sections:

The "start" signal is generated by lowering the data signal while the clock signal is high. The start signal will alert all devices attached to the I<sup>2</sup>C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the clock level is high.

After the last bit of the address is sent, the master checks for the LM4856's acknowledge. The master releases the data line high (through a pullup resistor). Then the master sends a clock pulse. If the LM4856 has received the address correctly, then it holds the data line low during the clock pulse. If the data line is not low, then the master should send a "stop" signal (discussed later) and abort the transfer.

The 8 bits of data are sent next, most significant bit first. Each data bit should be valid while the clock level is stable high.

After the data byte is sent, the master must generate another acknowledge to see if the LM4856 received the data.

If the master has more data bytes to send to the LM4856, then the master can repeat the previous two steps until all data bytes have been sent.

The "stop" signal ends the transfer. To signal "stop", the data signal goes high while the clock signal is high.

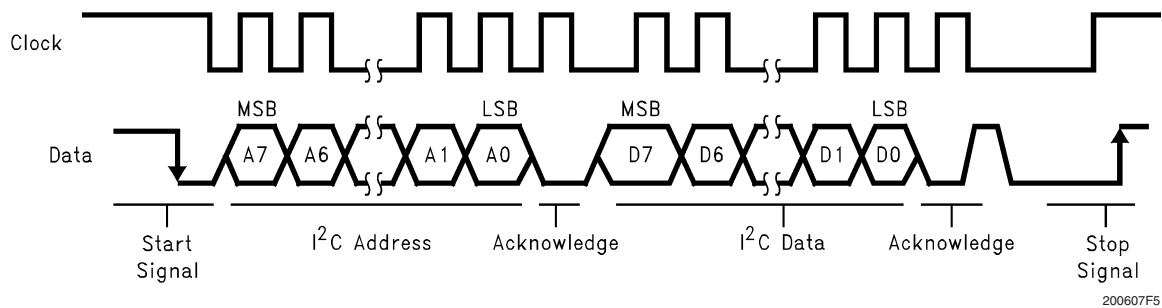


FIGURE 2. I<sup>2</sup>C Bus Format

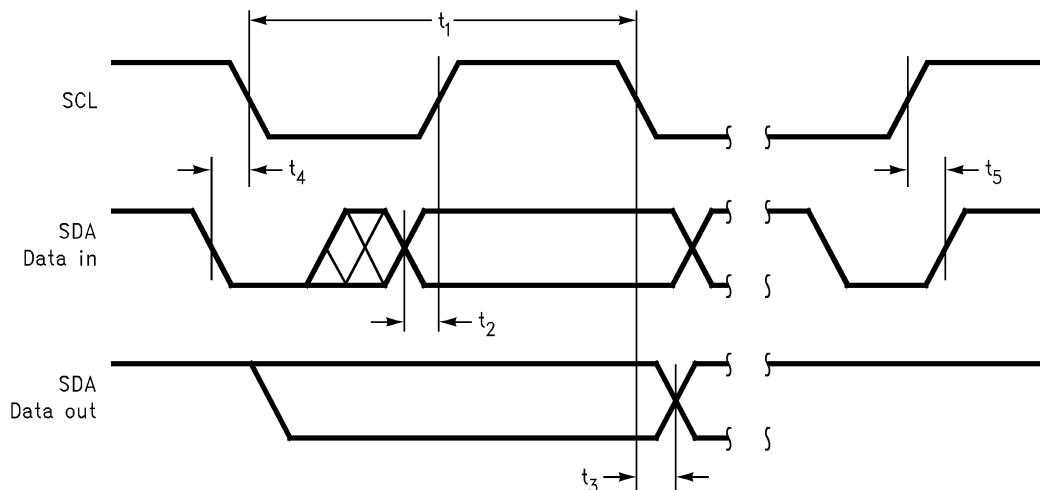


FIGURE 3. I<sup>2</sup>C Timing Diagram

## Application Information (Continued)

**TABLE 1. Data Register**

	DATA							
BIT	D7	D6	D5	D4	D3	D2	D1	D0
Function	Volume Control					Output Mode Control		
Name	V4	V3	V2	V1	V0	M2	M1	M0
Default	0	0	0	0	0	0	0	0

**TABLE 2. Output Mode Selection**

M2	M1	M0	Handsfree Speaker Output	Right Headphone Output	Left Headphone Output	Output Mode Number
0	0	0	SD	SD	SD	0
0	0	1	$12\text{dB} \times P_{\text{IHF}}$	MUTE	MUTE	1
0	1	0	MUTE	$G1 \times P_{\text{HS}}$	$G1 \times P_{\text{HS}}$	2
0	1	1	$12\text{dB} \times P_{\text{IHF}}$	$G1 \times P_{\text{HS}}$	$G1 \times P_{\text{HS}}$	3
1	0	0	MUTE	$G2 \times R$	$G2 \times L$	4
1	0	1	$12\text{dB} \times P_{\text{IHF}}$	$G2 \times R$	$G2 \times L$	5
1	1	0	MUTE	$(G1 \times P_{\text{HS}}) + (G2 \times R)$	$(G1 \times P_{\text{HS}}) + (G2 \times L)$	6
1	1	1	$12\text{dB} \times P_{\text{IHF}}$	$(G1 \times P_{\text{HS}}) + (G2 \times R)$	$(G1 \times P_{\text{HS}}) + (G2 \times L)$	7

$P_{\text{IHF}}$  = External High Pass Phone\_In\_IHF

$P_{\text{HS}}$  = Non Filtered Phone\_In\_HS

$R = R_{\text{IN}}$

$L = L_{\text{IN}}$

SD = Shutdown

MUTE = Mute Mode

$G1$  = gain from  $P_{\text{HS}}$  to  $L_{\text{OUT}}$  and  $R_{\text{OUT}}$

$G2$  = gain from  $L_{\text{IN}}$  and  $R_{\text{IN}}$  to  $L_{\text{OUT}}$  and  $R_{\text{OUT}}$

$G1 = G2 + 6\text{dB}$

## Application Information (Continued)

TABLE 3. Volume Control

V4	V3	V2	V1	V0	Gain (dB)	
					G2	G1
					$R_{IN}, L_{IN}$ to $R_{OUT}, L_{OUT}$	$P_{HS}$ to $R_{OUT}, L_{OUT}$
0	0	0	0	0	-34.5	-40.5
0	0	0	0	1	-33.0	-39.0
0	0	0	1	0	-31.5	-37.5
0	0	0	1	1	-30.0	-36.0
0	0	1	0	0	-28.5	-34.5
0	0	1	0	1	-27.0	-33.0
0	0	1	1	0	-25.5	-31.5
0	0	1	1	1	-24.0	-30.0
0	1	0	0	0	-22.5	-28.5
0	1	0	0	1	-21.0	-27.0
0	1	0	1	0	-19.5	-25.5
0	1	0	1	1	-18.0	-24.0
0	1	1	0	0	-16.5	-22.5
0	1	1	0	1	-15.0	-21.0
0	1	1	1	0	-13.5	-19.5
0	1	1	1	1	-12.0	-18.0
1	0	0	0	0	-10.5	-16.5
1	0	0	0	1	-9.0	-15.0
1	0	0	1	0	-7.5	-13.5
1	0	0	1	1	-6.0	-12.0
1	0	1	0	0	-4.5	-10.5
1	0	1	0	1	-3.0	-9.0
1	0	1	1	0	-1.5	-7.5
1	0	1	1	1	0.0	-6.0
1	1	0	0	0	1.5	-4.5
1	1	0	0	1	3.0	-3.0
1	1	0	1	0	4.5	-1.5
1	1	0	1	1	6.0	0.0
1	1	1	0	0	7.5	1.5
1	1	1	0	1	9.0	3.0
1	1	1	1	0	10.5	4.5
1	1	1	1	1	12.0	6.0

### EXPOSED-DAP MOUNTING CONSIDERATIONS

The LM4856's exposed-DAP (die attach paddle) package (LD) provides a low thermal resistance between the die and the PCB to which the part is mounted and soldered. This allows rapid heat transfer from the die to the surrounding PCB copper area heatsink, copper traces, ground plane, and finally, surrounding air. The result is a low voltage audio power amplifier that produces 1.1W dissipation in a 8Ω load at ≤ 1% THD+N. This high power is achieved through careful consideration of necessary thermal design. Failing to optimize thermal design may compromise the LM4856's high power performance and activate unwanted, though necessary, thermal shutdown protection.

The LD package must have its DAP soldered to a copper pad on the PCB. The DAP's PCB copper pad is then, ideally,

connected to a large plane of continuous unbroken copper. This plane forms a thermal mass, heat sink, and radiation area. Place the heat sink area on either outside plane in the case of a two-sided or multi-layer PCB. (The heat sink area can also be placed on an inner layer of a multi-layer board. The thermal resistance, however, will be higher.) Connect the DAP copper pad to the inner layer or backside copper heat sink area with 6 (3 X 2) (LD) vias. The via diameter should be 0.012in - 0.013in with a 1.27mm pitch. Ensure efficient thermal conductivity by plugging and tenting the vias with plating and solder mask, respectively.

Best thermal performance is achieved with the largest practical copper heat sink area. If the heatsink and amplifier share the same PCB layer, a nominal 2.5in<sup>2</sup> (min) area is necessary for 5V operation with a 4Ω load. Heatsink areas



## Application Information (Continued)

not placed on the same PCB layer as the LM4856 should be  $5\text{in}^2$  (min) for the same supply voltage and load resistance. The last two area recommendations apply for  $25^\circ\text{C}$  ambient temperature. Increase the area to compensate for ambient temperatures above  $25^\circ\text{C}$ . In all circumstances and under all conditions, the junction temperature must be held below  $150^\circ\text{C}$  to prevent activating the LM4856's thermal shutdown protection. Further detailed and specific information concerning PCB layout and fabrication and mounting an LD (LLP) is found in National Semiconductor's AN1187.

### PCB LAYOUT AND SUPPLY REGULATION CONSIDERATIONS FOR DRIVING $3\Omega$ AND $4\Omega$ LOADS

Power dissipated by a load is a function of the voltage swing across the load and the load's impedance. As load impedance decreases, load dissipation becomes increasingly dependent on the interconnect (PCB trace and wire) resistance between the amplifier output pins and the load's connections. Residual trace resistance causes a voltage drop, which results in power dissipated in the trace and not in the load as desired. For example,  $0.1\Omega$  trace resistance reduces the output power dissipated by a  $4\Omega$  load from  $1.7\text{W}$  to  $1.6\text{W}$ . The problem of decreased load dissipation is exacerbated as load impedance decreases. Therefore, to maintain the highest load dissipation and widest output voltage swing, PCB traces that connect the output pins to a load must be as wide as possible.

Poor power supply regulation adversely affects maximum output power. A poorly regulated supply's output voltage decreases with increasing load current. Reduced supply voltage causes decreased headroom, output signal clipping, and reduced output power. Even with tightly regulated supplies, trace resistance creates the same effects as poor supply regulation. Therefore, making the power supply traces as wide as possible helps maintain full output voltage swing.

### BRIDGE CONFIGURATION EXPLANATION

As shown in *Figure 1*, the LM4856 consists of three pairs of output amplifier blocks (A4-A6). Amplifier block A6 consists of a bridged-tied amplifier pair that drives SPKROUT. The LM4856 drives a load, such as a speaker, connected between outputs, SPKROUT+ and SPKROUT-. In the amplifier block A6, the output of the amplifier that drives SPKROUT- serves as the input to the unity gain inverting amplifier that drives SPKROUT+.

This results in both amplifiers producing signals identical in magnitude, but  $180^\circ$  out of phase. Taking advantage of this phase difference, a load is placed between SPKROUT- and SPKROUT+ and driven differentially (commonly referred to as 'bridge mode'). This results in a differential or BTL gain of:

$$A_{VD} = 2(R_f / R_i) = 2 \quad (1)$$

Bridge mode amplifiers are different from single-ended amplifiers that drive loads connected between a single amplifier's output and ground. For a given supply voltage, bridge mode has a distinct advantage over the single-ended configuration: its differential output doubles the voltage swing across the load. Theoretically, this produces four times the output power when compared to a single-ended amplifier

under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited and that the output signal is not clipped.

Another advantage of the differential bridge output is no net DC voltage across the load. This is accomplished by biasing SPKROUT- and SPKROUT+ outputs at half-supply. This eliminates the coupling capacitor that single supply, single-ended amplifiers require. Eliminating an output coupling capacitor in a typical single-ended configuration forces a single-supply amplifier's half-supply bias voltage across the load. This increases internal IC power dissipation and may permanently damage loads such as speakers.

### POWER DISSIPATION

Power dissipation is a major concern when designing a successful single-ended or bridged amplifier.

A direct consequence of the increased power delivered to the load by a bridge amplifier is higher internal power dissipation. The LM4856 has a pair of bridged-tied amplifiers driving a handsfree speaker, SPKROUT. The maximum internal power dissipation operating in the bridge mode is twice that of a single-ended amplifier. From Equation (2), assuming a  $5\text{V}$  power supply and an  $8\Omega$  load, the maximum SPKROUT power dissipation is  $634\text{mW}$ .

$$P_{\text{DMAX-SPKROUT}} = 4(V_{DD})^2 / (2\pi^2 R_L): \text{Bridge Mode} \quad (2)$$

The LM4856 also has a pair of single-ended amplifiers driving stereo headphones, ROUT and LOUT. The maximum internal power dissipation for ROUT and LOUT is given by equation (3) and (4). From Equations (3) and (4), assuming a  $5\text{V}$  power supply and a  $32\Omega$  load, the maximum power dissipation for LOUT and ROUT is  $40\text{mW}$ , or  $80\text{mW}$  total.

$$P_{\text{DMAX-LOUT}} = (V_{DD})^2 / (2\pi^2 R_L): \text{Single-ended Mode} \quad (3)$$

$$P_{\text{DMAX-ROUT}} = (V_{DD})^2 / (2\pi^2 R_L): \text{Single-ended Mode} \quad (4)$$

The maximum internal power dissipation of the LM4856 occurs when all 3 amplifiers pairs are simultaneously on; and is given by Equation (5).

$$P_{\text{DMAX-TOTAL}} = P_{\text{DMAX-SPKROUT}} + P_{\text{DMAX-LOUT}} + P_{\text{DMAX-ROUT}} \quad (5)$$

The maximum power dissipation point given by Equation (5) must not exceed the power dissipation given by Equation (6):

$$P_{\text{DMAX}}' = (T_{J\text{MAX}} - T_A) / \theta_{JA} \quad (6)$$

The LM4856's  $T_{J\text{MAX}} = 150^\circ\text{C}$ . In the ITL package, the LM4856's  $\theta_{JA}$  is  $48^\circ\text{C/W}$ . In the LD package soldered to a DAP pad that expands to a copper area of  $2.5\text{in}^2$  on a PCB, the LM4856's  $\theta_{JA}$  is  $42^\circ\text{C/W}$ . At any given ambient temperature  $T_A$ , use Equation (6) to find the maximum internal power dissipation supported by the IC packaging. Rearranging Equation (6) and substituting  $P_{\text{DMAX-TOTAL}}$  for  $P_{\text{DMAX}}'$  results in Equation (7). This equation gives the maximum ambient

## Application Information (Continued)

temperature that still allows maximum stereo power dissipation without violating the LM4856's maximum junction temperature.

$$T_A = T_{JMAX} - P_{DMAX-TOTAL} \theta_{JA} \quad (7)$$

For a typical application with a 5V power supply and an 8Ω load, the maximum ambient temperature that allows maximum stereo power dissipation without exceeding the maximum junction temperature is approximately 104°C for the IBL package.

$$T_{JMAX} = P_{DMAX-TOTAL} \theta_{JA} + T_A \quad (8)$$

Equation (8) gives the maximum junction temperature  $T_{JMAX}$ . If the result violates the LM4856's 150°C, reduce the maximum junction temperature by reducing the power supply voltage or increasing the load resistance. Further allowance should be made for increased ambient temperatures.

The above examples assume that a device is a surface mount part operating around the maximum power dissipation point. Since internal power dissipation is a function of output power, higher ambient temperatures are allowed as output power or duty cycle decreases. If the result of Equation (5) is greater than that of Equation (6), then decrease the supply voltage, increase the load impedance, or reduce the ambient temperature. If these measures are insufficient, a heat sink can be added to reduce  $\theta_{JA}$ . The heat sink can be created using additional copper area around the package, with connections to the ground pin(s), supply pin and amplifier output pins. External, solder attached SMT heatsinks such as the Thermalloy 7106D can also improve power dissipation. When adding a heat sink, the  $\theta_{JA}$  is the sum of  $\theta_{JC}$ ,  $\theta_{CS}$ , and  $\theta_{SA}$ . ( $\theta_{JC}$  is the junction-to-case thermal impedance,  $\theta_{CS}$  is the case-to-sink thermal impedance, and  $\theta_{SA}$  is the sink-to-ambient thermal impedance.) Refer to the Typical Performance Characteristics curves for power dissipation information at lower output power levels.

### POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. Applications that employ a 5V regulator typically use a 10μF in parallel with a 0.1μF filter capacitors to stabilize the regulator's output, reduce noise on the supply line, and improve the supply's transient response. However, their presence does not eliminate the need for a local 1.0μF tantalum bypass capacitance connected between the LM4856's supply pins and ground. Keep the length of leads and traces that connect capacitors between the LM4856's power supply pin and ground as short as possible. Connecting a 1μF capacitor,  $C_B$ , between the BYPASS pin and ground improves the internal bias voltage's stability and improves the amplifier's PSRR. The PSRR improvements increase as the bypass pin capacitor value increases. Too large, however, increases turn-on time and can compromise the amplifier's click and pop performance. The selection of bypass capacitor values, especially  $C_B$ , depends on desired PSRR requirements, click and pop performance (as explained in the section, Proper Selection of External Components), system cost, and size constraints.

## SELECTING EXTERNAL COMPONENTS

### Input Capacitor Value Selection

Amplifying the lowest audio frequencies requires high value input coupling capacitor ( $C_i$  in *Figure 3*). A high value capacitor can be expensive and may compromise space efficiency in portable designs. In many cases, however, the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 150Hz. Applications using speakers with this limited frequency response reap little improvement by using large input capacitor.

The internal input resistor ( $R_i$ ) and the input capacitor ( $C_i$ ) produce a high pass filter cutoff frequency that is found using Equation (9).

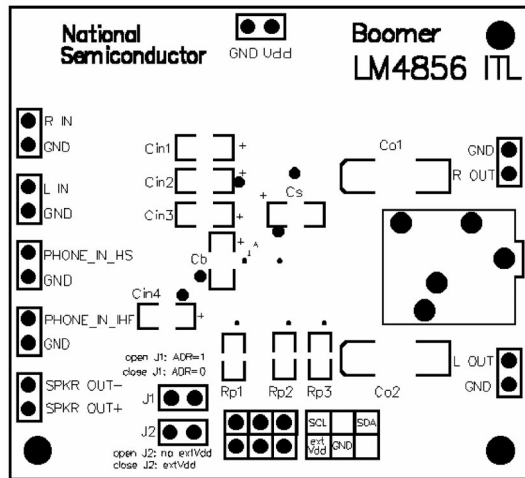
$$f_c = 1 / (2\pi R_i C_i) \quad (9)$$

As an example when using a speaker with a low frequency limit of 150Hz,  $C_i$ , using Equation (9) is 0.063μF. The 0.22μF  $C_i$  shown in *Figure 1* allows the LM4856 to drive high efficiency, full range speaker whose response extends below 40Hz.

### Bypass Capacitor Value Selection

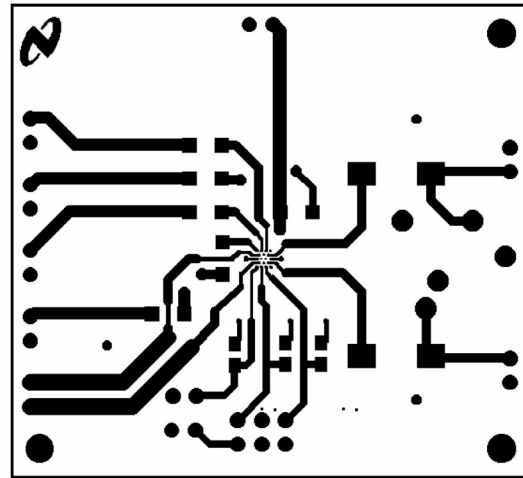
Besides minimizing the input capacitor size, careful consideration should be paid to value of  $C_B$ , the capacitor connected to the BYPASS pin. Since  $C_B$  determines how fast the LM4856 settles to quiescent operation, its value is critical when minimizing turn-on pops. The slower the LM4856's outputs ramp to their quiescent DC voltage (nominally  $V_{DD}/2$ ), the smaller the turn-on pop. Choosing  $C_B$  equal to 1.0μF along with a small value of  $C_i$  (in the range of 0.1μF to 0.39μF), produces a click-less and pop-less shutdown function. As discussed above, choosing  $C_i$  no larger than necessary for the desired bandwidth helps minimize clicks and pops.  $C_B$ 's value should be in the range of 5 times to 7 times the value of  $C_i$ . This ensures that output transients are eliminated when power is first applied or the LM4856 resumes operation after shutdown.

## Demonstration ITL/LQ Board Layout



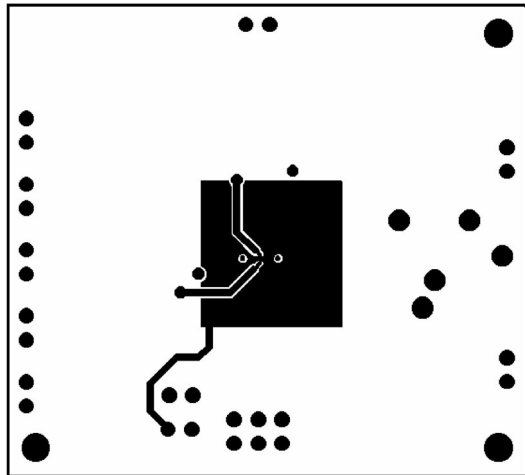
200607G0

Recommended ITL PC Board Layout:  
Top Overlay Layer



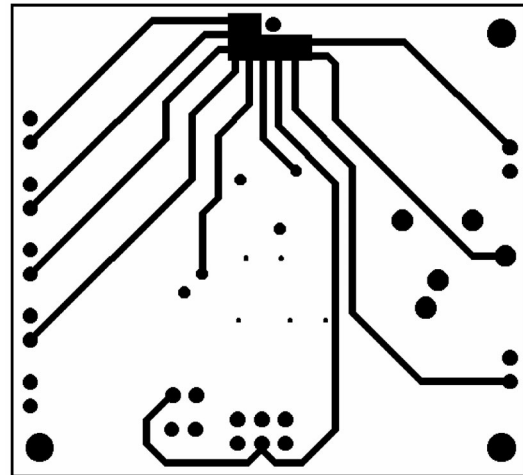
200607F9

Recommended ITL PC Board Layout:  
Top Layer



200607F7

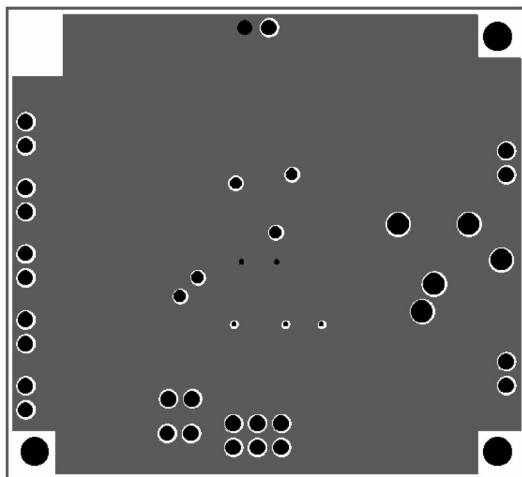
Recommended ITL PC Board Layout:  
Middle 1 Layer



200607F8

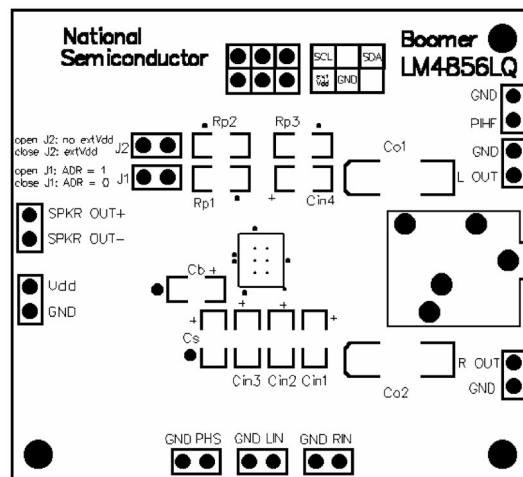
Recommended ITL PC Board Layout:  
Middle 2 Layer

## Demonstration ITL/LQ Board Layout (Continued)



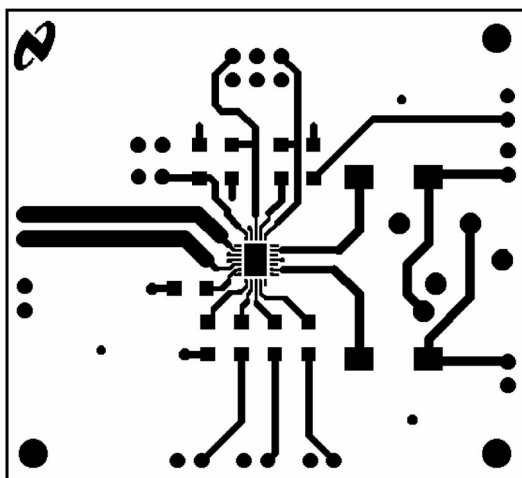
200607F6

Recommended ITL PC Board Layout:  
Bottom Layer



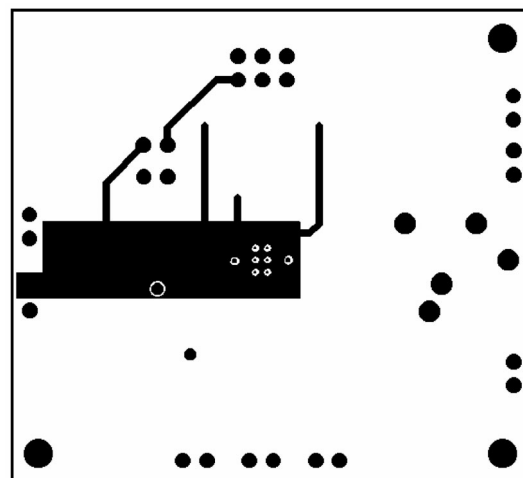
200607G5

Recommended LQ PC Board Layout:  
Top Overlay Layer



200607G4

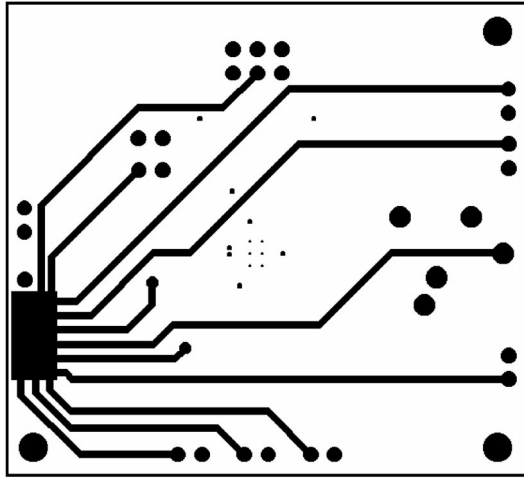
Recommended LQ PC Board Layout:  
Top Layer



200607G2

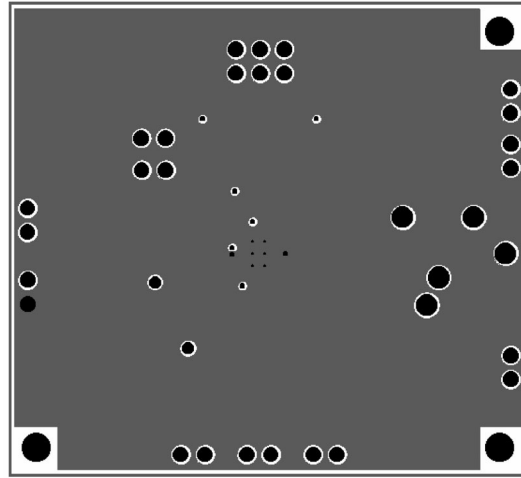
Recommended LQ PC Board Layout:  
Middle 1 Layer

## Demonstration ITL/LQ Board Layout (Continued)



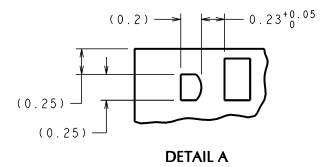
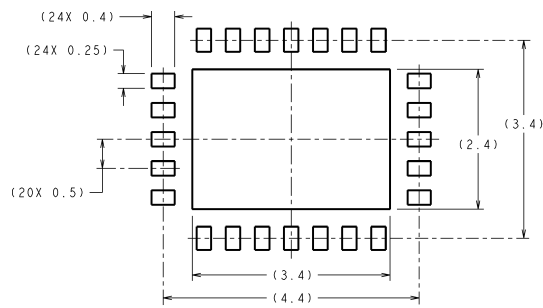
200607G3

**Recommended LQ PC Board Layout:  
Middle 2 Layer**

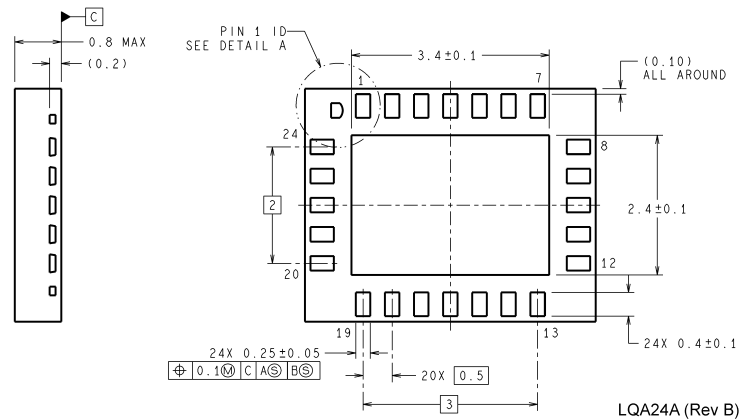
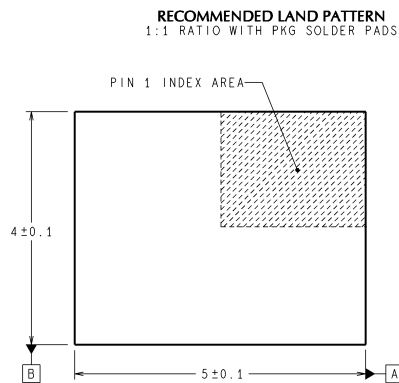


200607G1

**Recommended LQ PC Board Layout:  
Bottom Layer**

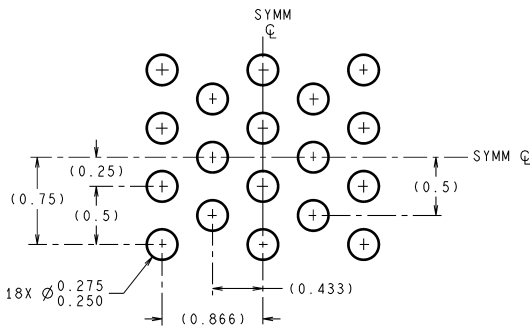


**DIMENSIONS ARE IN MILLIMETERS**  
DIMENSIONS IN ( ) FOR REFERENCE ONLY

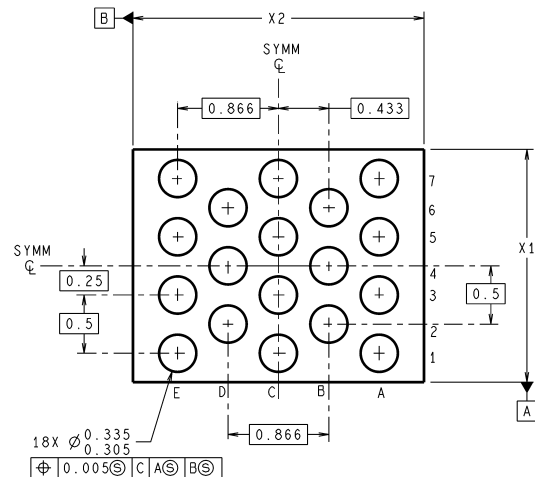
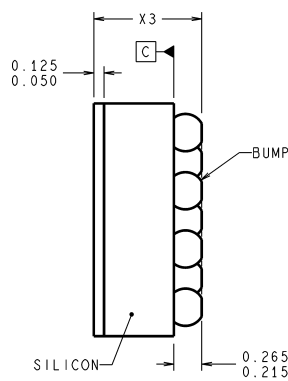
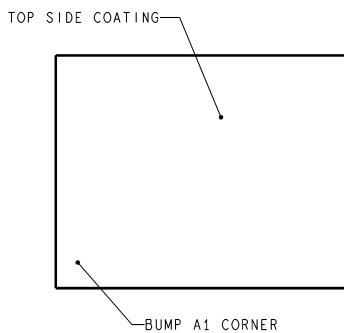


**24-Lead MOLDED PKG, Leadless Leadframe Package LLP**  
**Order Number LM4856LQ**  
**NS Package Number LQA24A**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



### LAND PATTERN RECOMMENDATION



TLA18XXX (Rev C)

**18-Bump micro SMD**  
**Order Number LM4856ITL**  
**NS Package Number TLA18AAA**  
 **$X_1 = 1.996$   $X_2 = 2.225$   $X_3 = 0.600$**

## LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

## BANNED SUBSTANCE COMPLIANCE

National Semiconductor certifies that the products and packing materials meet the provisions of the Customer Products Stewardship Specification (CSP-9-111C2) and the Banned Substances and Materials of Interest Specification (CSP-9-111S2) and contain no "Banned Substances" as defined in CSP-9-111S2.



**National Semiconductor**  
**Americas Customer**  
**Support Center**  
Email: new.feedback@nsc.com  
Tel: 1-800-272-9959

www.national.com

**National Semiconductor**  
**Europe Customer Support Center**  
Fax: +49 (0) 180-530 85 86  
Email: europe.support@nsc.com  
Deutsch Tel: +49 (0) 69 9508 6208  
English Tel: +44 (0) 870 24 0 2171  
Français Tel: +33 (0) 1 41 91 8790

**National Semiconductor**  
**Asia Pacific Customer**  
**Support Center**  
Email: ap.support@nsc.com

**National Semiconductor**  
**Japan Customer Support Center**  
Fax: 81-3-5639-7507  
Email: jpn.feedback@nsc.com  
Tel: 81-3-5639-7560