



Low Voltage, Micropower Sampling 8-Bit Serial I/O A/D Converters

December 1995

FEATURES

- Specified at 2.65V Minimum Supply
- Maximum Supply Current: 80 μ A
- Auto Shutdown to 1nA
- 8-Pin SO Package**
- On-Chip Sample-and-Hold
- Conversion Time: 32 μ s
- Sample Rates: 16.5ksp/s
- I/O Compatible with SPI, MICROWIRE™, etc.

APPLICATIONS

- Battery-Operated Systems
- Remote Data Acquisition
- Isolated Data Acquisition
- Battery Monitoring
- Temperature Measurement

DESCRIPTION

The LTC®1096L/LTC1098L are 3V micropower, 8-bit successive approximation sampling A/D converters. They typically draw only 40 μ A of supply current when converting and automatically power down to a typical supply current of 1nA between conversions. They are packaged in 8-pin SO packages and operate on a 3V supply. These 8-bit, switched capacitor, successive approximation ADCs include a sample-and-hold. The LTC1096L has a single differential analog input. The LTC1098L offers a software selectable 2-channel multiplexed input.

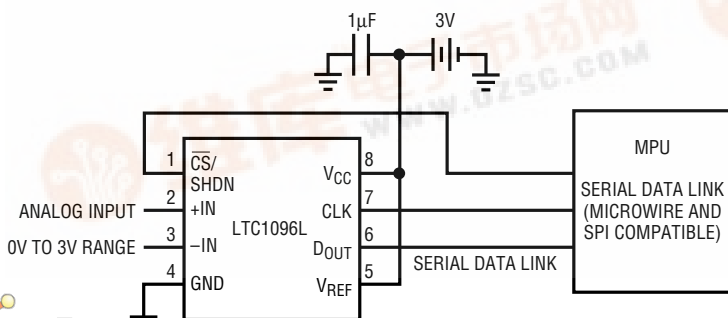
On-chip serial ports allow efficient data transfer to a wide range of microprocessors and microcontrollers over three wires. This, coupled with micropower consumption, makes remote location possible and facilitates transmitting data through isolation barriers.

The circuits can be used in ratiometric applications or with an external reference. The high impedance analog inputs and the ability to operate with reduced spans (to 1V full scale) allow direct connection to sensors and transducers in many applications, eliminating the need for gain stages.

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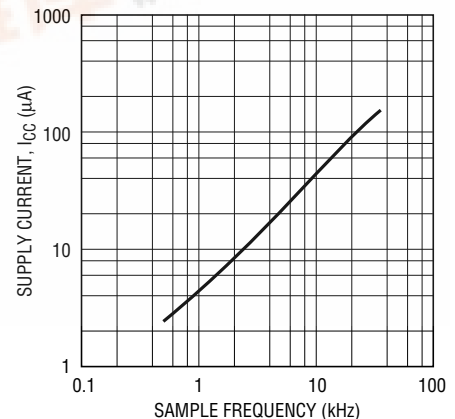
TYPICAL APPLICATION

10 μ W, SO-8 Package, 8-Bit A/D Converter
Samples at 200Hz and Runs Off a 3V Battery



1096/8 TA01

Supply Current vs Sample Rate



1096/8 TA02



LTC1096L/LTC1098L

ABSOLUTE MAXIMUM RATINGS (Notes 1 and 2)

Supply Voltage (V_{CC}) to GND	12V	Operating Temperature	
Voltage		LTC1096LAC/LTC1098LAC	0°C to 70°C
Analog and Reference	-0.3V to $V_{CC} + 0.3V$	LTC1096LAI/LTC1098LAI	-40°C to 85°C
Digital Inputs	-0.3V to 12V	LTC1096LC/LTC1098LC	0°C to 70°C
Digital Outputs	-0.3V to $V_{CC} + 0.3V$	LTC1096LI/LTC1098LI	-40°C to 85°C
Power Dissipation	500mW	Storage Temperature Range	-65°C to 150°C
		Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION (Note 3)

TOP VIEW	ORDER PART NUMBER	TOP VIEW	ORDER PART NUMBER
<p>S8 PACKAGE 8-LEAD PLASTIC SO $T_{JMAX} = 150^{\circ}C$, $\theta_{JA} = 175^{\circ}C/W$</p>	LTC1096LACS8 LTC1096LAIS8 LTC1096LCS8 LTC1096LIS8	<p>S8 PACKAGE 8-LEAD PLASTIC SO $T_{JMAX} = 150^{\circ}C$, $\theta_{JA} = 175^{\circ}C/W$</p>	LTC1098LACS8 LTC1098LAIS8 LTC1098LCS8 LTC1098LIS8
	S8 PART MARKING		S8 PART MARKING
	096LIA 1096LA 1096LI 1096L		098LIA 1098LA 1098LI 1098L

Consult factory for Military grade parts.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage		2.65		4.0	V
f_{CLK}	Clock Frequency	$V_{CC} = 2.65V$	25		250	kHz
t_{CYC}	Total Cycle Time	LTC1096L, $f_{CLK} = 250kHz$ LTC1098L, $f_{CLK} = 250kHz$	58			μs
t_{hDI}	Hold Time, D_{IN} After $CLK\uparrow$	$V_{CC} = 2.65V$	450			ns
$t_{su\overline{CS}}$	Setup Time $\overline{CS}\downarrow$ Before First $CLK\uparrow$ (See Operating Sequence)	$V_{CC} = 2.65V$, LTC1096L $V_{CC} = 2.65V$, LTC1098L	1			μs
t_{WAKEUP}	Wakeup Time $\overline{CS}\downarrow$ Before First $CLK\downarrow$ After First $CLK\uparrow$ (See Figure 1, LTC1096L Operating Sequence)	$V_{CC} = 2.65V$, LTC1096L	10			μs
	Wakeup Time $\overline{CS}\downarrow$ Before MSBF Bit $CLK\downarrow$ (See Figure 2, LTC1098L Operating Sequence)	$V_{CC} = 2.65V$, LTC1098L	10			μs
t_{suDI}	Setup Time, D_{IN} Stable Before $CLK\uparrow$	$V_{CC} = 2.65V$	1			μs
t_{WHCLK}	CLK High Time	$V_{CC} = 2.65V$	1.6			μs
t_{WLCLK}	CLK Low Time	$V_{CC} = 2.65V$	1.6			μs
$t_{WH\overline{CS}}$	\overline{CS} High Time Between Data Transfer Cycles	$V_{CC} = 2.65V$	2			μs
$t_{WL\overline{CS}}$	\overline{CS} Low Time During Data Transfer	LTC1096L, $f_{CLK} = 250kHz$	56			μs
		LTC1098L, $f_{CLK} = 250kHz$	56			μs

CONVERTER AND MULTIPLEXER CHARACTERISTICS $V_{CC} = 2.65V$, $V_{REF} = 2.5V$, $f_{CLK} = 250kHz$, unless otherwise noted.

PARAMETER	CONDITIONS	LTC1096LA/LTC1098LA			LTC1096L/LTC1098L			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Resolution (No Missing Code)		●	8		8		Bits	
Offset Error	(Note 4)	●		±0.5		±1	LSB	
Linearity Error		●		±0.5		±1	LSB	
Full Scale Error		●		±0.5		±1	LSB	
Total Unadjusted Error (Note 5)	$V_{REF} = 2.5V$	●		±1		±1.5	LSB	
Analog Input Range	(Note 6)		-0.05V to $V_{CC} + 0.05V$				V	
REF Input Range (Note 6)	$2.65 \leq V_{CC} \leq 4.0V$		-0.05V to $V_{CC} + 0.05V$				V	
Analog Input Leakage Current	(Note 7)	●		±1		±1	μA	

DIGITAL AND DC ELECTRICAL CHARACTERISTICS $V_{CC} = 2.65V$, $V_{REF} = 2.5V$, $f_{CLK} = 250kHz$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
V_{IH}	High Level Input Voltage	$V_{CC} = 3.6V$	●	1.9		V	
V_{IL}	Low Level Input Voltage	$V_{CC} = 2.65V$	●		0.45	V	
I_{IH}	High Level Input Current	$V_{IN} = V_{CC}$	●		2.5	μA	
I_{IL}	Low Level Input Current	$V_{IN} = 0V$	●		-2.5	μA	
V_{OH}	High Level Output Voltage	$V_{CC} = 2.65V$, $I_O = 10\mu A$ $I_O = 360\mu A$	●	2.4	2.64	V	
			●	2.1	2.50	V	
V_{OL}	Low Level Output Voltage	$V_{CC} = 2.65V$, $I_O = 400\mu A$	●		0.3	V	
I_{OZ}	Hi-Z Output Leakage	$\overline{CS} = High$	●		±3	μA	
I_{SOURCE}	Output Source Current	$V_{OUT} = 0V$		-10		mA	
I_{SINK}	Output Sink Current	$V_{OUT} = V_{CC}$		15		mA	
I_{REF}	Reference Current	$\overline{CS} = V_{CC}$ $t_{CYC} \geq 200\mu s$, $f_{CLK} \leq 50kHz$ $t_{CYC} = 58\mu s$, $f_{CLK} = 250kHz$	●	0.001	2.5	μA	
			●		3.500	7.5	μA
			●		35.00	50.0	μA
I_{CC}	Supply Current	$\overline{CS} = V_{CC}$	●	0.001	± 3	μA	
			LTC1096L, $t_{CYC} \geq 200\mu s$, $f_{CLK} \leq 50kHz$ $t_{CYC} = 58\mu s$, $f_{CLK} = 250kHz$	●	40	80	μA
				●	120	180	μA
			LTC1098L, $t_{CYC} \geq 200\mu s$, $f_{CLK} \leq 50kHz$ $t_{CYC} = 58\mu s$, $f_{CLK} = 250kHz$	●	44	88	μA
●	155	230		μA			

LTC1096L/LTC1098L

AC CHARACTERISTICS

$V_{CC} = 2.65V$, $V_{REF} = 2.5V$, $f_{CLK} = 250kHz$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{SMPL}	Analog Input Sample Time	See Operating Sequences		1.5		CLK Cycles
$f_{SMPL(MAX)}$	Maximum Sampling Frequency		●	16.5		kHz
t_{CONV}	Conversion Time	See Operating Sequences		8		CLK Cycles
t_{dDO}	Delay Time, $CLK\downarrow$ to D_{OUT} Data Valid	See Test Circuits	●	500	1000	ns
t_{dis}	Delay Time, $\overline{CS}\uparrow$ to D_{OUT} Hi-Z	See Test Circuits	●	220	800	ns
t_{en}	Delay Time, $CLK\downarrow$ to D_{OUT} Enable	See Test Circuits	●	160	480	ns
t_{hDO}	Time Output Data Remains Valid After $CLK\downarrow$	$C_{LOAD} = 100pF$		400		ns
t_f	D_{OUT} Fall Time	See Test Circuits	●	70	250	ns
t_r	D_{OUT} Rise Time	See Test Circuits	●	50	200	ns
C_{IN}	Input Capacitance	Analog Inputs		25		pF
		On Channel Off Channel		5		pF
		Digital Input		5		pF

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to GND.

Note 3: This device is specified at 2.65V. Consult factory for 5V specified devices.

Note 4: Linearity error is specified between the actual end points of the A/D transfer curve.

Note 5: Total unadjusted error includes offset, full scale, linearity, multiplexer and hold step errors.

Note 6: Two on-chip diodes are tied to each reference and analog input which will conduct for reference or analog input voltages one diode below GND or one diode drop above V_{CC} . This spec allows 50mV forward bias of either diode for $2.65V \leq V_{CC} \leq 3.6V$. This means that as long as the reference or analog input does not exceed the supply voltage by more than 50mV, the output code will be correct. To achieve an absolute 0V to 3V input voltage range will therefore require a minimum supply voltage of 2.950V over initial tolerance, temperature variations and loading.

Note 7: Channel leakage current is measured after the channel selection.

PIN FUNCTIONS

LTC1096L

$\overline{CS}/SHDN$ (Pin 1): Chip Select Input. A logic low on this input enables the LTC1096L. A logic high on this input disables the LTC1096L and disconnects the power to the LTC1096L.

IN^+ (Pin 2): Analog Input. This input must be free of noise with respect to GND.

IN^- (Pin 3): Analog Input. This input must be free of noise with respect to GND.

GND (Pin 4): Analog Ground. GND should be tied directly to an analog ground plane.

V_{REF} (Pin 5): Reference Input. The reference input defines the span of the A/D converter and must be kept free of noise with respect to GND.

D_{OUT} (Pin 6): Digital Data Output. The A/D conversion result is shifted out of this output.

CLK (Pin 7): Shift Clock. This clock synchronizes the serial data transfer.

V_{CC} (Pin 8): Power Supply Voltage. This pin provides power to the A/D converter. It must be free of noise and ripple by bypassing directly to the analog ground plane.

LTC1098L

$\overline{CS}/SHDN$ (Pin 1): Chip Select Input. A logic low on this input enables the LTC1098L. A logic high on this input disables the LTC1098L and disconnects the power to the LTC1098L.

CHO (Pin 2): Analog Input. This input must be free of noise with respect to GND.

PIN FUNCTIONS

CH1 (Pin 3): Analog Input. This input must be free of noise with respect to GND.

GND (Pin 4): Analog Ground. GND should be tied directly to an analog ground plane.

D_{IN} (Pin 5): Digital Data Input. The multiplexer address is shifted into this pin.

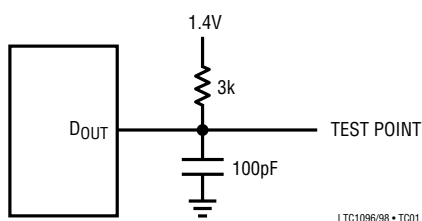
D_{OUT} (Pin 6): Digital Data Output. The A/D conversion result is shifted out of this output.

CLK (Pin 7): Shift Clock. This clock synchronizes the serial data transfer.

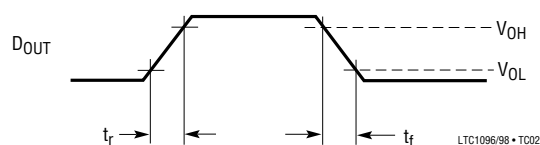
V_{CC} (V_{REF}) (Pin 8): Power Supply Voltage. This pin provides power and defines the span of the A/D converter. It must be free of noise and ripple by bypassing directly to the analog ground plane

TEST CIRCUITS

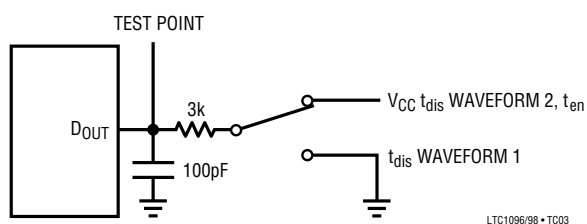
Load Circuit for t_{dDO} , t_r and t_f



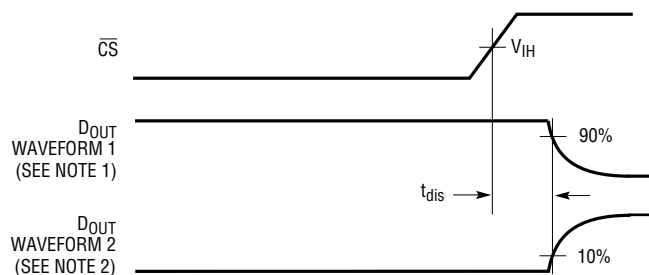
Voltage Waveforms for D_{OUT} Rise and Fall Times, t_r , t_f



Load Circuit for t_{dis} and t_{en}



Voltage Waveforms for t_{dis}

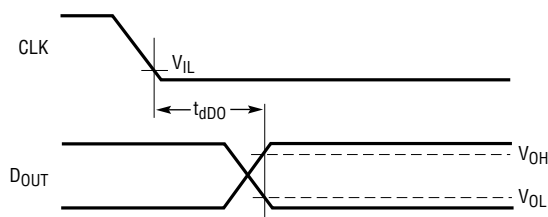


NOTE 1: WAVEFORM 1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH UNLESS DISABLED BY THE OUTPUT CONTROL.

NOTE 2: WAVEFORM 2 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW UNLESS DISABLED BY THE OUTPUT CONTROL.

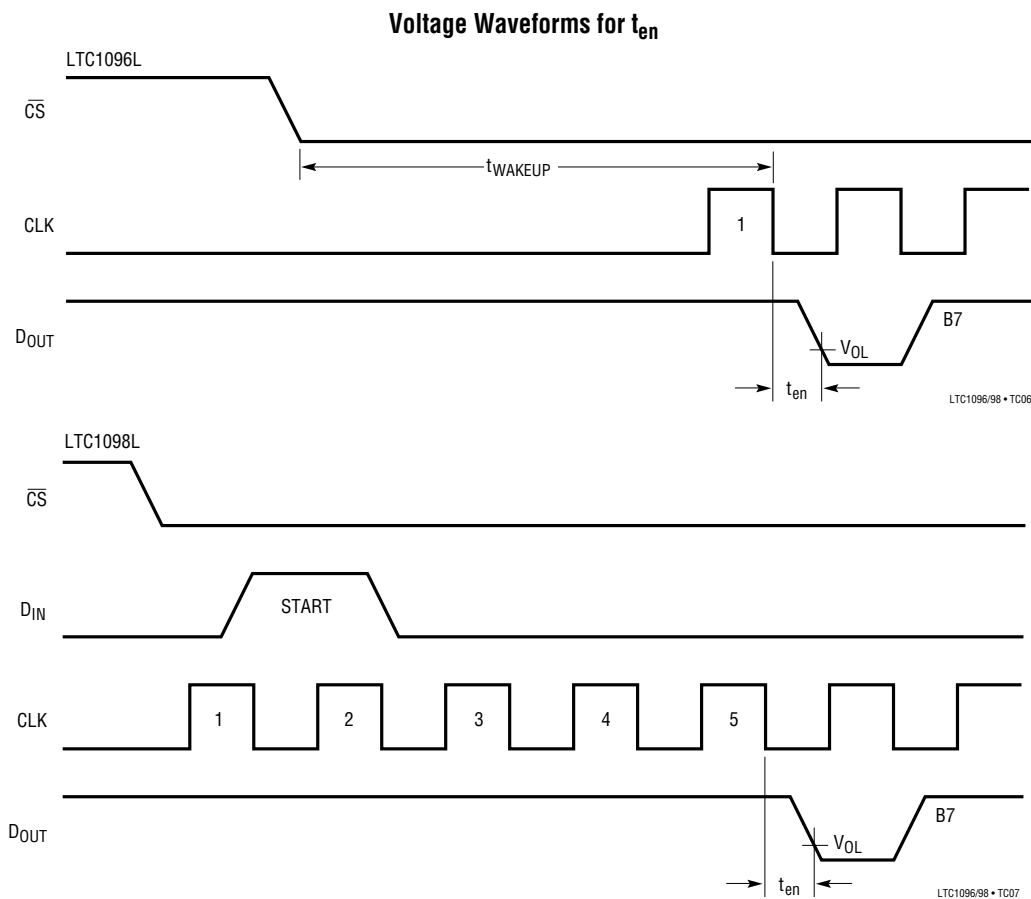
LTC1096/98 • TC04

Voltage Waveforms for D_{OUT} Delay Time, t_{dDO}



LTC1096/98 • TC05

TEST CIRCUITS

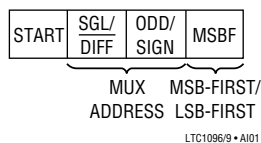


APPLICATIONS INFORMATION

INPUT DATA WORD

The LTC1096L requires no D_{IN} word. It is permanently configured to have a single differential input. The conversion result, in which the output on the D_{OUT} line is presented in MSB-first sequence followed by LSB sequence, provides easy interface to MSB- or LSB-first serial ports.

The LTC1098L latches data into the D_{IN} input on the rising edge of the clock. The input data words are defined as follows:



Start Bit

The first “logical one” clocked into the D_{IN} input after \overline{CS} goes low is the start bit. The start bit initiates the data transfer. The LTC1098L will ignore all leading zeroes which precede this logical one. After the start bit is received, the remaining bits of the input word will be clocked in. Further inputs on the D_{IN} pin are then ignored until the next \overline{CS} cycle.

Multiplexer (MUX) Address

The bits of the input word following the START bit assign the MUX configuration for the requested conversion. For a given channel selection, the converter will measure the voltage between the two channels indicated by the “+” and “-” signs in the selected row of the following tables. In

APPLICATIONS INFORMATION

single-ended mode, all input channels are measured with respect to GND.

LTC1098L Channel Selection

MUX ADDRESS		CHANNEL #		
SGL/DIFF	ODD/SIGN	CH0	CH1	GND
1	0	+		-
1	1		+	-
0	0	+	-	
0	1	-	+	

LTC1096/8 • A102

MSB-First/LSB-First (MSBF)

The output data of the LTC1098L is programmed for MSB-first or LSB-first sequence using the MSBF bit. When the MSBF bit is a logical one, data will appear on the D_{OUT} line in MSB-first format. Logical zeroes will be filled in indefinitely following the last data bit. When the MSBF bit is a logical zero, LSB-first data will follow the normal MSB-first data on the D_{OUT} line (see Figures 1 and 2).

ANALOG CONSIDERATIONS

Grounding

The LTC1096L/LTC1098L should be used with an analog ground plane and single point grounding techniques. Do

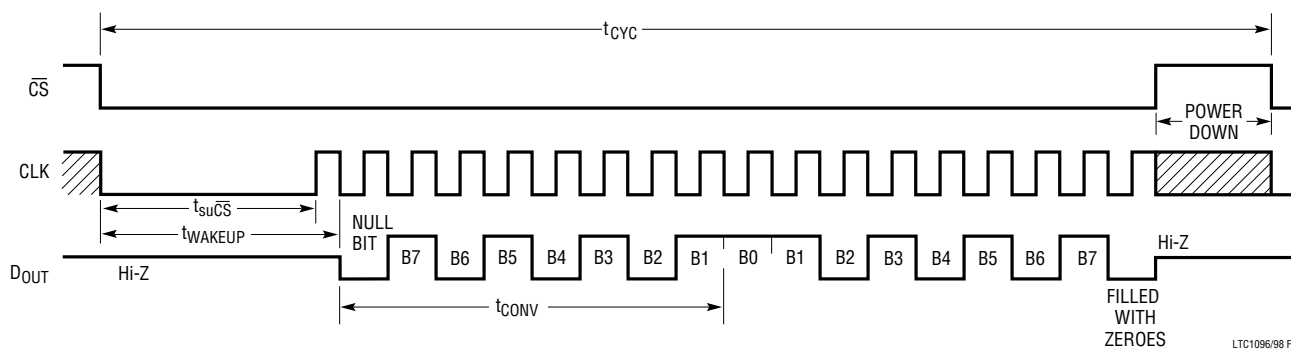
not use wire wrapping techniques to breadboard and evaluate the device. To achieve the optimum performance use a printed circuit board. The GND pin (Pin 4) should be tied directly to the ground plane with minimum lead length.

Bypassing

For good performance, the LTC1096L/LTC1098L V_{CC} and V_{REF} pins must be free of noise and ripple. Any changes in the V_{CC} and V_{REF} voltage with respect to ground during the conversion cycle can induce errors or noise in the output code. Bypass the V_{CC} and V_{REF} pins directly to the analog ground plane with a minimum $0.1\mu\text{F}$ capacitor and with leads as short as possible. The LTC1098L combines V_{CC} and V_{REF} into one pin, $V_{CC}(V_{REF})$, which can be bypassed by a $0.1\mu\text{F}$ capacitor.

Analog Inputs

Because of the capacitive redistribution A/D conversion techniques used, the analog inputs of the LTC1096L/LTC1098L have capacitive switching input current spikes. These current spikes settle quickly and do not cause a problem. But if large source resistances are used or if slow settling op amps drive the inputs, take care to ensure the transients caused by the current spikes settle completely before the conversion begins.



LTC1096/88 F01

Figure 1. LTC1096L Operating Sequence

LTC1096L/LTC1098L

APPLICATIONS INFORMATION

MSB-FIRST DATA (MSBF = 0)

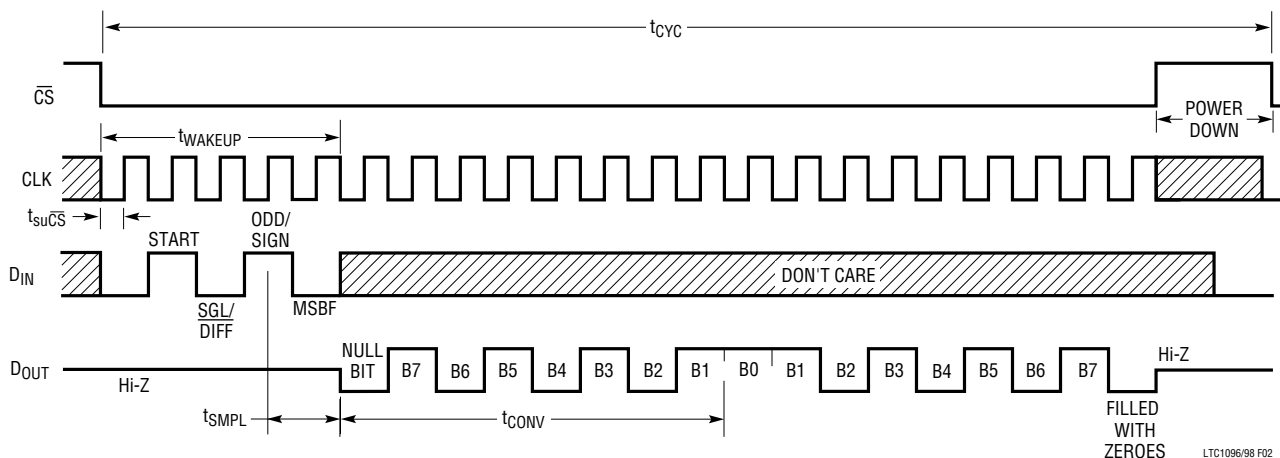
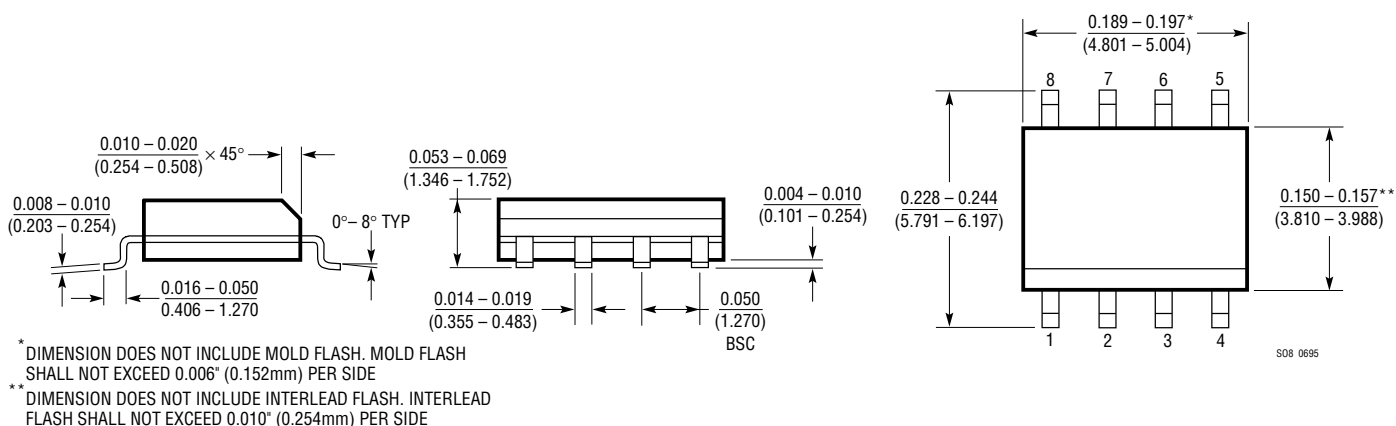


Figure 2. LTC1098L Operating Sequence Example: Differential Inputs (CH^+ , CH^-)

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

S8 Package 8-Lead Plastic Small Outline (Narrow 0.150) (LTC DWG # 05-08-1610)



* DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1096/LTC1098	8-Pin SO, Micropower 8-Bit ADC	Low Power, Small Size, Low Cost
LTC1196/LTC1198	8-Pin SO, 1Msps 8-Bit ADC	Low Power, Small Size, Low Cost
LTC1285/LTC1288	8-Pin SO, 3V Micropower 12-Bit ADC	12-Bit ADC in SO-8
LTC1289	Multiplexed 3V 12-Bit ADC	8-Channel 12-Bit Serial I/O
LTC1584L	Multiplexed 3V 12-Bit ADC	4-Channel 12-Bit Serial I/O, Micropower