Document Title

1M x 16Bit x 4 Banks (64-MBIT) SDRAM

Revision History

Revision No	History	Draft Date	Remark
0A	Initial Draft	Demcember 20,2001	
0B	Revise DC OPERATING CONDITIONS	April 15,2002	
0C	1. add -6ns speed grade 2. obsolete 8Mx8 configuration 3. obsolete Low power version 4. obsolete -8ns speed grade	Novembver 22,2002	
0D	Add 60 ball(64M SDRAM) VF-BGA package	September 05,2003	
0E	Add Pb-free package	December 02,2003	

1M x 16 Bits x 4 Banks (64-MBIT) SYNCHRONOUS DYNAMIC RAM

FEATURES

- Single 3.3V (± 0.3V) power supply
- High speed clock cycle time -6: 166MHz, -7: 133MHz<3-3-3>
- Fully synchronous operation referenced to clock rising edge
- Possible to assert random column access in every cycle
- Quad internal banks contorlled by A12 & A13 (Bank Select)
- Byte control by LDQM and UDQM for IC42S16400
- Programmable Wrap sequence (Sequential / Interleave)
- Programmable burst length (1, 2, 4, 8 and full page)
- Programmable $\overline{\text{CAS}}$ latency (2 and 3)
- Automatic precharge and controlled precharge
- CBR (Auto) refresh and self refresh
- LVTTL compatible inputs and outputs
- 4,096 refresh cycles / 64ms
- Burst termination by Burst stop and Precharge command
- Package 400mil 54-pin TSOP-2 and 60ball(64M) VF-BGA
- Pb(lead)-free package is available

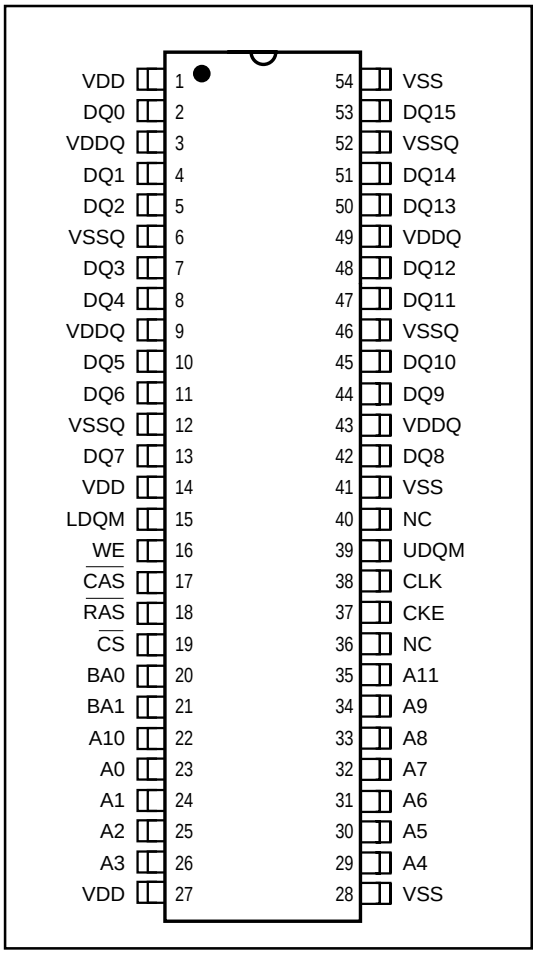
DESCRIPTION

The IC42S16400 are high-speed 67,108,864-bit synchronous dynamic random-access memories, organized as 1,048,576 x 16 x 4 (word x bit x bank), respectively.

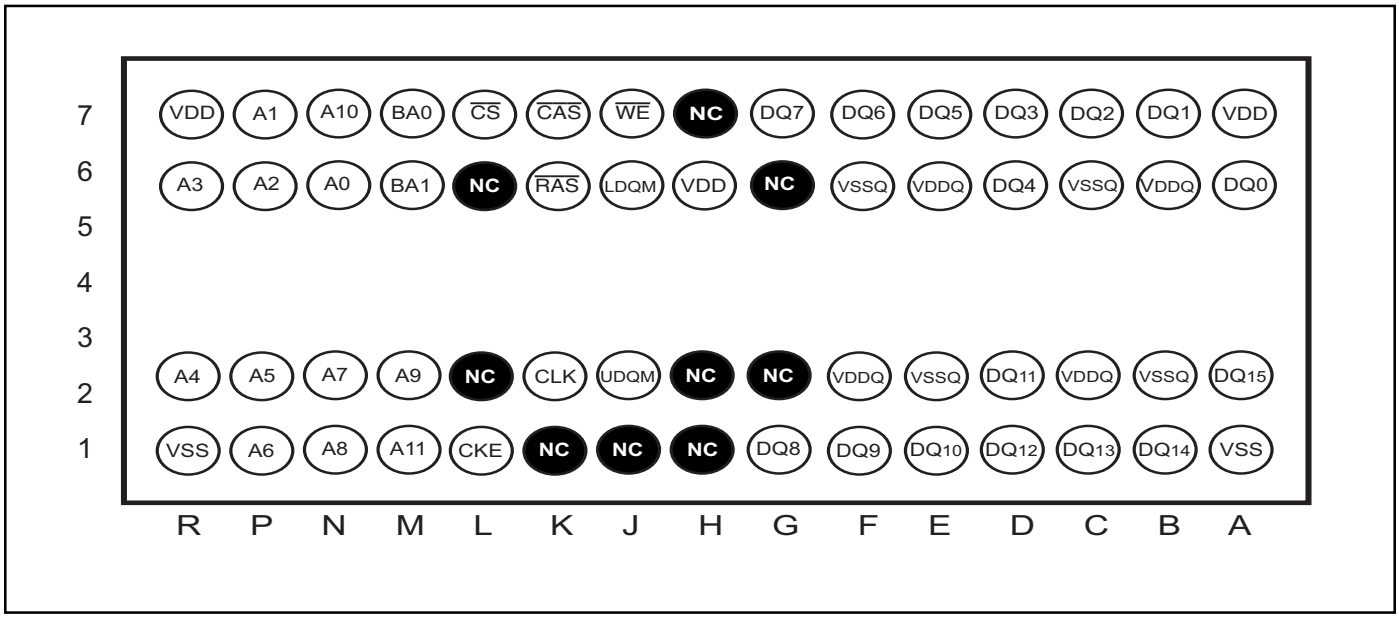
The synchronous DRAMs achieved high-speed data transfer using the pipeline architecture and clock frequency up to 166MHz for -6. All input and outputs are synchronized with the positive edge of the clock.The synchronous DRAMs are compatible with Low Voltage TTL (LVTTL).These products are packaged in 54-pin TSOP-2 and 60ball(64M) VF-BGA.

PIN CONFIGURATIONS

54-Pin TSOP-2



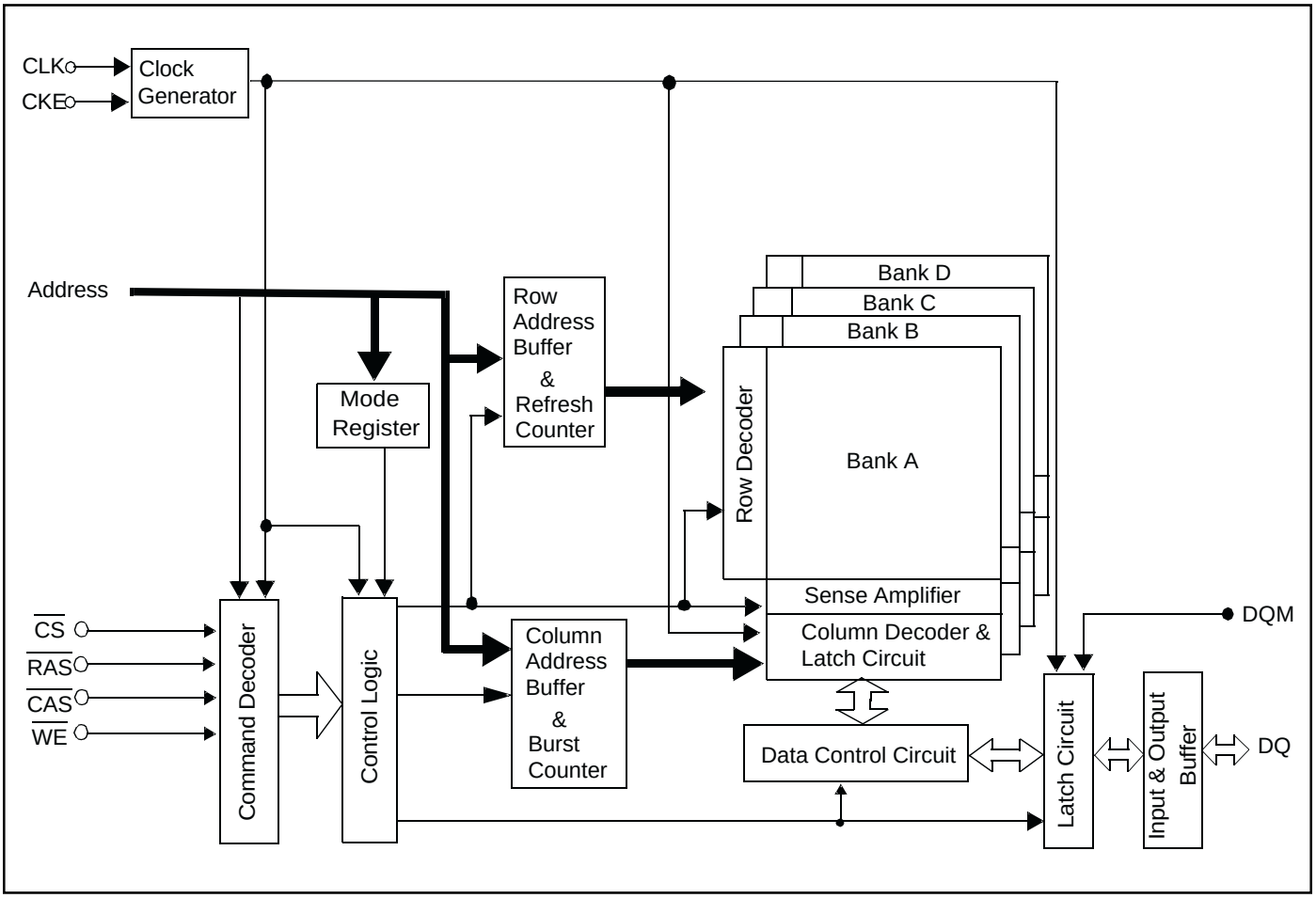
60-BALL VF-BGA (64M SDRAM)



PIN DESCRIPTIONS

A0 - A11	Address	Row Address : RA0 - RA11, Column Address : CA0 - CA7 Auto-precharge flag : A10
BA0,BA1	Bank Address	Selects bank to be activated during $\overline{RAS}$ activity Selects bank to be read/written during $\overline{CAS}$ activity
DQ0 - DQ15	Data Input/Output	Multiplexed data input / output pin
CLK	Clock	The system clock input.All other inputs are registered to the SDRAM on the rising edge of CLK
CKE	Clock Enable	Controls internal clock signal and when deactivated,the SDRAM will be one of the states among power down,suspend or self refresh
$\overline{CS}$	Chip Select	Enables or disables all inputs except CLK, CKE and DQM
$\overline{RAS}$	Row Address Strobe	$\overline{RAS}$,$\overline{CAS}$ and $\overline{WE}$ define the operation
$\overline{CAS}$	Column Address Strobe	Refer function truth table for details
$\overline{WE}$	Write Enable	
LDQM,UDQM	Data Input/Output Mask	Controls output buffers in read mode and masks input data in write mode
V_{DD}/V_{SS}	Power Supply/Ground	Power supply for internal circuits and input buffers
$V_{DD}Q/V_{SS}Q$	Data Output Power/Ground	Power supply for output buffers
NC	No Connection	No Connection

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameters	Rating	Unit
V_{DD}	Supply Voltage (with respect to V_{SS})	–0.5 to +4.6	V
V_{DDQ}	Supply Voltage for Output (with respect to V_{SSQ})	–0.5 to +4.6	V
V_I	Input Voltage (with respect to V_{SS})	–0.5 to V_{DD}+0.5	V
V_O	Output Voltage (with respect to V_{SSQ})	–1.0 to V_{DDQ}+0.5	V
I_O	Short circuit output current	50	mA
P_D	Power Dissipation (T_A = 25 °C)	1	W
T_{OPT}	Operating Temperature	0 to +70	°C
T_{STG}	Storage Temperature	–65 to +150	°C

Notes:
1. Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

DC RECOMMENDED OPERATING CONDITIONS

(At T_A = 0 to +70°C unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	3.0	3.3	3.6	V
V_{DDQ}	Supply Voltage for DQ	3.0	3.3	3.6	V
V_{IH}	High Level Input Voltage (all Inputs)	2.0	—	V_{DD} + 0.3	V
V_{IL}	Low Level Input Voltage (all Inputs)	-0.3	—	+0.8	V

CAPACITANCE CHARACTERISTICS

(At T_A = 0 ~ 70°C, V_{DD} = V_{DDQ} = 3.3 ± 0.3V, V_{SS} = V_{SSQ} = 0V , unless otherwise noted)

Symbol	Parameter	Min.	Max.	Unit
C_{IN}	Input Capacitance, address & control pin	2.5	3.8	pF
C_{CLK}	Input Capacitance, CLK pin	2.5	3.5	pF
$C_{I/O}$	Data Input/Output Capacitance	4.0	6.5	pF

DC ELECTRICAL CHARACTERISTICS

(At T_A = 0 ~ 70°C, V_{DD} = V_{DDQ} = 3.3 ± 0.3V, V_{SS} = V_{SSQ} = 0V , unless otherwise noted)

Symbol	Parameter	Test Condition		Speed	Min.	Max.	Unit
I_{CC1}(1)	Operating Current	One Bank active, Burst Length=1 t_{RC} = t_{RC} (min.) t_{CLK} = t_{CLK} (min.)	$\overline{CAS}$ latency = 3	-6(42S16400) -7(42S16400)	— —	95 85	mA mA
I_{CC2P}	Precharge Standby Current (In Power-Down Mode)	CKE < V_{IL} (MAX)	t_{CK} = 15 ns	-6 -7	— —	2 2	mA mA
I_{CC2PS}		CKE < V_{IL} (MAX)	CLK < V_{IL} (MAX)	-6 -7	— —	1 1	mA mA
I_{CC2N}(2)	Precharge Standby Current (In Non Power-Down Mode)	CS > V_{CC} -0.2V CKE > V_{IH} (MIN)	t_{CK} = 15 ns	-6 -7	— —	20 20	mA mA
I_{CC2NS}		CS > V_{CC} -0.2V CKE > V_{IH} (MIN)	CKE < V_{IL} (MAX) All input signals are stable.	-6 -7	— —	15 15	mA mA
I_{CC3P}	Active Standby Current (In Power-Down Mode)	CKE < V_{IL} (MAX)	t_{CK} = 10 ns	-6 -7	— —	7 7	mA mA
I_{CC3PS}		CKE < V_{IL} (MAX)	CLK < V_{IL} (MAX)	-6 -7	— —	5 5	mA mA
I_{CC3N}(2)	Active Standby Current (In Non Power-Down Mode)	CS > V_{CC} -0.2V CKE > V_{IH} (MIN)	t_{CK} = 15 ns	-6 -7	— —	30 30	mA mA
I_{CC3NS}		CS > V_{CC} -0.2V CKE > V_{IH} (MIN)	CKE < V_{IL} (MAX) All input signals are stable.	-6 -7	— —	25 25	mA mA
I_{CC4}	Operating Current (In Burst Mode)	All Banks active Burst Length=1 t_{CK} = t_{CK} (MIN)	$\overline{CAS}$ latency = 3	-6(42S16400) -7(42S16400)	— —	130 100	mA mA
I_{CC5}	Auto-Refresh Current	t_{RC} = t_{RC} (MIN) t_{CLK} = t_{CLK} (MIN)		-6 -7	— —	150 130	mA mA
I_{CC6}(3, 4)	Self-Refresh Current	CKE < 0.2V		-6 -7	— —	1 1	mA mA
I_{IL}	Input Leakage Current (Inputs)	0V < V_{IN} < V_{DD} (MAX) Pins not under test = 0V			–5	5	µA
I_{OL}	Output Leakage Current (I/O pins)	Output is disabled DQ# in H - Z., 0V < V_{OUT} < V_{DD} (MAX)			–5	5	µA
V_{OH}	High Level Output Voltage	I_{OUT} = –2 mA			2.4	—	V
V_{OL}	Low Level Output Voltage	I_{OUT} = +2 mA			—	0.4	V

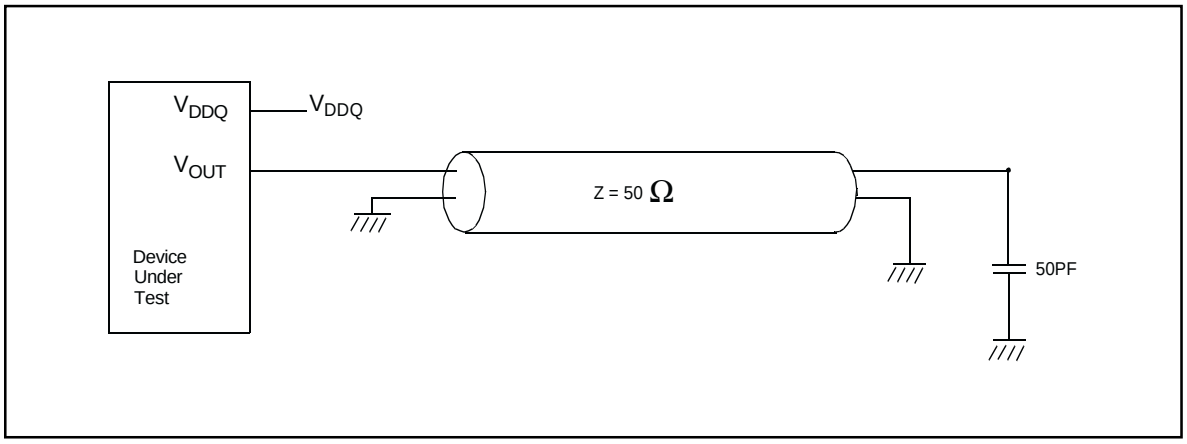
Notes:
1. I_{CC}(max) is specified at the output open condition.
2. Input signals are changed one time during 30ns.

AC TEST CONDITIONS

(At T_A = 0 ~ 70°C, V_{DD} = V_{DDQ} = 3.3 ± 0.3V, V_{SS} = V_{SSQ} = 0V , unless otherwise noted)

Parameter	Rating	Unit
AC input Levels (V_{IH} /V_{IL})	2.0 / 0.8	V
Input timing reference level /Output timing reference level	1.4	V
Input rise and fall time	1	ns
Output load condition	50	pF

Output Load Conditions



AC ELECTRICAL CHARACTERISTICS

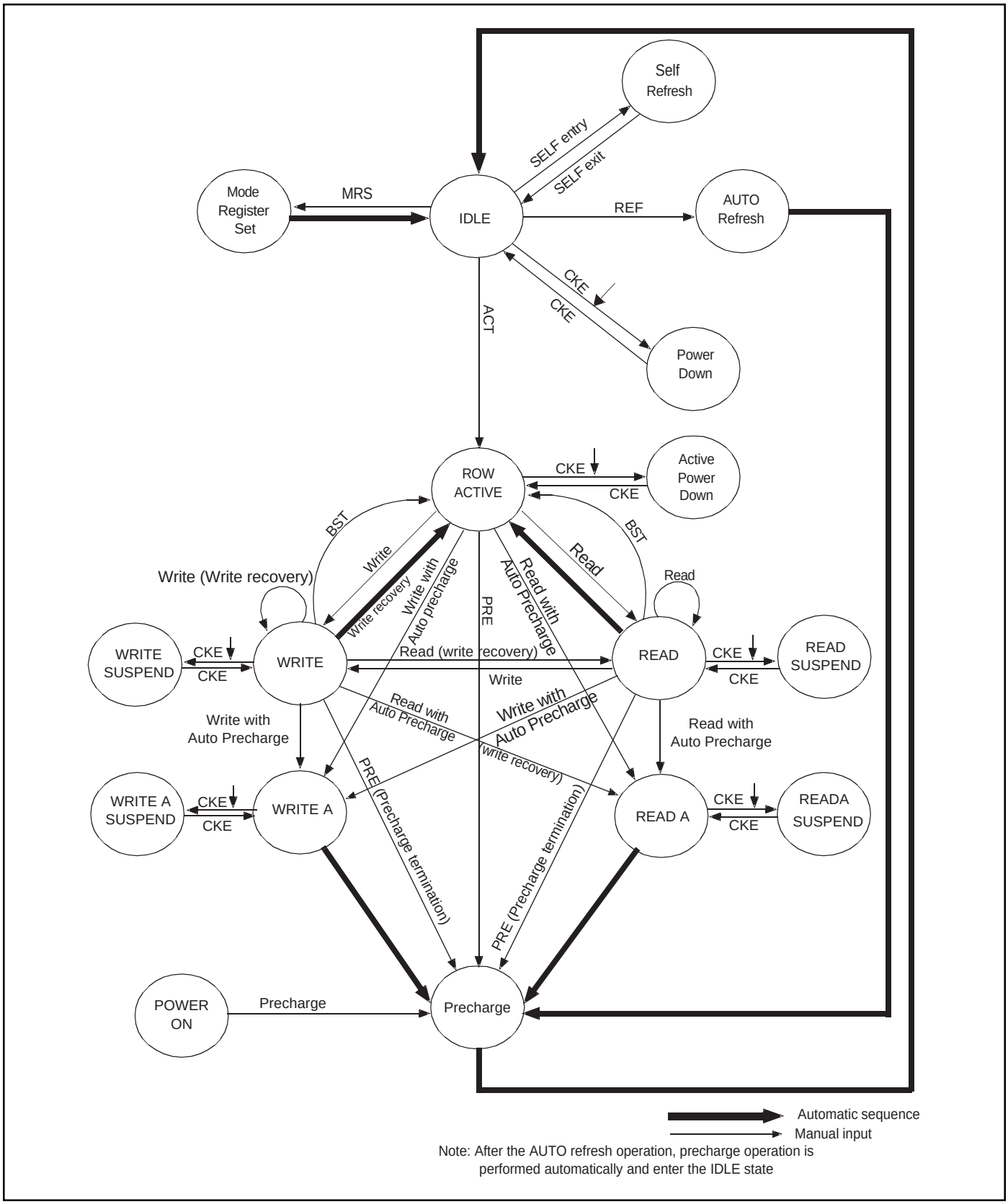
(At T_A = 0 ~ 70°C, V_{DD} = V_{DDQ} = 3.3 ± 0.3V, V_{SS} = V_{SSQ} = 0V , unless otherwise noted)

Symbol	Parameter		-6		-7		Units
			Min.	Max.	Min.	Max.	
$t_{CK}3$	CLK Cycle Time	$\overline{CAS}$ Latency = 3	6	—	7.5	—	ns
$t_{CK}2$		$\overline{CAS}$ Latency = 2	7.5	—	10	—	ns
$t_{AC}3$	CLK to valid output delay(1)	$\overline{CAS}$ Latency = 3	—	5	—	5.4	ns
$t_{AC}2$		$\overline{CAS}$ Latency = 2	—	6	—	6	ns
t_{CH}	CLK high pulse width		2.5	—	2.5	—	ns
t_{CL}	CLK low pulse width		2.5	—	2.5	—	ns
t_{CKE}	CKE setup time		1.5	—	1.5	—	ns
t_{CKH}	CKE hold time		0.8	—	0.8	—	ns
t_{AS}	Address setup time		1.5	—	1.5	—	ns
t_{AH}	Address hold time		0.8	—	0.8	—	ns
t_{CMS}	Command setup time		1.5	—	1.5	—	ns
t_{CMH}	Command hold time		0.8	—	0.8	—	ns
t_{DS}	Data input setup time		1.5	—	1.5	—	ns
t_{DH}	Data input hold time		0.8	—	0.8	—	ns
$t_{OH}3$	Output data hold time(1)	$\overline{CAS}$ Latency = 3	2.5	—	2.7	—	ns
$t_{OH}2$		$\overline{CAS}$ Latency = 2	2.5	—	3	—	ns
t_{LZ}	CLK to output in low - Z		0	—	0	—	ns
t_{HZ}	CLK to output in H - Z		2.5	5	2.7	5.4	ns
t_{RC}	ROW cycle time		60	—	67.5	—	ns
t_{RAS}	ROW active time		42	100,000	45	100,000	ns
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay		18	—	20	—	ns
t_{RP}	Row precharge time		15	—	20	—	ns
t_{RRD}	Row active to active delay		12	—	15	—	ns
t_{DPL}	Data in to precharge		12	—	15	—	ns
t_T	Transition time		1	10	1	10	ns
t_{RSC}	Mode reg. set cycle		10	—	10	—	ns
t_{PDE}	Power down exit setup time		7.5	—	7.5	—	ns
t_{SRX}	Self refresh exit time		7.5	—	7.5	—	ns
t_{REF}	Refresh Time		—	64	—	64	ms

Notes:
1. if clock rising time is longer than 1ns, (tr/2-0.5ns) should be added to the parameter.

Basic Features and Function Description

Simplified State Diagram



Note: After the AUTO refresh operation, precharge operation is performed automatically and enter the IDLE state

COMMAND TRUTH TABLE

Symbol	Command	CKE n-1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	A10	A11 A9-A0
DESL	Device deselect	H	X	H	X	X	X	X	X	X
NOP	No operation	H	X	L	H	H	H	X	X	X
MRS	Mode register set	H	X	L	L	L	L	L	L	V
ACT	Bank activate	H	X	L	L	H	H	V	V	V
READ	Read	H	X	L	H	L	H	V	L	V
READA	Read with auto precharge	H	X	L	H	L	H	V	H	V
WRIT	Write	H	X	L	H	L	L	V	L	V
WRITA	Write with auto precharge	H	X	L	H	L	L	V	H	V
PRE	Precharge select bank	H	X	L	L	H	L	V	L	X
PALL	Precharge all banks	H	X	L	L	H	L	X	H	X
BST	Burst stop	H	X	L	H	H	L	X	X	X
REF	CBR (Auto) refresh	H	H	L	L	L	H	X	X	X
SELF	Self refresh	H	L	L	L	L	H	X	X	X

Notes:
H : High level
X : High or Low level (Don't care)
L : Low level
V : Valid Data input

DQM TRUTH TABLE

Symbol	Command	CKE n-1	CKE n	DQM
ENB	Data Write / Output Enable	H	X	L
MASK	Data Mask / Output Disable	H	X	H

CKE TRUTH TABLE

Symbol	Command	Current State	CKE n-1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addreess
—	Clock suspend mode entry	Activating	H	L	X	X	X	X	X
—	Clock suspend	Any	L	L	X	X	X	X	X
—	Clock suspend mode exit	Clock suspend	L	H	X	X	X	X	X
REF	CBR refresh command	Idle	H	H	L	L	L	H	X
SELF	Self refresh entry	Idle	H	L	L	L	L	H	X
—	Self refresh exit	Self refresh	L	H	L	H	H	H	X
			L	H	H	X	X	X	X
—	Power down entry	Idle	H	L	X	X	X	X	X
—	Power down exit	Power down	L	H	X	X	X	X	X

OPERATION COMMAND TABLE(1)

Current State	Command	Operation	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address
Idle	DESL	NOP or Power-Down(2)	H	X	X	X	X
	NOP or BST	NOP or Power-Down(2)	L	H	H	X	X
	READ / READA	Illegal(3)	L	H	L	H	BA, CA, A10
	WRIT/WRITA	Illegal(3)	L	H	L	L	BA, CA, A10
	ACT	Row Active	L	L	H	H	BR, RA
	PRE/PALL	NOP	L	L	H	L	BA, A10
	REF/SELF	Refresh or Self-Refresh(4)	L	L	L	H	X
	MRS	Mode Register Set	L	L	L	L	Op-Code
Row Active	DESL	NOP	H	X	X	X	X
	NOP or BST	NOP	L	H	H	H	X
	READ/READA	Begin read : Determine AP(5)	L	H	L	H	BA, CA, A10
	WRIT/WRITA	Begin write : Determine AP(5)	L	H	L	L	BA, CA, A10
	ACT	Illegal(3)	L	L	H	H	BR, RA
	PRE/PALL	Precharge(6)	L	L	H	L	BA, A10
	REF/SELF	Illegal	L	L	L	H	X
	MRS	Illegal	L	L	L	L	Op-Code
Read	DESL	Continue burst to end -> Row active	H	X	X	X	X
	NOP	Continue burst to end -> Row active	L	H	H	H	X
	BST	Burst stop -> Row active	L	H	H	L	X
	READ/READA	Term burst, new read : Determine AP(7)	L	H	L	H	BA, CA, A10
	WRIT/WRITA	Term burst, start write : Determine AP(7, 8)	L	H	L	L	BA, CA, A10
	ACT	Illegal(3)	L	L	H	H	BR, RA
	PRE/PALL	Term burst, precharging	L	L	H	L	BA, A10
	REF/SELF	Illegal	L	L	L	H	X
	MRS	Illegal	L	L	L	L	Op-Code
Write	DESL	Continue burst to end -> write recovering	H	X	X	X	X
	NOP	Continue burst to end -> write recovering	L	H	H	H	X
	BST	Burst stop -> Row active	L	H	H	L	X
	READ/READA	Term burst, start read : Determine AP(7, 8)	L	H	L	H	BA, CA, A10
	WRIT/WRITA	Term burst, new write : Determine AP(7)	L	H	L	L	BA, CA, A10
	ACT	Illegal(3)	L	L	H	H	BR, RA
	PRE/PALL	Term burst, precharging(9)	L	L	H	L	BA, A10
	REF/SELF	Illegal	L	L	L	H	X
	MRS	Illegal	L	L	L	L	Op-Code
Read With Auto-Precharge	DESL	Continue burst to end -> Precharging	H	X	X	X	X
	NOP	Continue burst to end -> Precharging	L	H	H	H	X
	BST	Illegal	L	H	H	L	X
	READ/READA	Illegal(11)	L	H	L	H	BA, CA, A10
	WRIT/WRITA	Illegal(11)	L	H	L	L	BA, CA, A10
	ACT	Illegal(3)	L	L	H	H	BR, RA
	PRE/PALL	Illegal(11)	L	L	H	L	BA, A10
	REF/SELF	Illegal	L	L	L	H	X
	MRS	Illegal	L	L	L	L	Op-Code

OPERATION COMMAND TABLE(continue)

Current State	Command	Operation	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address
Write with auto	DESL	Continue burst to end -> write recovering with auto precharge	H	X	X	X	X
precharge	NOP	Continue burst to end -> write recovering with auto precharge	L	H	H	H	X
	BST	Illegal	L	H	H	L	X
	READ / READA	Illegal(11)	L	H	L	H	BA, CA, A10
	WRIT/WRITA	Illegal(11)	L	H	L	L	BA, CA, A10
	ACT	Illegal(3, 11)	L	L	H	H	BR, RA
	PRE/PALL	Illegal(3, 11)	L	L	H	L	BA, A10
	REF/SELF	Illegal	L	L	L	H	X
	MRS	Illegal	L	L	L	L	Op-Code
Precharging	DESL	Nop -> Enter idle after t_{RP}	H	X	X	X	X
	NOP	Nop -> Enter idle after t_{RP}	L	H	H	H	X
	BST	Nop -> Enter idle after t_{RP}	L	H	H	L	X
	READ/READA	Illegal(3)	L	H	L	H	BA, CA, A10
	WRIT/WRITA	Illegal(3)	L	H	L	L	BA, CA, A10
	ACT	Illegal(3)	L	L	H	H	BR, RA
	PRE/PALL	Nop -> Enter idle after t_{RP}	L	L	H	L	BA, A10
	REF/SELF	Illegal	L	L	L	H	X
	MRS	Illegal	L	L	L	L	Op-Code
Row activating	DESL	Nop - > Enter row active after t_{RCD}	H	X	X	X	X
	NOP	Nop - > Enter row active after t_{RCD}	L	H	H	H	X
	BST	Nop - > Enter row active after t_{RCD}	L	H	H	L	X
	READ/READA	Illegal(3)	L	H	L	H	BA, CA, A10
	WRIT/WRITA	Illegal(3)	L	H	L	L	BA, CA, A10
	ACT	Illegal(3, 9)	L	L	H	H	BR, RA
	PRE/PALL	Illegal(3)	L	L	H	L	BA, A10
	REF/SELF	Illegal	L	L	L	H	X
	MRS	Illegal	L	L	L	L	Op-Code
Write	DESL	Nop -> Enter row active after t_{DPL}	H	X	X	X	X
recovering	NOP	Nop -> Enter row active after t_{DPL}	L	H	H	H	X
	BST	Nop -> Enter row active after t_{DPL}	L	H	H	L	X
	READ/READA	Start read, Determine AP(8)	L	H	L	H	BA, CA, A10
	WRIT/WRITA	New write, Determine AP	L	H	L	L	BA, CA, A10
	ACT	Illegal(3)	L	L	H	H	BR, RA
	PRE/PALL	Illegal(3)	L	L	H	L	BA, A10
	REF/SELF	Illegal	L	L	L	H	X
	MRS	Illegal	L	L	L	L	Op-Code

OPERATION COMMAND TABLE(continue)

Current State	Command	Operation	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address
Write	DESL	Nop -> Enter precharge after t_{DPL}	H	X	X	X	X
recovering	NOP	Nop -> Enter precharge after t_{DPL}	L	H	H	H	X
with auto	BST	Nop -> Enter precharge after t_{DPL}	L	H	H	L	X
precharge	READ/READA	Illegal(3 ,8, 11)	L	H	L	H	BA, CA, A10
	WRIT/WRITA	Illegal(3,11)	L	H	L	L	BA, CA, A10
	ACT	Illegal(3, 11)	L	L	H	H	BR, RA
	PRE/PALL	Illegal(3, 11)	L	L	H	L	BA, A10
	REF/SELF	Illegal	L	L	L	H	X
	MRS	Illegal	L	L	L	L	Op-Code
Auto	DESL	Nop Enter idle after t_{RC}	H	X	X	X	X
Refreshing	NOP/BST	Nop Enter idle after t_{RC}	L	H	H	X	X
	READ/WRIT	Illegal	L	H	L	X	X
	ACT/PRE/PALL	Illegal	L	L	H	X	X
	REF/SELF/MRS	Illegal	L	L	L	X	X
Mode	DESL	Nop -> Enter idle after 2 Clocks	H	X	X	X	X
register	NOP	Nop -> Enter idle after 2 Clocks	L	H	H	H	X
setting	BST	Illegal	L	H	H	L	X
	READ/WRIT	Illegal	L	H	L	X	X
	ACT/PRE/PALL/ REF/SELF/MRS	Illegal	L	L	X	X	X

Notes:
1. All entries assume that CKE was active (High level) during the preceding clock cycle.
2. If both banks are idle, and CKE is inactive (Low level), the device will enter Power downmode. All input buffers except CKE will be disabled.
3. Illegal to bank in specified states; Function may be legal in the bank indicated by Bank Address(BA), depending on the state of that bank.
4. If both banks are idle, and CKE is inactive (Low level), the device will enter Self refresh mode. All input buffers except CKE will be disabled.
5. Illegal if t_{RCD} is not satisfied.
6. Illegal if t_{RAS} is not satisfied.
7. Must satisfy burst interrupt condition.
8. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
9. Must mask preceding data which don't satisfy t_{DPL} .
10. Illegal if t_{RRD} is not satisfied.
11. Illegal for single bank, but legal for other banks in multi-bank devices.

CKE RELATED COMMAND TRUTH TABLE(1)

Current State	Operation	CKE n-1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address
Self-Refresh (S.R.)	INVALID, CLK (n - 1)would exit S.R.	H	X	X	X	X	X	X
	Self-Refresh Recovery(2)	L	H	H	X	X	X	X
	Self-Refresh Recovery(2)	L	H	L	H	H	X	X
	Illegal	L	H	L	H	L	X	X
	Illegal	L	H	L	L	X	X	X
	Maintain S.R.	L	L	X	X	X	X	X
Self-Refresh Recovery	Idle After t_{RC}	H	H	H	X	X	X	X
	Idle After t_{RC}	H	H	L	H	H	X	X
	Illegal	H	H	L	H	L	X	X
	Illegal	H	H	L	L	X	X	X
	Begin clock suspend next cycle(5)	H	L	H	X	X	X	X
	Begin clock suspend next cycle(5)	H	L	L	H	H	X	X
	Illegal	H	L	L	H	L	X	X
	Illegal	H	L	L	L	X	X	X
	Exit clock suspend next cycle(2)	L	H	X	X	X	X	X
	Maintain clock suspend	L	L	X	X	X	X	X
Power-Down (P.D.)	INVALID, CLK (n - 1) would exit P.D.	H	X	X	X	X	X	—
	EXIT P.D. -> Idle(2)	L	H	X	X	X	X	X
	Maintain power down mode	L	L	X	X	X	X	X
Both Banks Idle	Refer to operations in Operative Command Table	H	H	H	X	X	X	—
	Refer to operations in Operative Command Table	H	H	L	H	X	X	—
	Refer to operations in Operative Command Table	H	H	L	L	H	X	—
	Auto-Refresh	H	H	L	L	L	H	X
	Refer to operations in Operative Command Table	H	H	L	L	L	L	Op - Code
	Refer to operations in Operative Command Table	H	L	H	X	X	X	—
	Refer to operations in Operative Command Table	H	L	L	H	X	X	—
	Refer to operations in Operative Command Table	H	L	L	L	H	X	—
	Self-Refresh(3)	H	L	L	L	L	H	X
	Refer to operations in Operative Command Table	H	L	L	L	L	L	Op - Code
	Power-Down(3)	L	X	X	X	X	X	X
Any state	Refer to operations in Operative Command Table	H	H	X	X	X	X	X
other than	Begin clock suspend next cycle(4)	H	L	X	X	X	X	X
listed above	Exit clock suspend next cycle	L	H	X	X	X	X	X
	Maintain clock suspend	L	L	X	X	X	X	X

Notes:
1. H : Hight level, L : low level, X : High or low level (Don't care).
2. CKE Low to High transition will re-enable CLK and other inputs asynchronously. A minimum setup time must be satisfied before any command other than EXIT.
3. Power down and Self refresh can be entered only from the both banks idle state.
4. Must be legal command as defined in Operative Command Table.
5. Illegal if t_{SREX} is not satisfied.

Initiallization

Before starting normal operation, the following power on sequence is necessary to prevent SDRAM from damged or malfunctioning.

1. Apply power and start clock. Attempt to maintain CKE high , DQN high and NOP condition at the inputs.
2. Maintain stable power, table clock , and NOP input conditions for a minimum of 200us.
3. Issue precharge commands for all bank. (PRE or PREA)
4. After all banks become idle state (after t_{RP}), issue 8 or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode regiser.

After these sequence, the SDRAM is in idle state and ready for normal operation.

Programming the Mode Register

The mode register is programmed by the mode register set command using address bits A13 through A0 as data inputs. The register retains data until it is reprogrammed or the device loses power.
The mode register has four fields;

Options : A13 through A7
$\overline{\text{CAS}}$ latency : A6 through A4
Wrap type : A3
Burst length : A2 through A0

Following mode register programming, no command can be asserted befor at least two clock cycles have elapsed.

$\overline{\text{CAS}}$ Latency

$\overline{\text{CAS}}$ latency is the most critical parameter being set. It tells the device how many clocks must elapse before the data will be available.
The value is determined by the frequency of the clock and the speed grade of the device. The value can be programmed as 2 or 3.

Burst Length

Burst Length is the number of words that will be output or input in read or write cycle. After a read burst is completed, the output bus will become high impedance.
The burst length is programmable as 1, 2, 4, 8 or full page.

Wrap Type (Burst Sequence)

The wrap type specifies the order in which the burst data will be addressed. The order is programmable as either “Sequential” or “Interleave”. The method chosen will depend on the type of CPU in the system.

MODE REGISTER

13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0	0	0	0	0	0	1								JEDEC Standard Test Set
13	12	11	10	9	8	7	6	5	4	3	2	1	0	
x	x	x	x	1	0	0	LTMODE			WT	BL			Burst Read and Single Write (for Write Through Cache)
13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	LTMODE			WT	BL			Burst Read and Burst Write

X = Don't care

	Bits2 - 0	WT = 0	WT = 1
Burst length	000	1	1
	001	2	2
	010	4	4
	011	8	8
	100	R	R
	101	R	R
	110	R	R
	111	Fullpage	R

Wrap type	0	Sequential
	1	Interleave

	Bits 6-4	$\overline{\text{CAS}}$ latency
Latency mode	000	R
	001	R
	010	2
	011	3
	100	R
	101	R
	110	R
	111	R

Remark R : Reserved

Burst Length and Sequence

Burst of Two

Starting Address (column address A0, binary)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence (decimal)
0	0, 1	0, 1
1	1, 0	1, 0

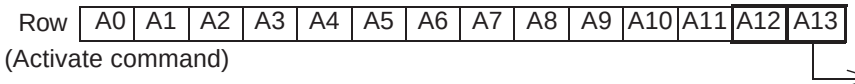
Burst of Four

Starting Address (column address A1 - A0, binary)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence (decimal)
00	0, 1, 2, 3	0, 1, 2, 3
01	1, 2, 3, 0	1, 0, 3, 2
10	2, 3, 0, 1	2, 3, 0, 1
11	3, 0, 1, 2	3, 2, 1, 0

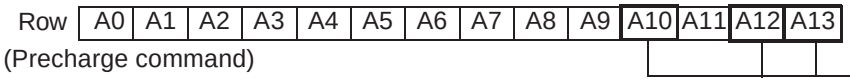
Burst of Eight

Starting Address (column address A2 - A0, binary)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence (decimal)
000	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
001	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
010	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
011	3, 4, 5, 6, 7, 0, 1 ,2	3, 2, 1, 0, 7, 6, 5, 4
100	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
101	5, 6 ,7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
110	6, 7 ,0 ,1 ,2 ,3 ,4 ,5	6, 7, 4, 5, 2, 3, 0, 1
111	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0

Address Bits of Bank-Select and Precharge



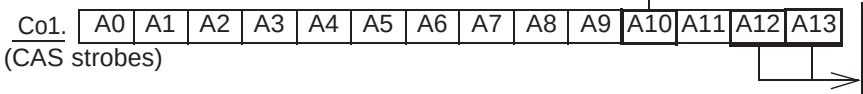
A12	A13	Result
0	0	Select Bank A “Activate “ command
0	1	Select Bank B “Activate” command
1	0	Select Bank C “Activate” command
1	1	Select Bank D “Activate” command



A10	A12	A13	Result
0	0	0	Precharge Bank A
0	0	1	Precharge Bank B
0	1	0	Precharge Bank C
0	1	1	Precharge Bank D
1	X	X	Precharge All Banks

X: Don't care

0	Disable Auto-Precharge (End of Burst)
1	Enable Auto - Precharge (End of Burst)



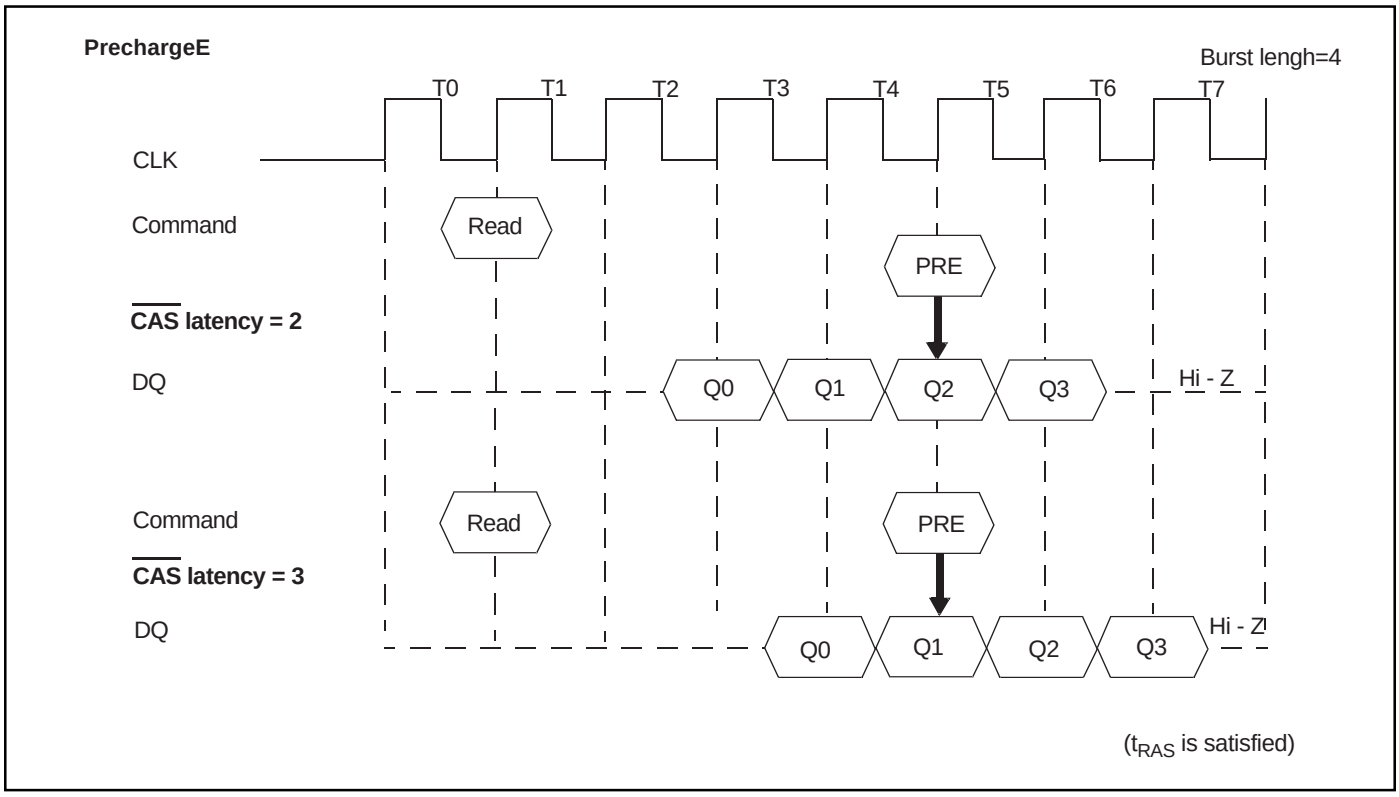
A12	A13	Result
0	0	Enable Read/Write commands for Bank A
0	1	Enable Read/Write commands for Bank B
1	0	Enable Read/Write commands for Bank C
1	1	Enable Read/Write commands for Bank D

Precharge

The precharge command can be asserted anytime after t_{RAS}(min.) is satisfied.

Soon after the precharge command is asserted, the precharge operation is performed and the synchronous DRAM enters the idle state after t_{RP}(min.) is satisfied. The parameter t_{RP} is the time required to perform the precharge.

The earliest timing in a read cycle that a precharge command can be asserted without losing any data in the burst is as follows.



In order to write all data to the memory cell correctly, the asynchronous parameter t_{DPL} must be satisfied. The t_{DPL}(min.) specification defines the earliest time that a precharge command can be asserted. The minimum number of clocks can be calculated by dividing t_{DPL}(min.) with the clock cycle time.

In summary, the precharge command can be asserted relative to the reference clock that indicates the last data word is valid. In the following table, minus means clocks before the reference; plus means time after the reference.

$\overline{\text{CAS}}$ latency	Read	Write
2	-1	+ t_{DPL}((min.)
3	-2	+ t_{DPL}((min.)

Auto Precharge

During a read or write command cycle, A10 controls whether auto precharge is selected. If A10 is high in the read or write command (Read with Auto precharge command or Write with Auto precharge command), auto precharge is selected and begins automatically.

In the write cycle, t_{DAL}(min.) must be satisfied before asserting the next activate command to the bank being precharged. When using auto precharge in the read cycle, knowing when the precharge starts is important because the next activate command to the bank being precharged cannot be executed until the precharge cycle ends. Once auto precharge has started, an activate command to the bank can be asserted after t_{RP} has been satisfied.

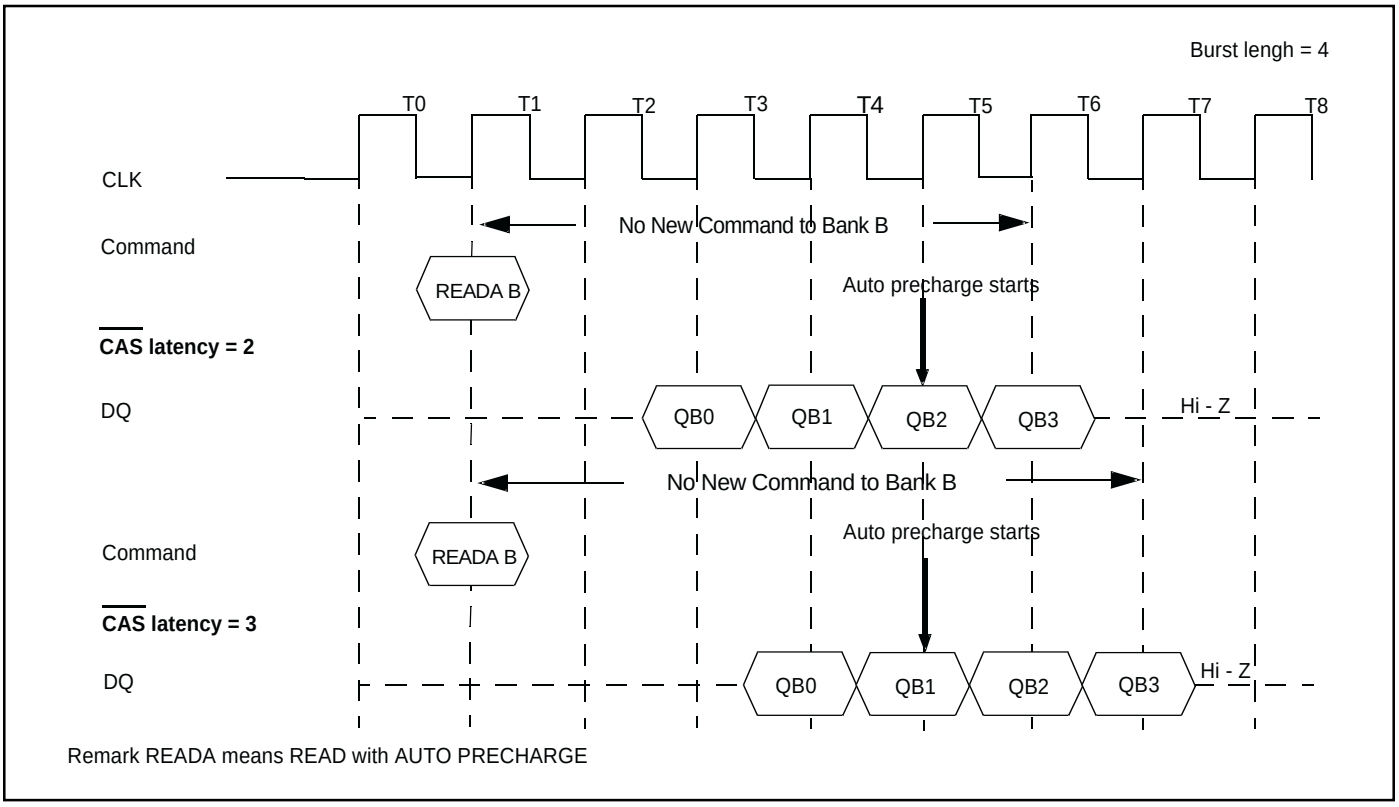
A Read or Write command without auto - precharge can be terminated in the midst of a burst operation. However, a Read or Write command with auto - precharge can not be interrupted by the same bank commands before the entire burst operation is completed. Therefore use of the same bank Read, Write, Precharge or Burst Stop command is prohibited during a read or write cycle with auto - precharge. It should be noted that the device will not respond to the Auto - Precharge command if the device is programmed for full page burst read or write cycles.

The timing when the auto precharge cycle begins depends both on both the $\overline{CAS}$ latency programmed into the mode register and whether the cycle is read or write.

Read with Auto Precharge

During a READA cycle, the auto precharge begins one clock earlier (CL = 2) or two clocks earlier (CL = 3) than the last word output.

READ with AUTO PRECHARGE

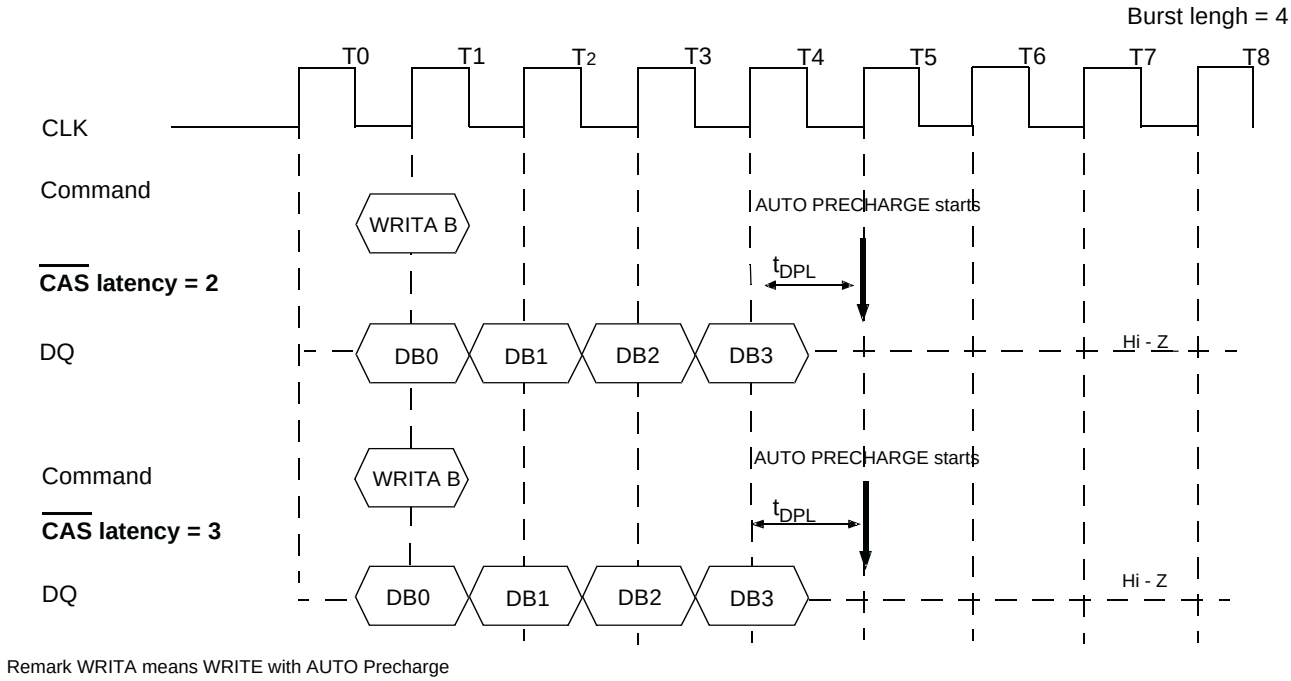


Remark READA means READ with AUTO PRECHARGE

Write with Auto Precharge

During a write cycle, the auto precharge starts at the timing that is equal to the value of t_{DPL}(min.) after the last data word input to the device.

WRITE with AUTO PRECHRGE



Remark WRITA means WRITE with AUTO Precharge

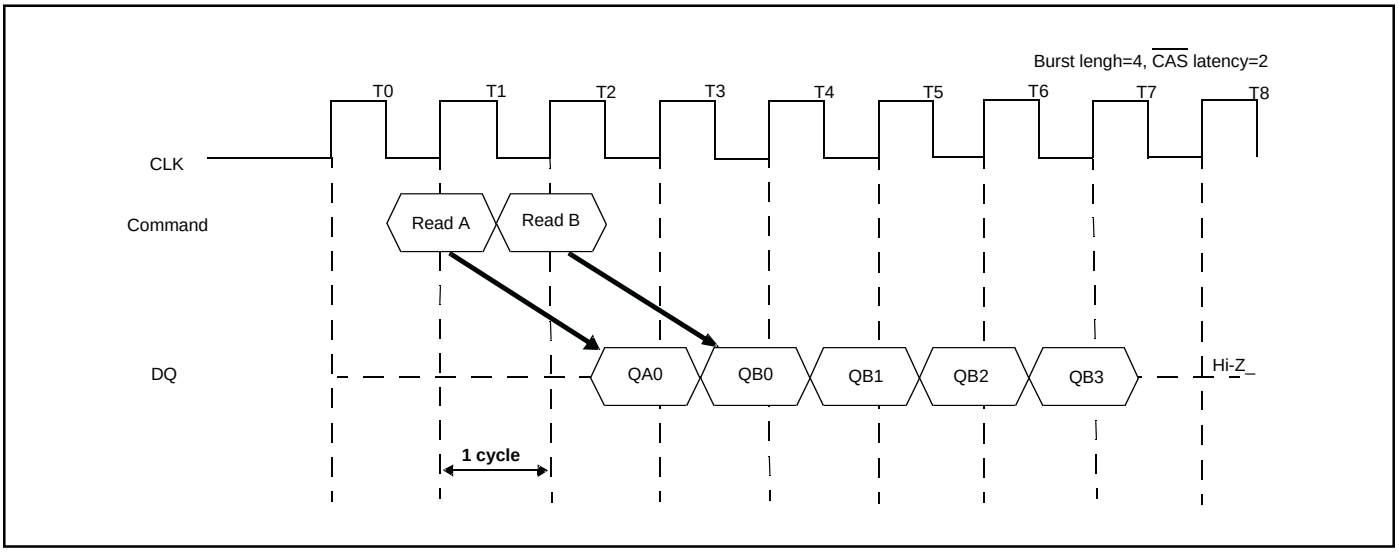
In summary, the auto precharge cycle begins relative to a reference clock that indicates the last data word is valid. In the table below, minus means clocks before the reference; plus means clocks after the reference.

$\overline{\text{CAS}}$ latency	Read	Write
2	-1	+ t_{DPL}((min.)
3	-2	+ t_{DPL}((min.)

Read / Write Command Interval

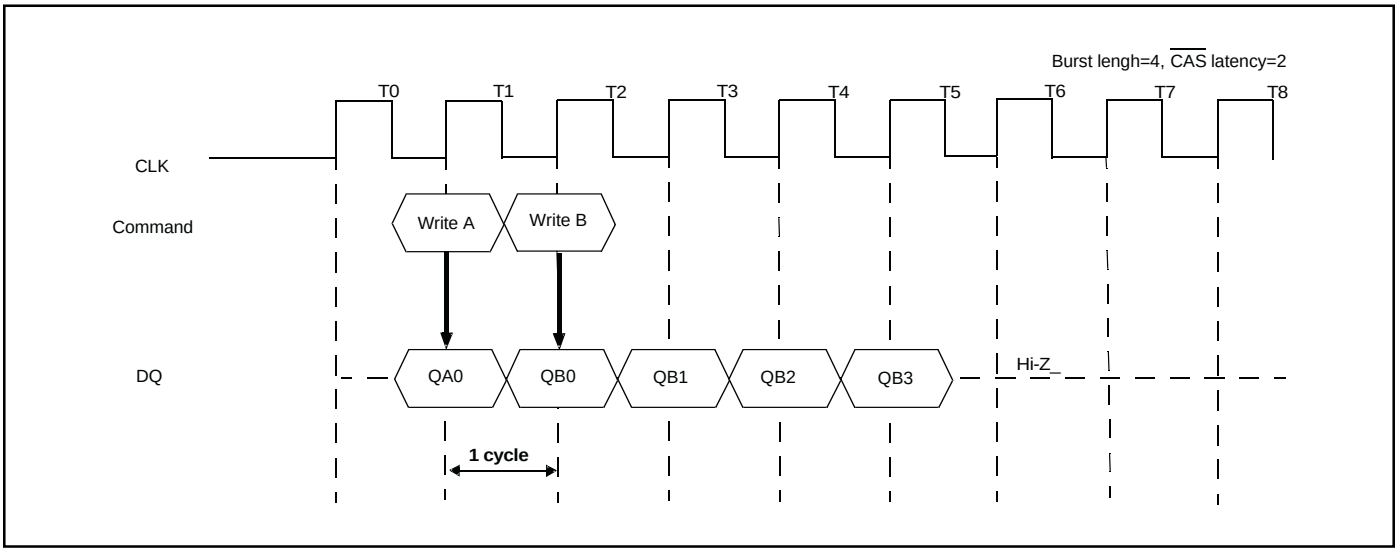
Read to Read Command Interval
During a read cycle when a new read command is asserted, it will be effective after the $\overline{CAS}$ latency, even if the previous read operation has not completed. READ will be interrupted by another READ.
Each read command can be asserted in every clock without any restriction.

READ to READ Command Interval



Write to Write Command Interval
During a write cycle, when a new Write command is asserted, the previous burst will terminate and the new burst will begin with a new write command. WRITE will be interrupted by another WRITE.
Each write command can be asserted in every clock without any restriction.

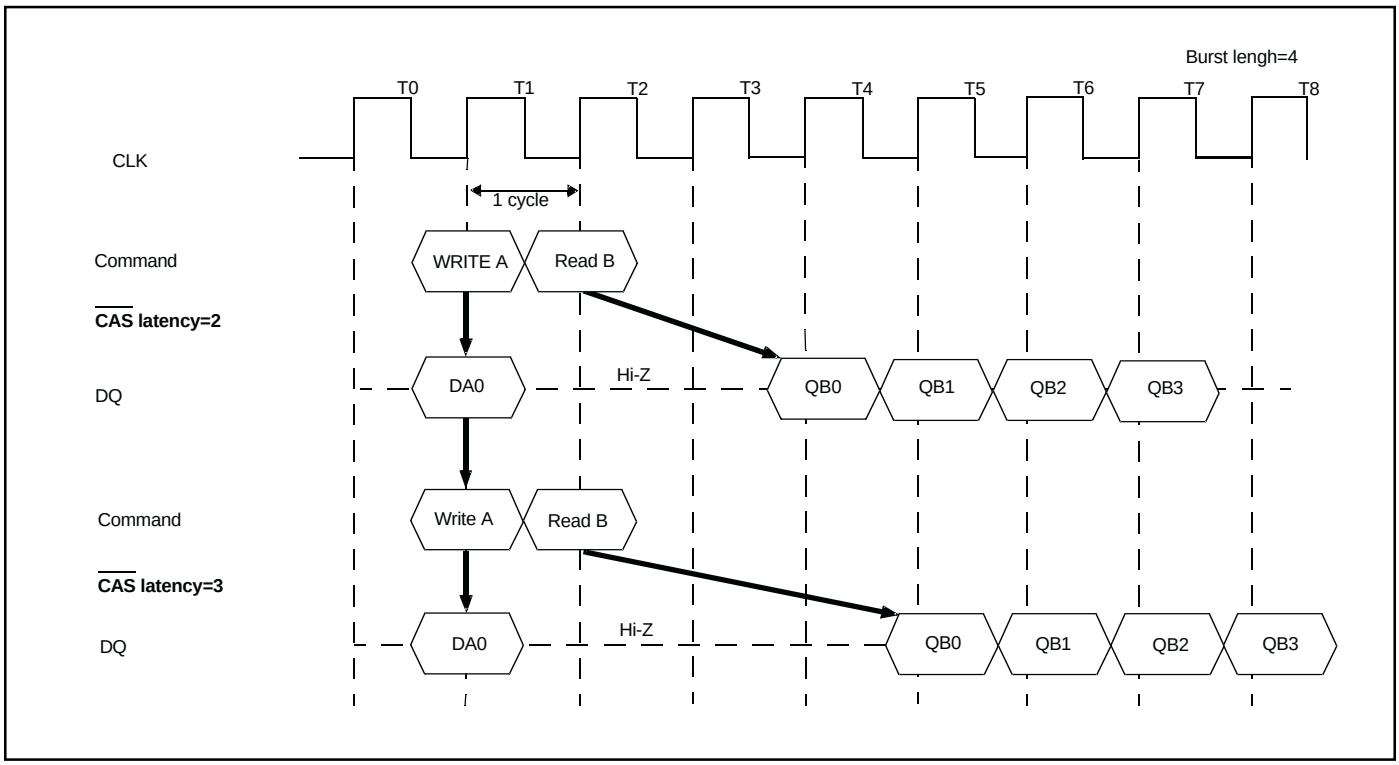
WRITE to WRITE Command Interval



Write to Read Command Interval

The write command to read command interval is also a minimum of 1 cycle. Only the write data before the read command will be written. The data bus must be Hi-Z at least one cycle prior to the first DOUT.

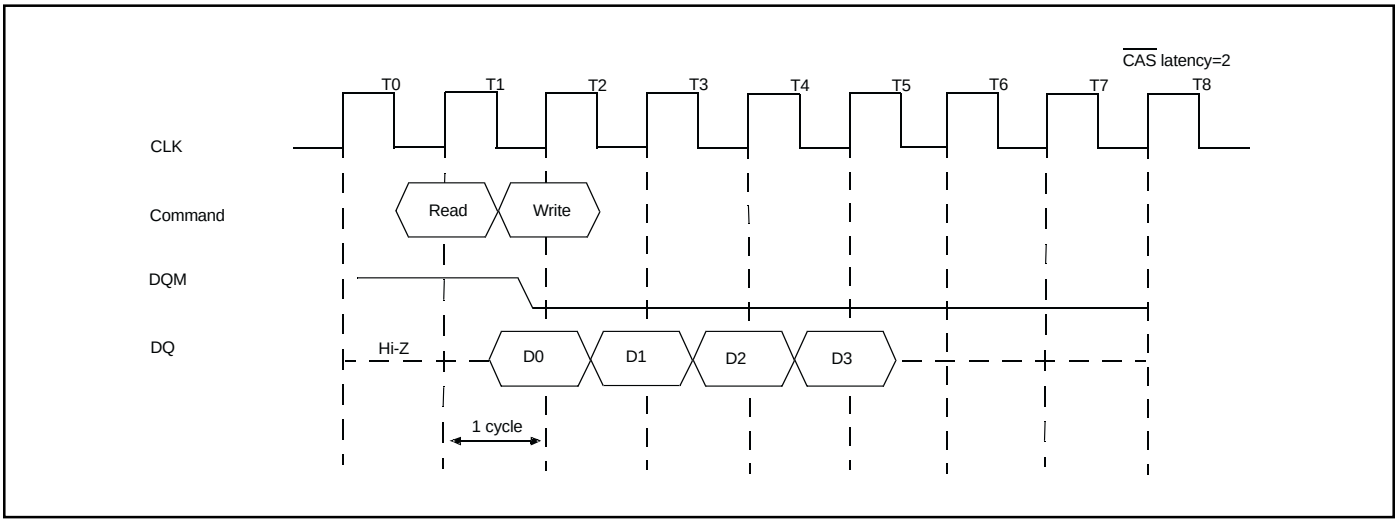
WRITE to READ Command Interval

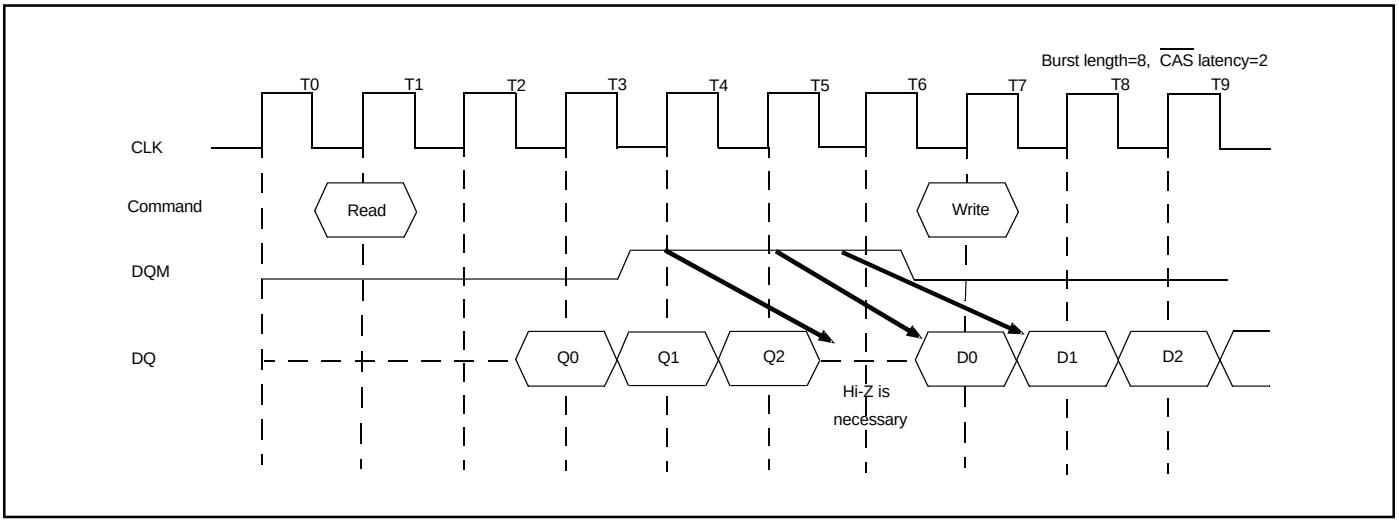


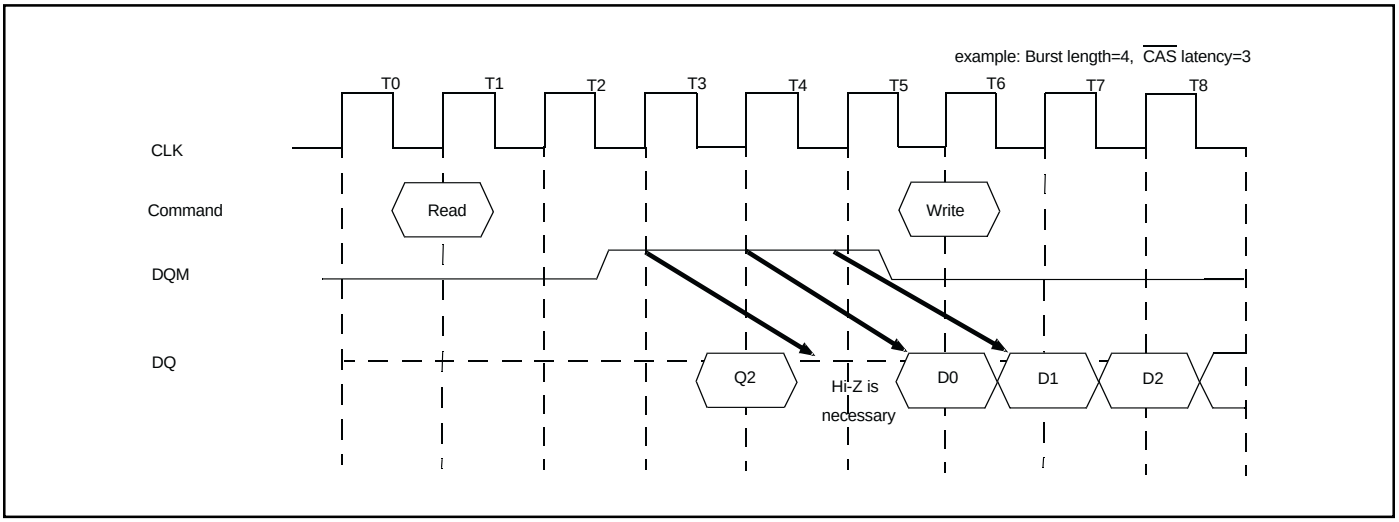
Read to Write Command Interval

During a read cycle, READ can be interrupted by WRITE.
DQM must be in High at least 3 clocks prior to the write command. There is a restriction to avoid a data conflict. The data bus must be Hi-Z using DQM before Write.

READ to WRITE Command Interval







BURST Termination

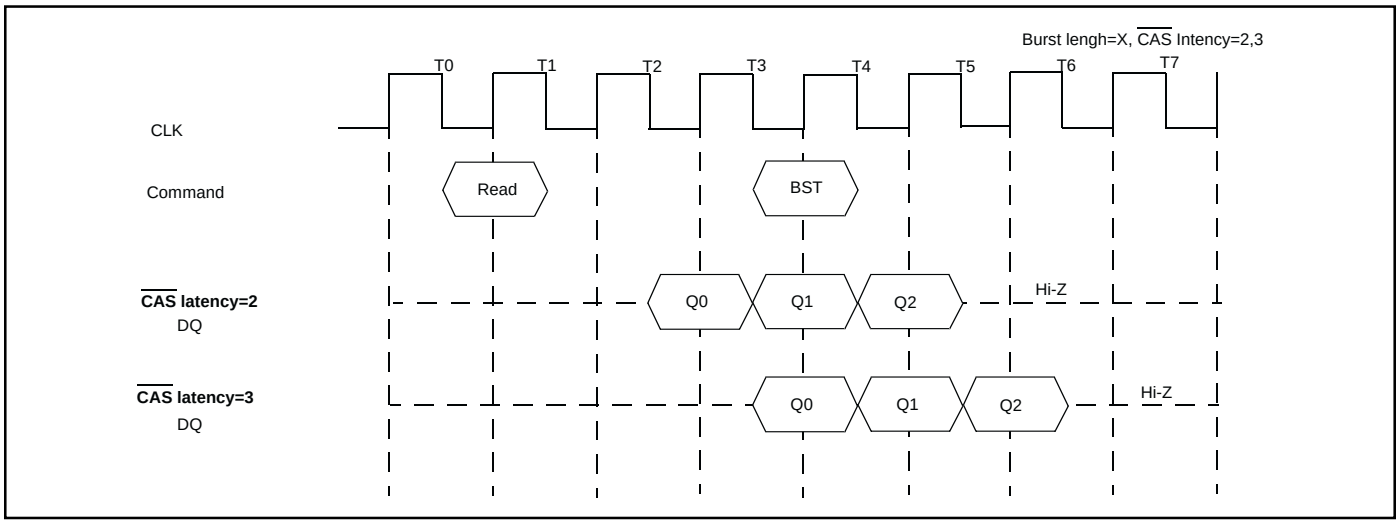
There are two methods to terminate a burst operation other than using a read or a write command. One is the burst stop command and the other is the precharge command.

BURST Stop Command

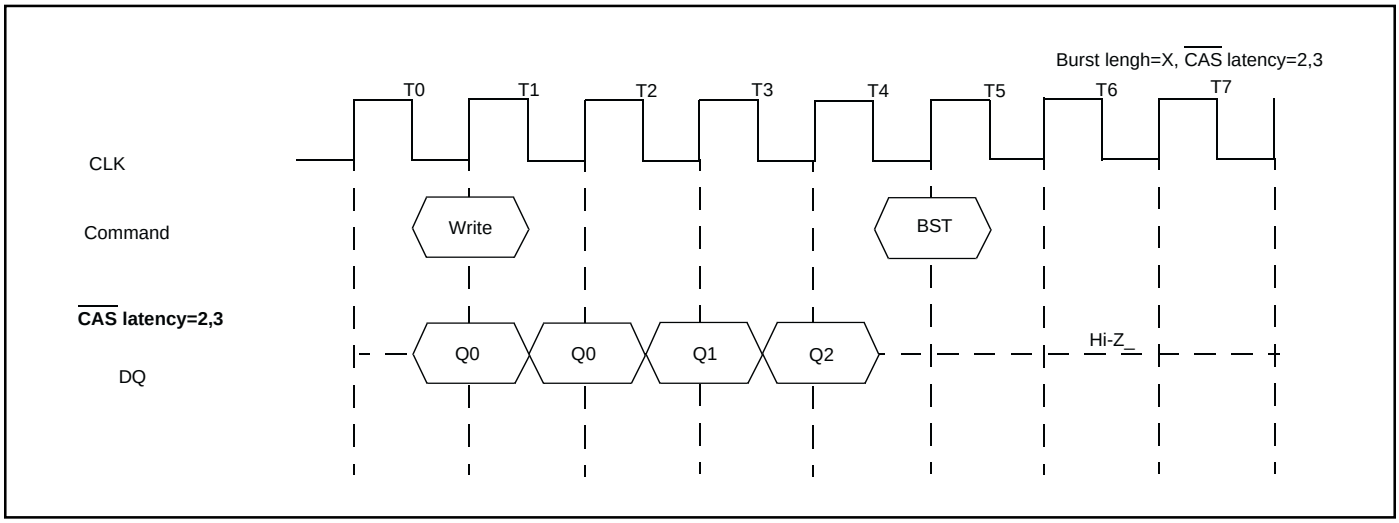
During a read burst, when the burst stop command is issued, the burst read data are terminated and the data bus goes to high-impedance after the $\overline{CAS}$ latency from the burst stop command.

During a write burst, when the burst stop command is issued, the burst write data are termained and data bus goes to Hi-Z at the same clock with the burst stop command.

Burst Termination



Remark BST: Burst stop command



Remark BST: Burst command

PRECHARGE TERMINATION

PRECHARGE TERMINATION in READ Cycle

During READ cycle, the burst read operation is terminated by a precharge command.

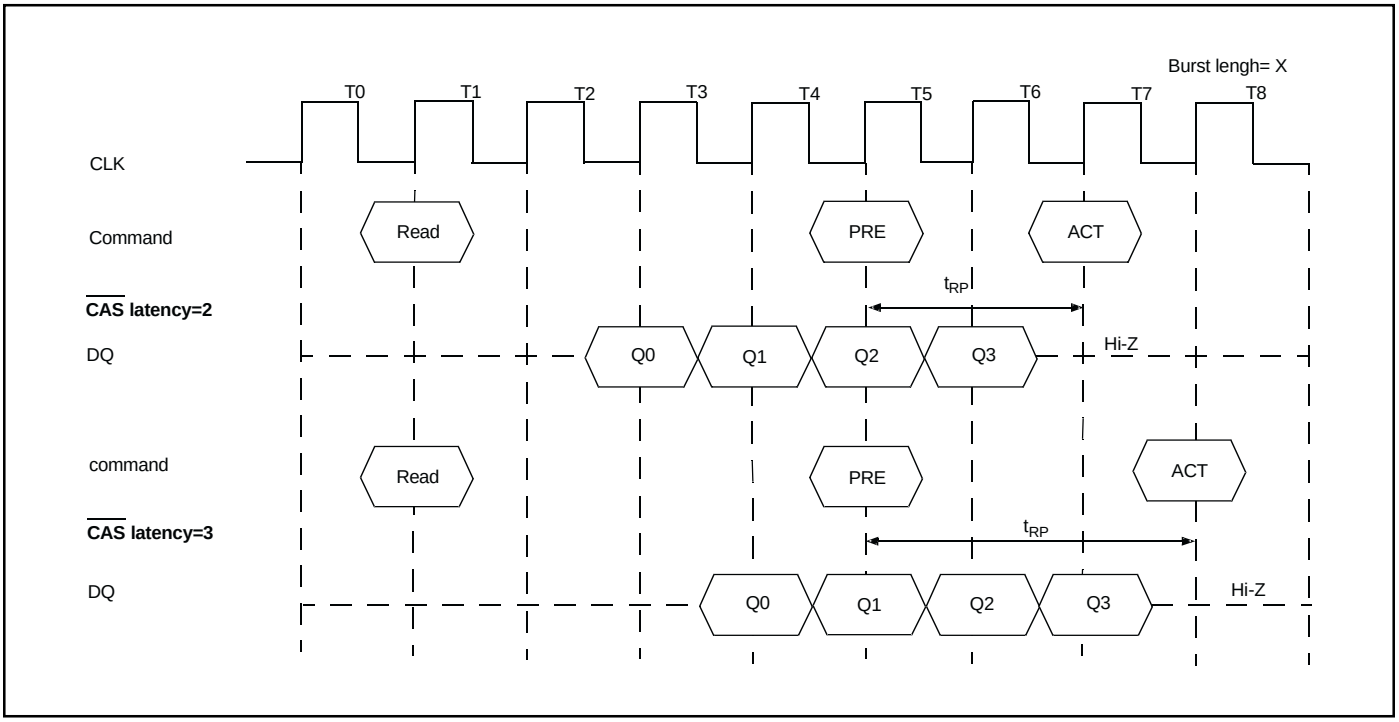
When the precharge command is issued, the burst read operation is terminated and precharge starts.

The same bank can be activated again after t_{RP} from the precharge command.

When $\overline{CAS}$ latency is 2, the read data will remain valid until one clock after the precharge command.

When $\overline{CAS}$ latency is 3, the read data will remain valid until two clocks after the precharge command.

Precharge Termination in READ Cycle



Precharge Termination in WRITE Cycle

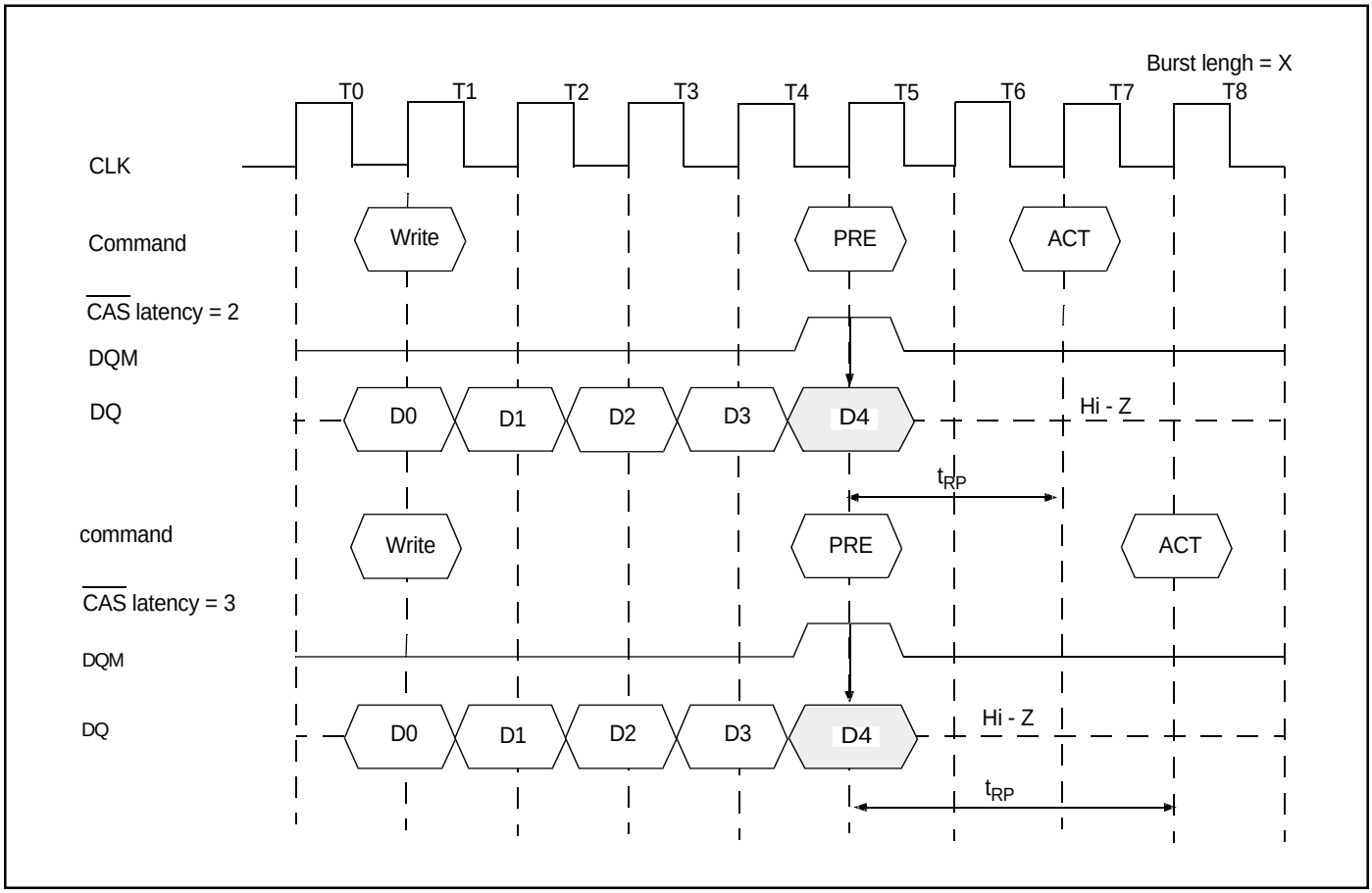
During WRITE cycle, the burst write operation is terminated by a precharge command.

When the precharge command is issued, the burst write operation is terminated and precharge starts.

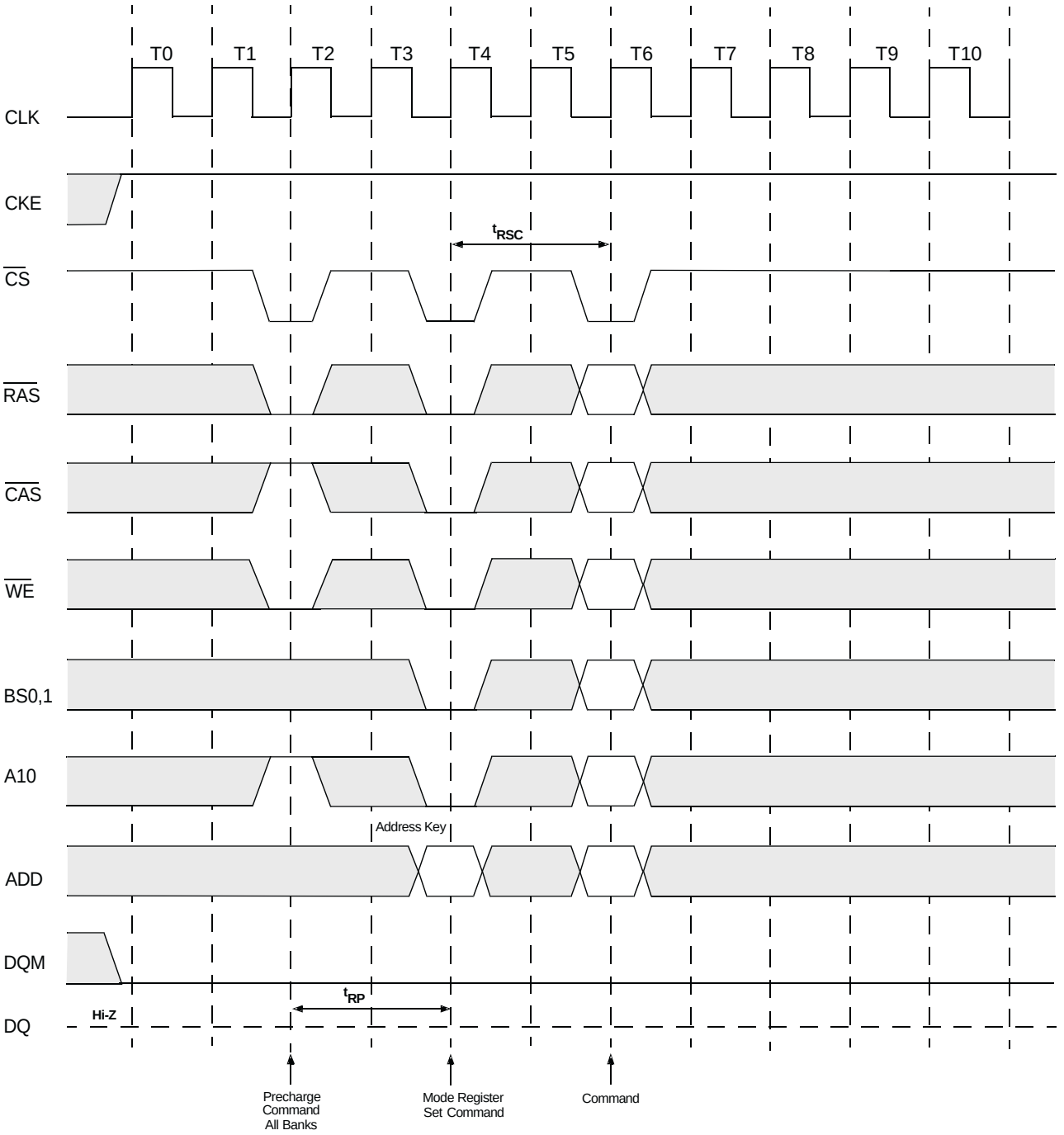
The same bank can be activated again after t_{RP} from the precharge command. The DQM must be high to mask invalid data in.

During WRITE cycle, the write data written prior to the precharge command will be correctly stored. However, invalid data may be written at the same clock as the precharge command. To prevent this from happening, DQM must be high at the same clock as the precharge command. This will mask the invalid data.

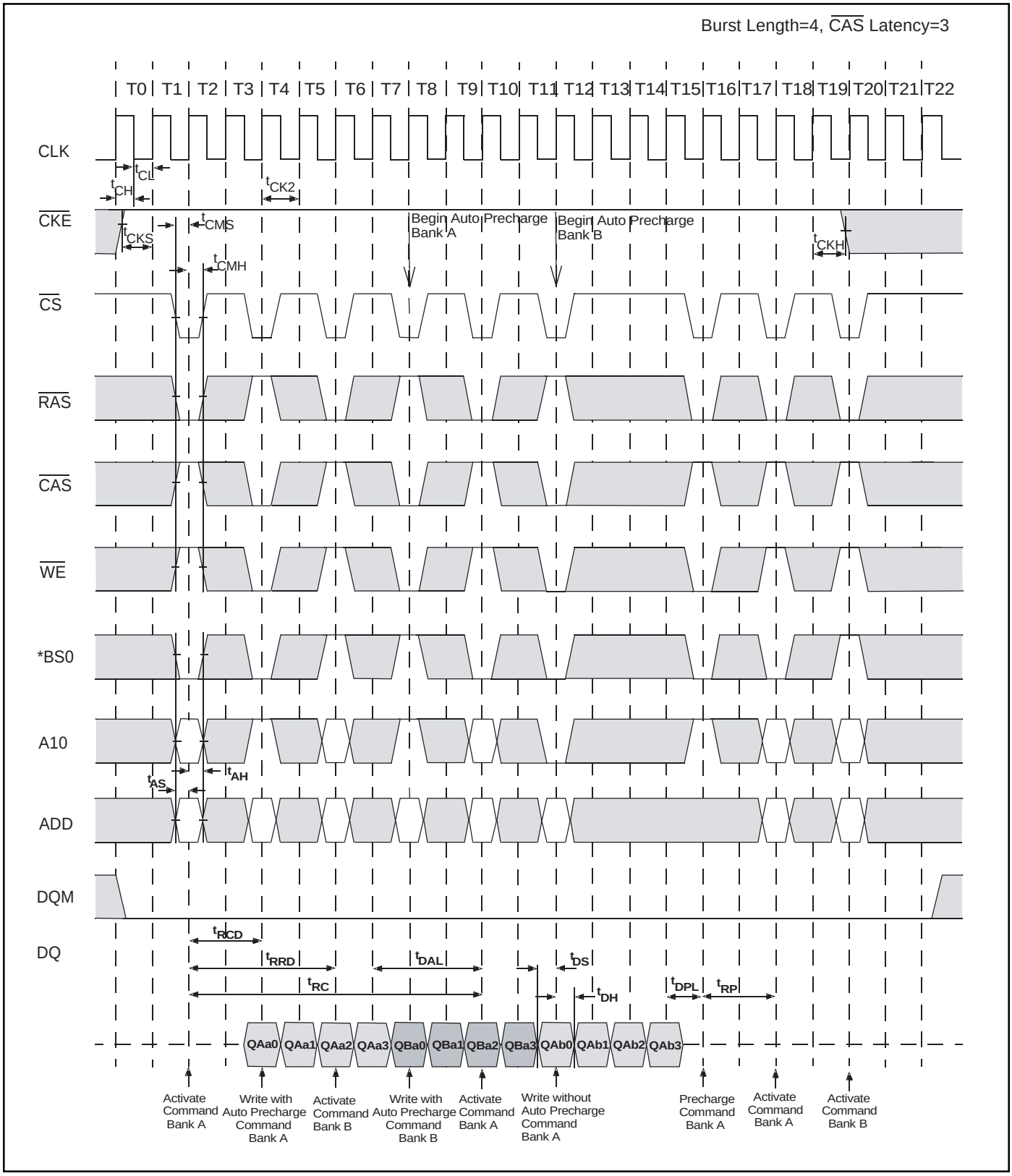
PRECHARGE TERMINATION in WRITE Cycle



Mode Register Set

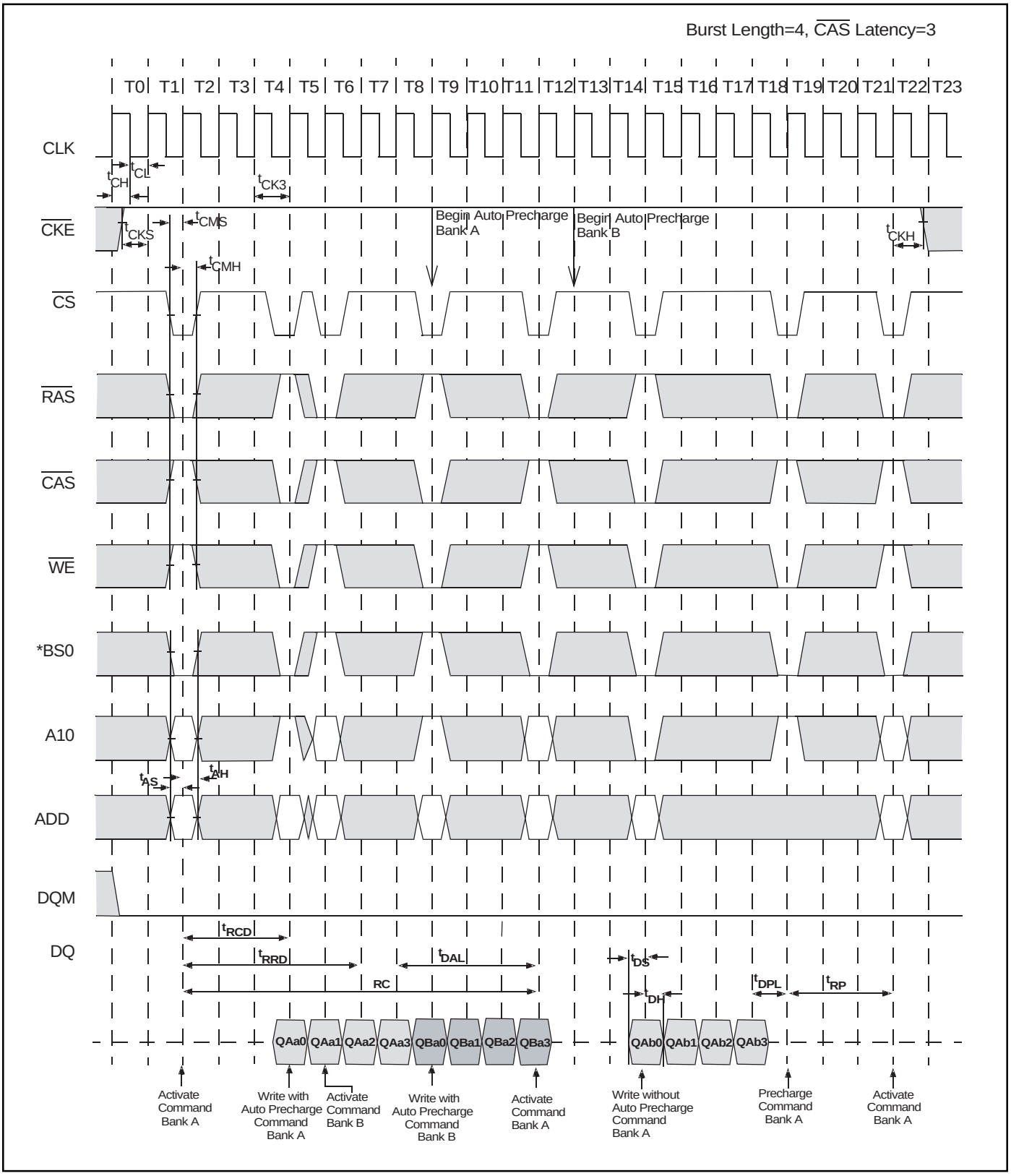


AC Parameters for Write Timing (1 of 2)



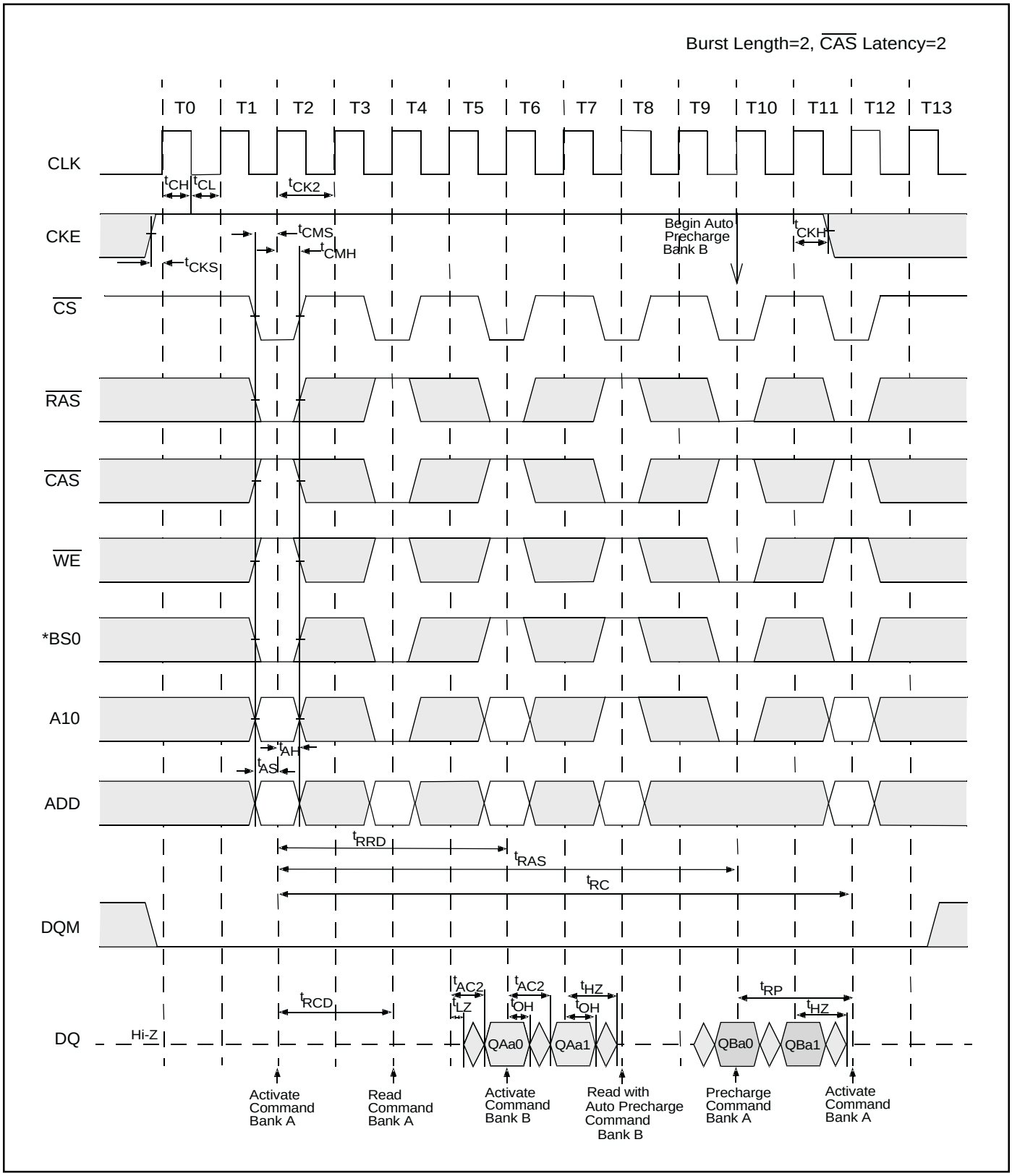
BS1="L", Bank C,D = Idle

AC Parameters for Write Timing (2 of 2)



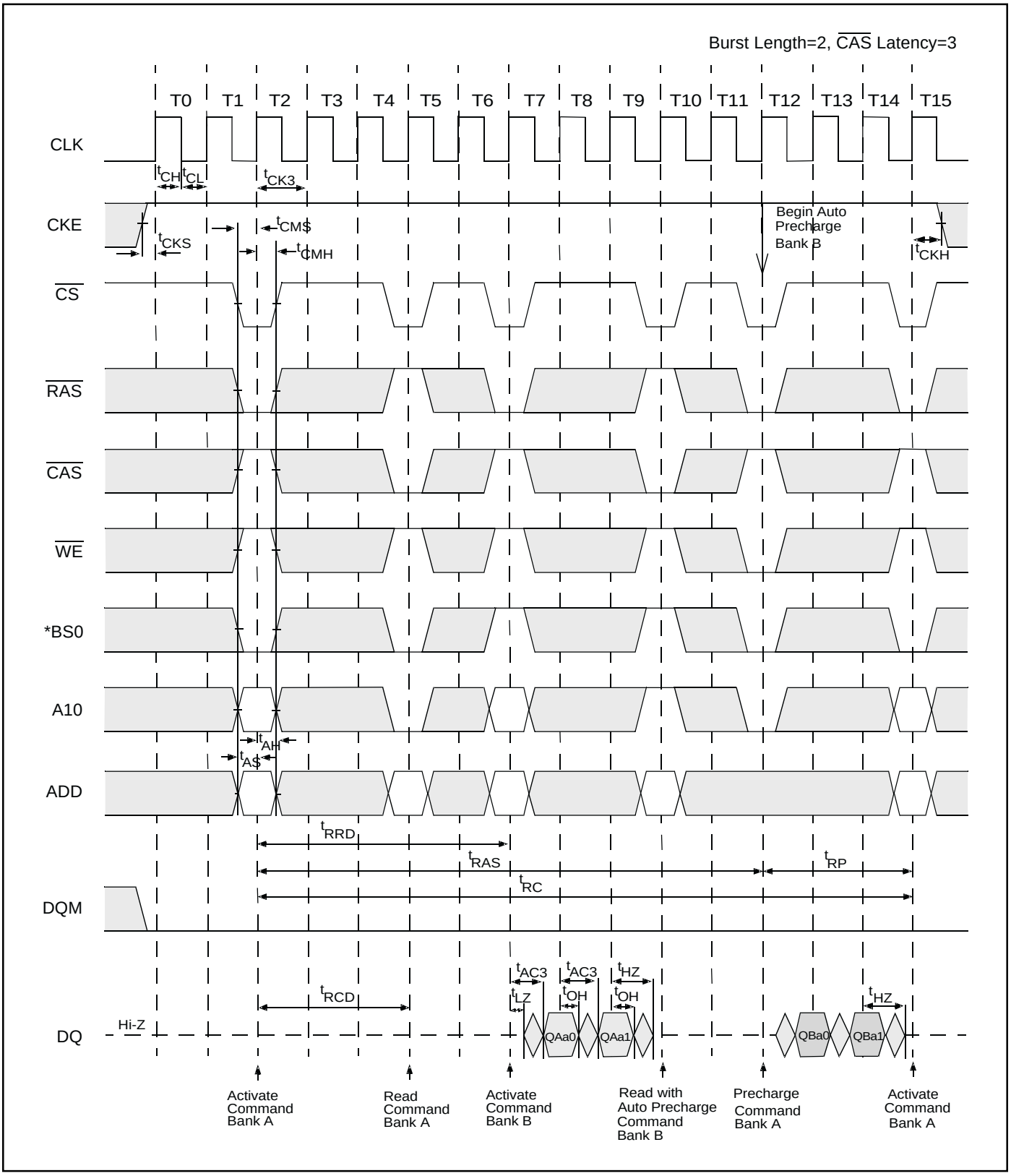
BS1="L", Bank C,D = Idle

AC Parameters for Read Timing (1 of 2)



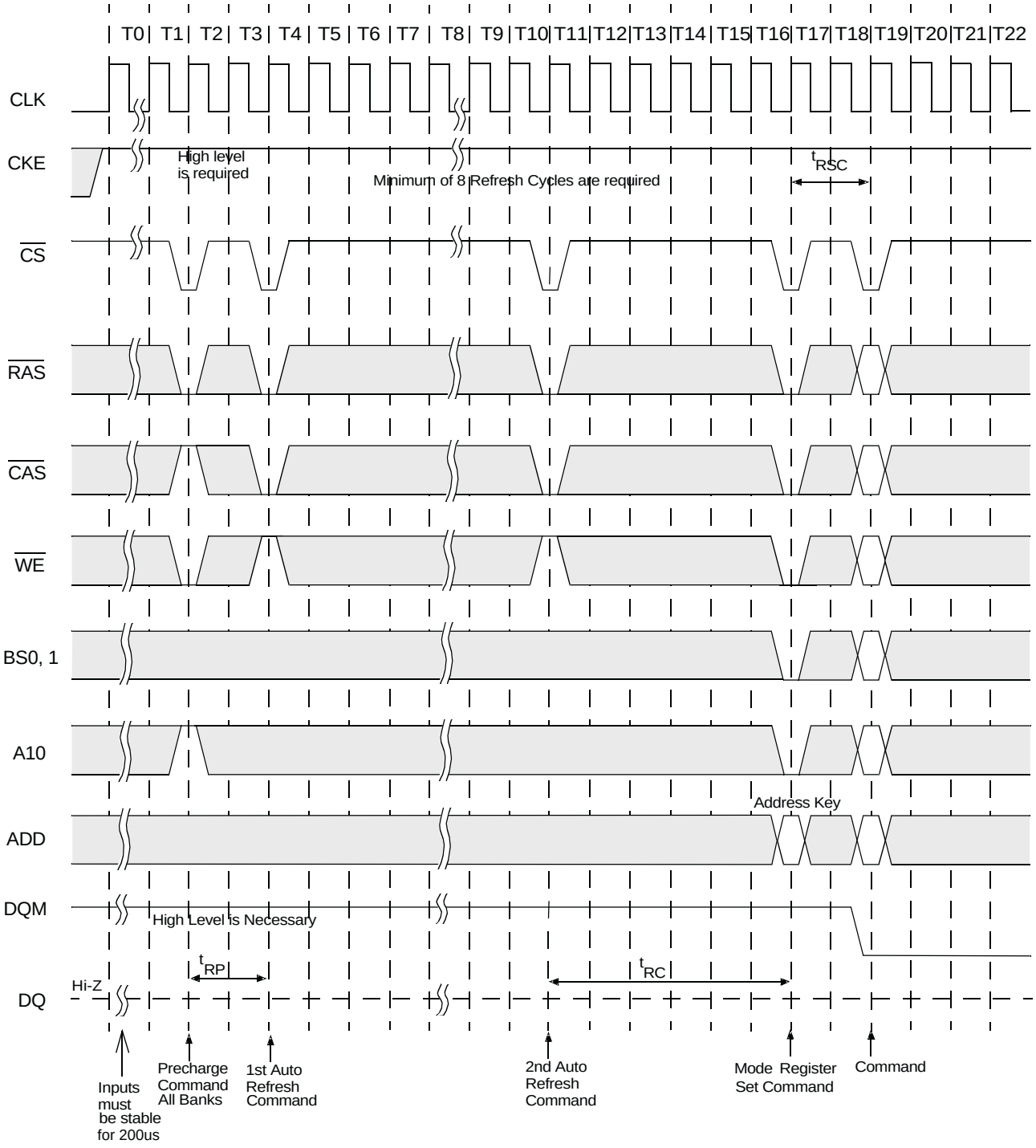
BS1="L", Bank C,D = Idle

AC Parameters for Read Timing (2 of 2)

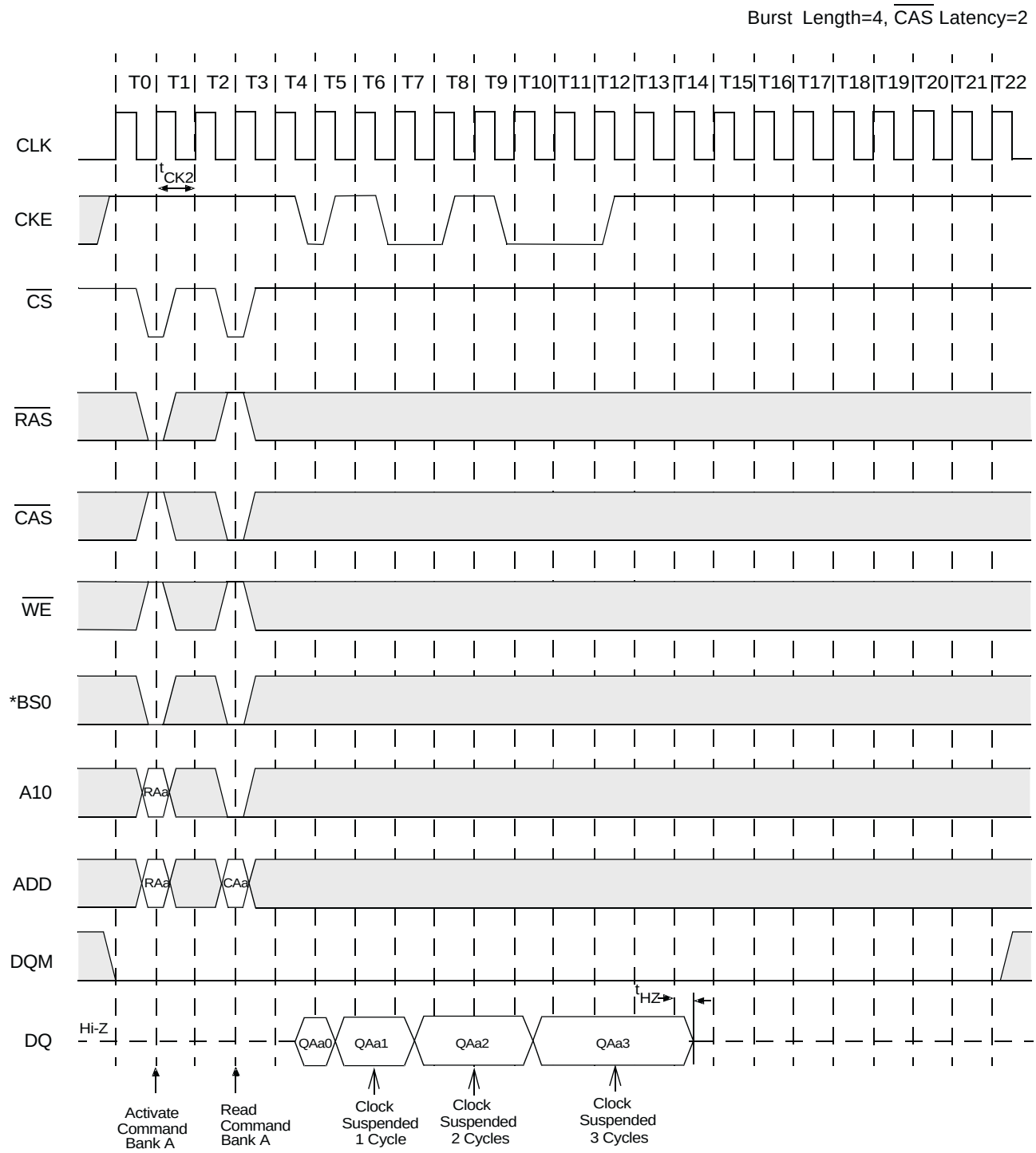


BS1="L", Bank C,D = Idle

Power on Sequence and Auto Refresh (CBR)

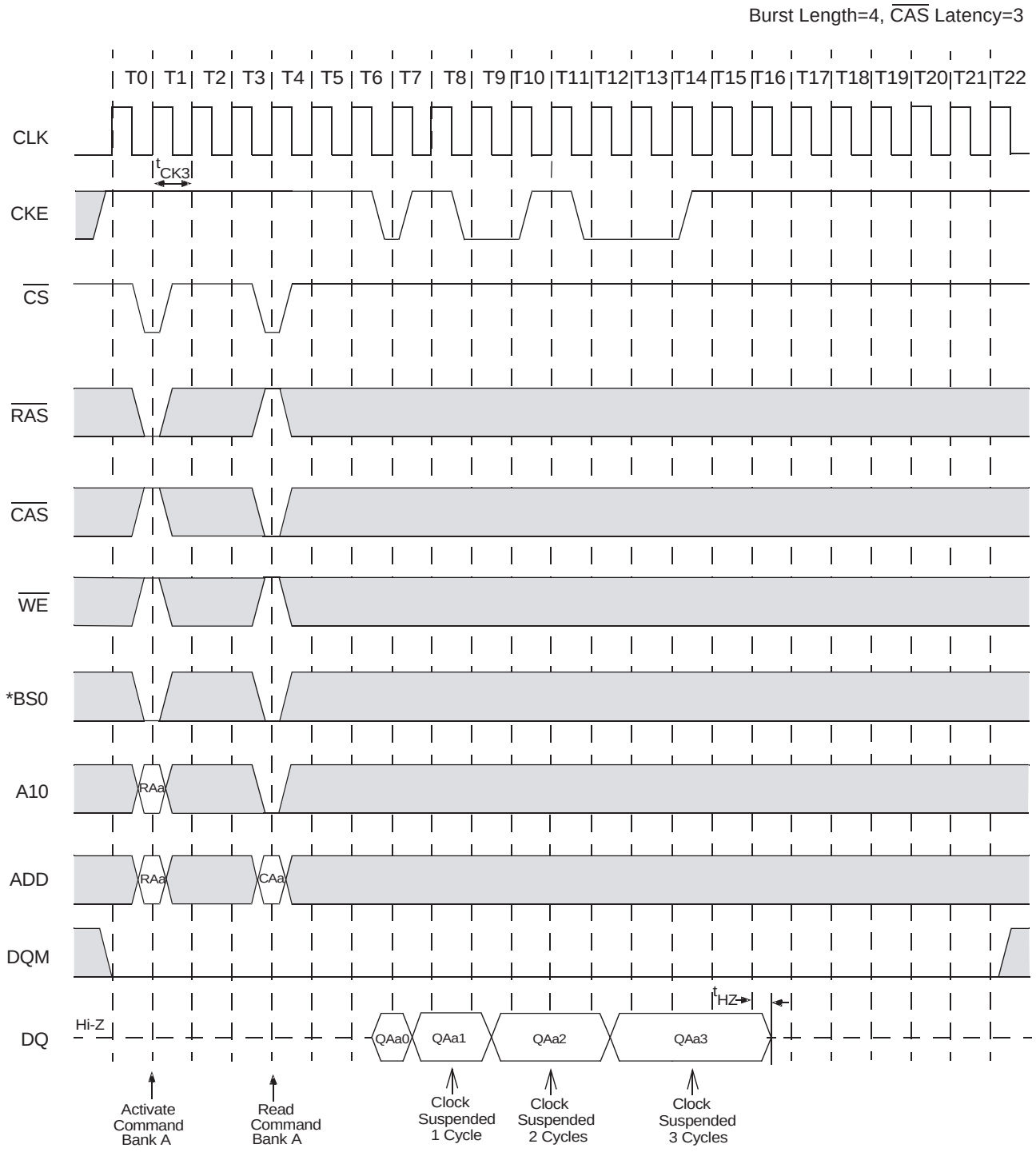


Clock Suspension During Burst Read (Using CKE) (1 of 2)



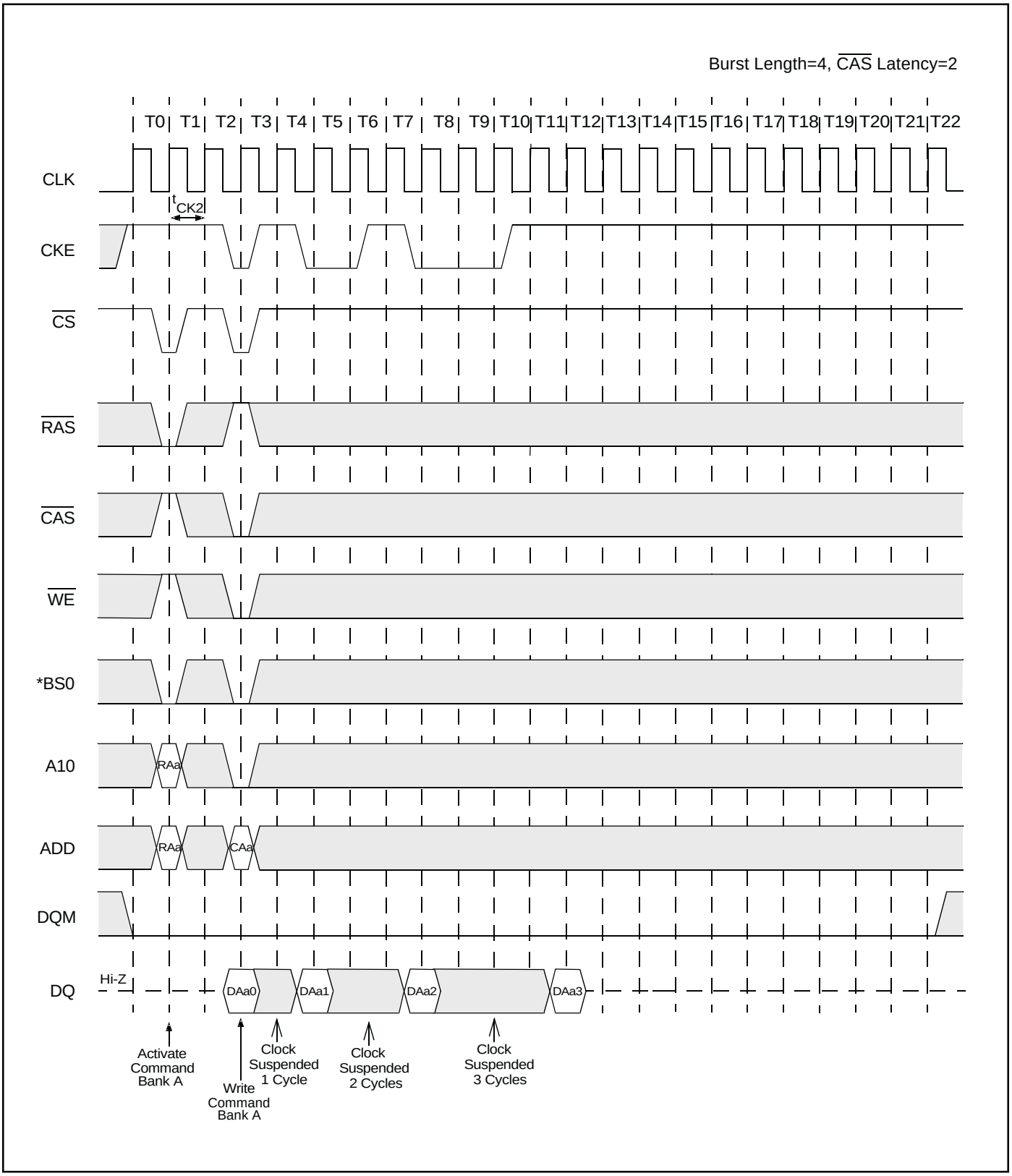
BS1="L", Bank C,D = Idle

Clock Suspension During Burst Read (Using CKE) (2 of 2)



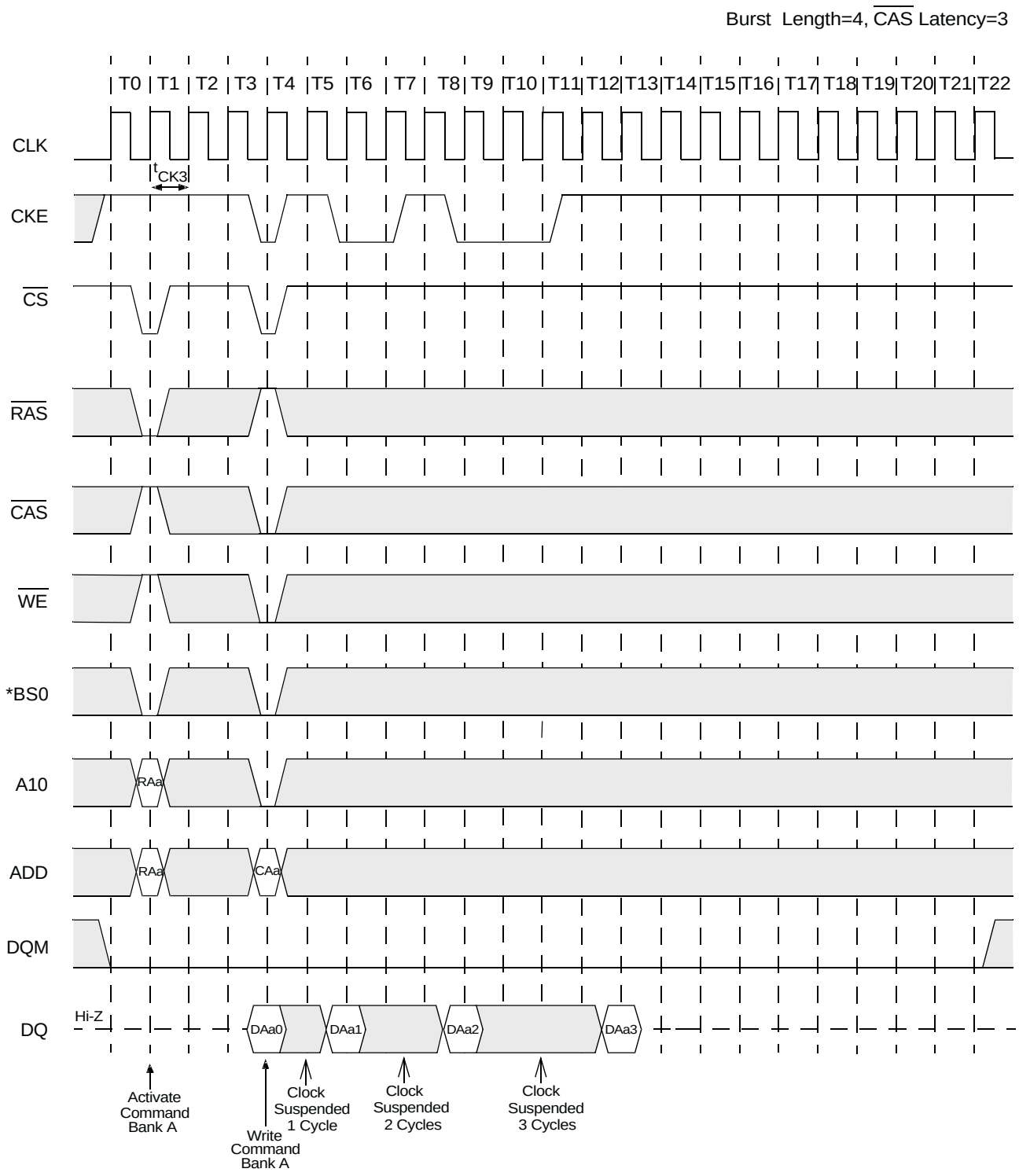
BS1="L", Bank C,D = Idle

Clock Suspension During Burst Write (Using CKE) (1 of 2)



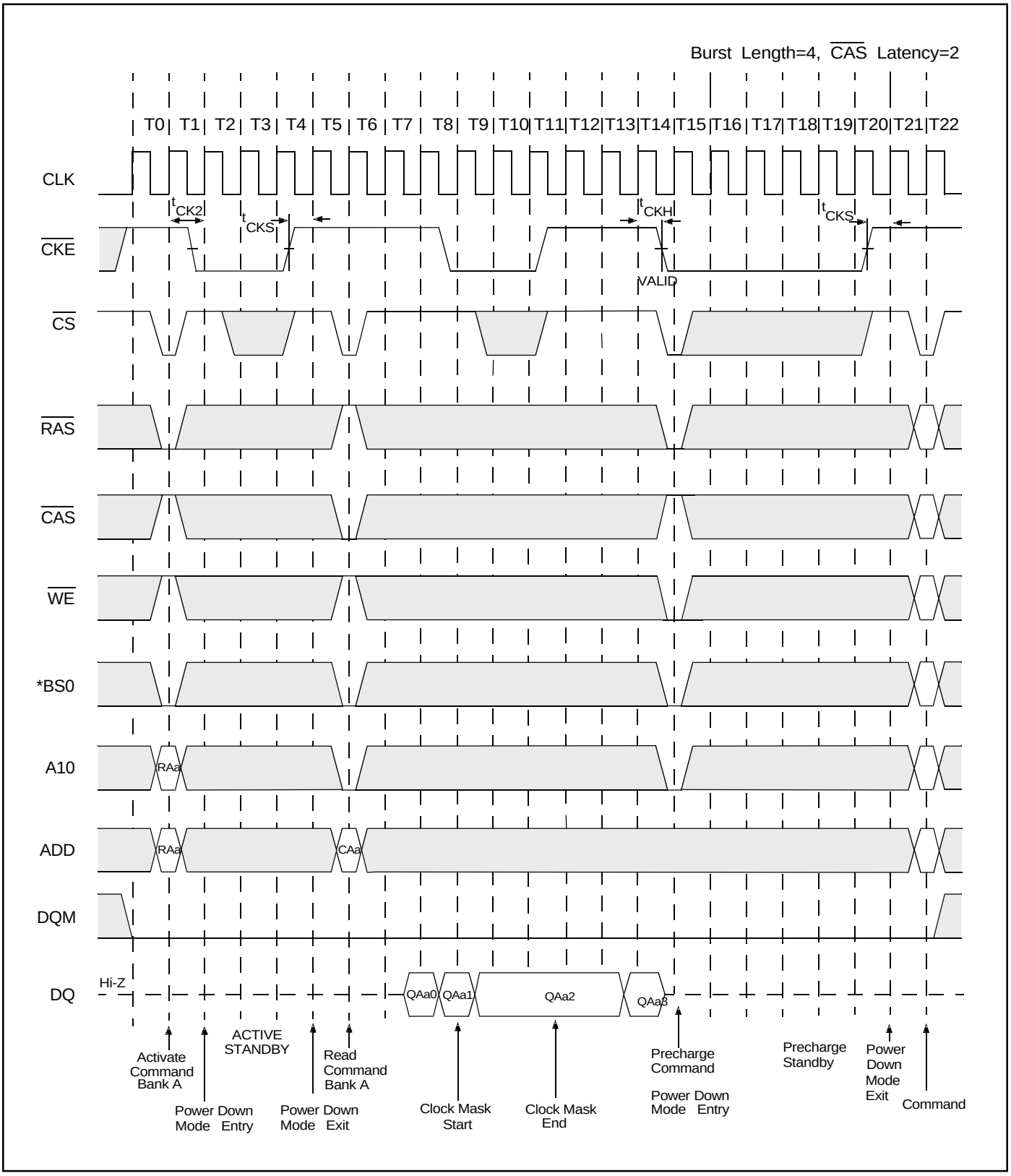
BS1="L", Bank C,D = Idle

Clock Suspension During Burst Write (Using CKE) (2 of 2)



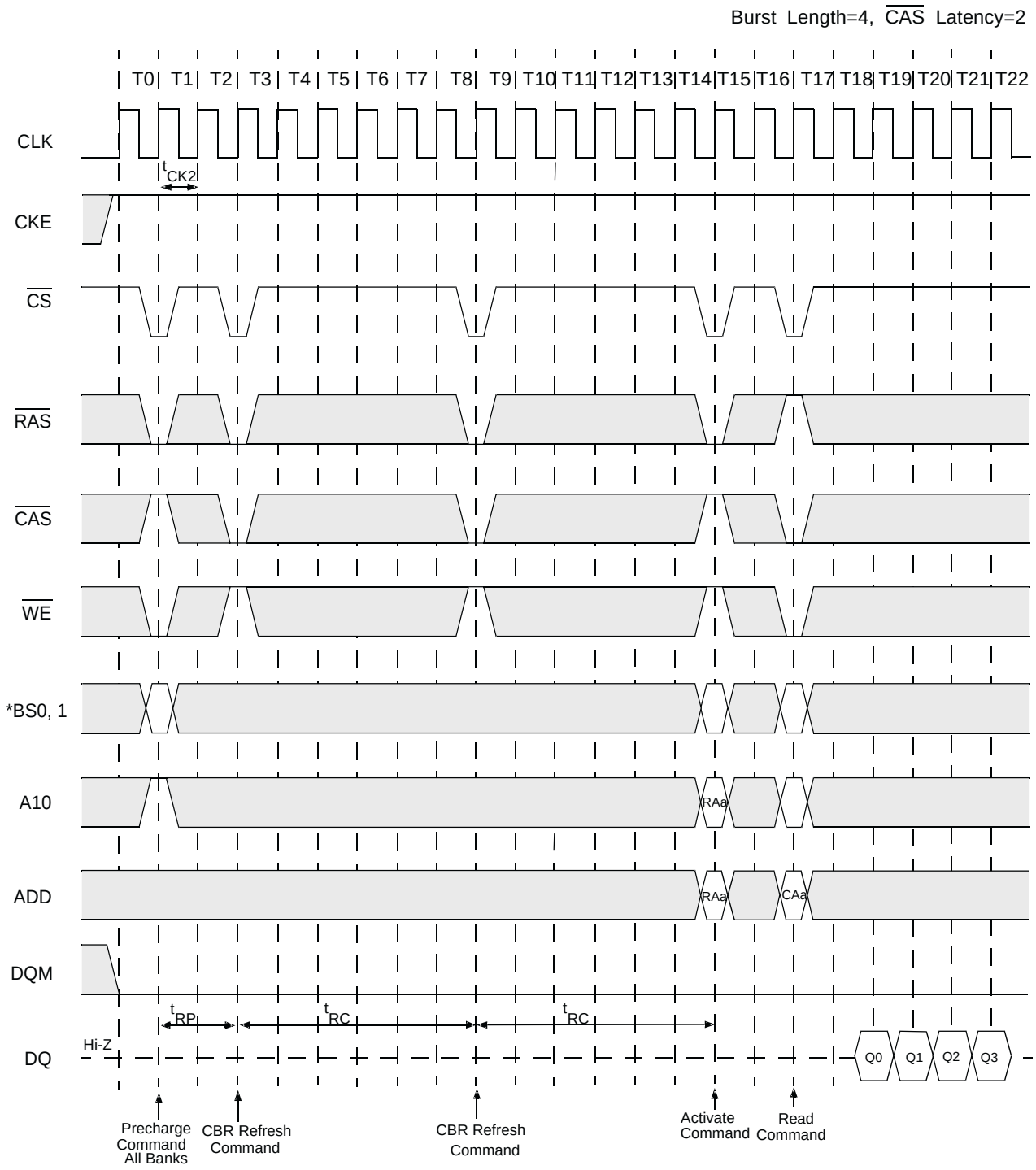
BS1="L", Bank C,D = Idle

Power Down Mode and Clock Mask



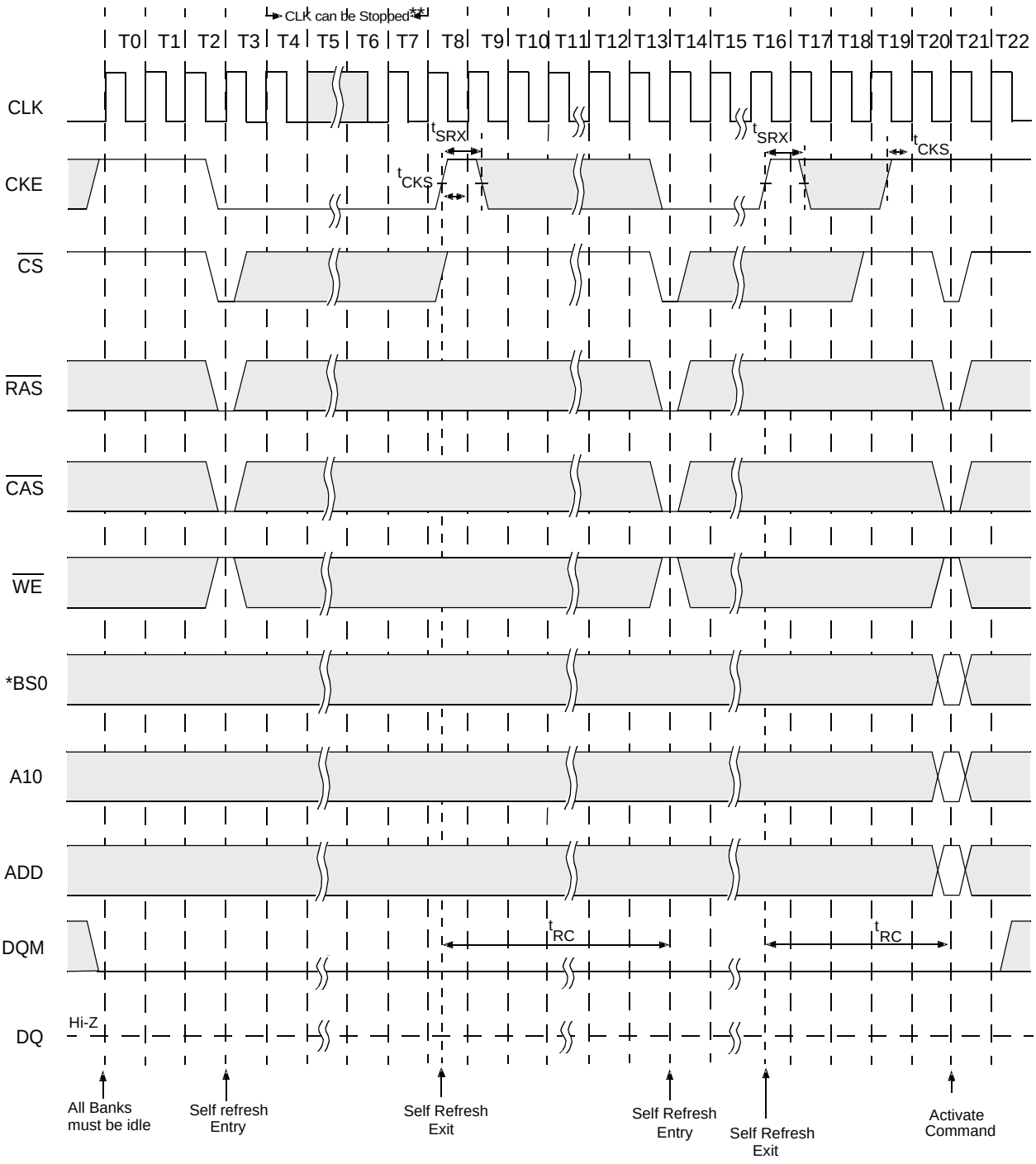
BS1="L", Bank C,D = Idle

Auto Refresh (CBR)



BS1="L", Bank C,D = Idle

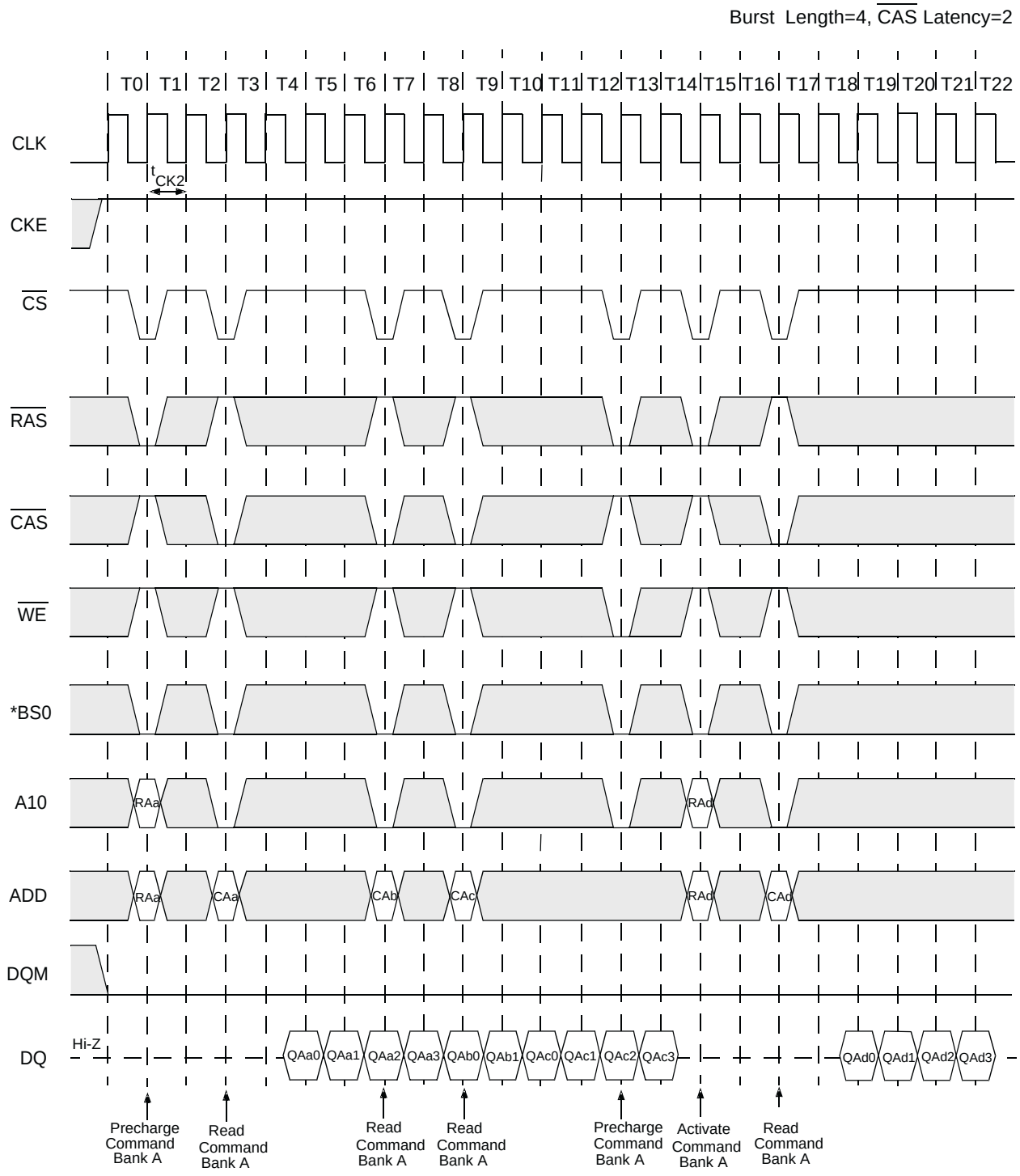
Self Refresh (Entry and Exit)



BS1="L", Bank C,D = Idle

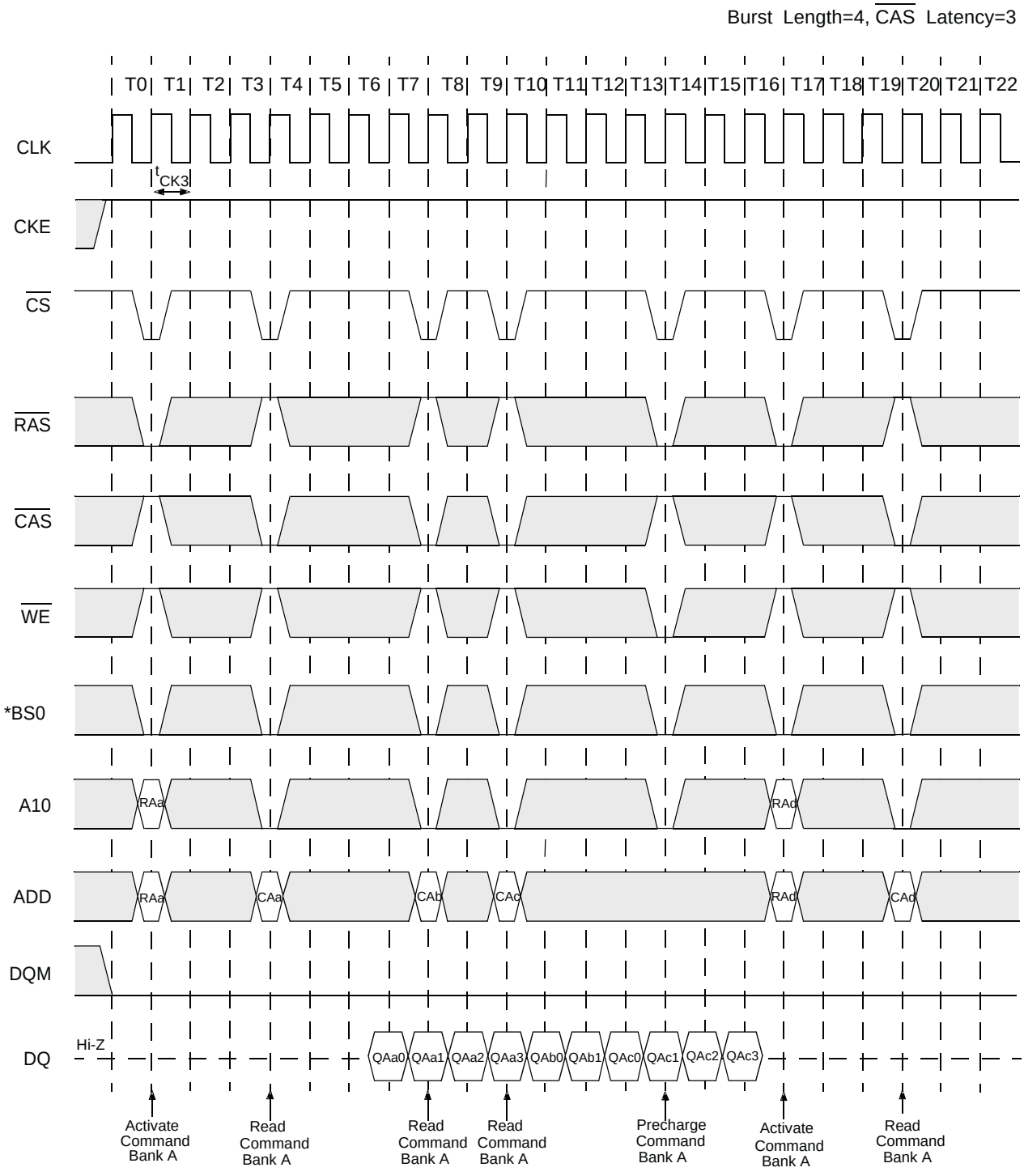
Clock can be stopped at CKE=Low. If clock is stopped, it must be restarted/stable for 4 clock cycles before CKE=High

Random Column Read (Page With Same Bank) (1 of 2)



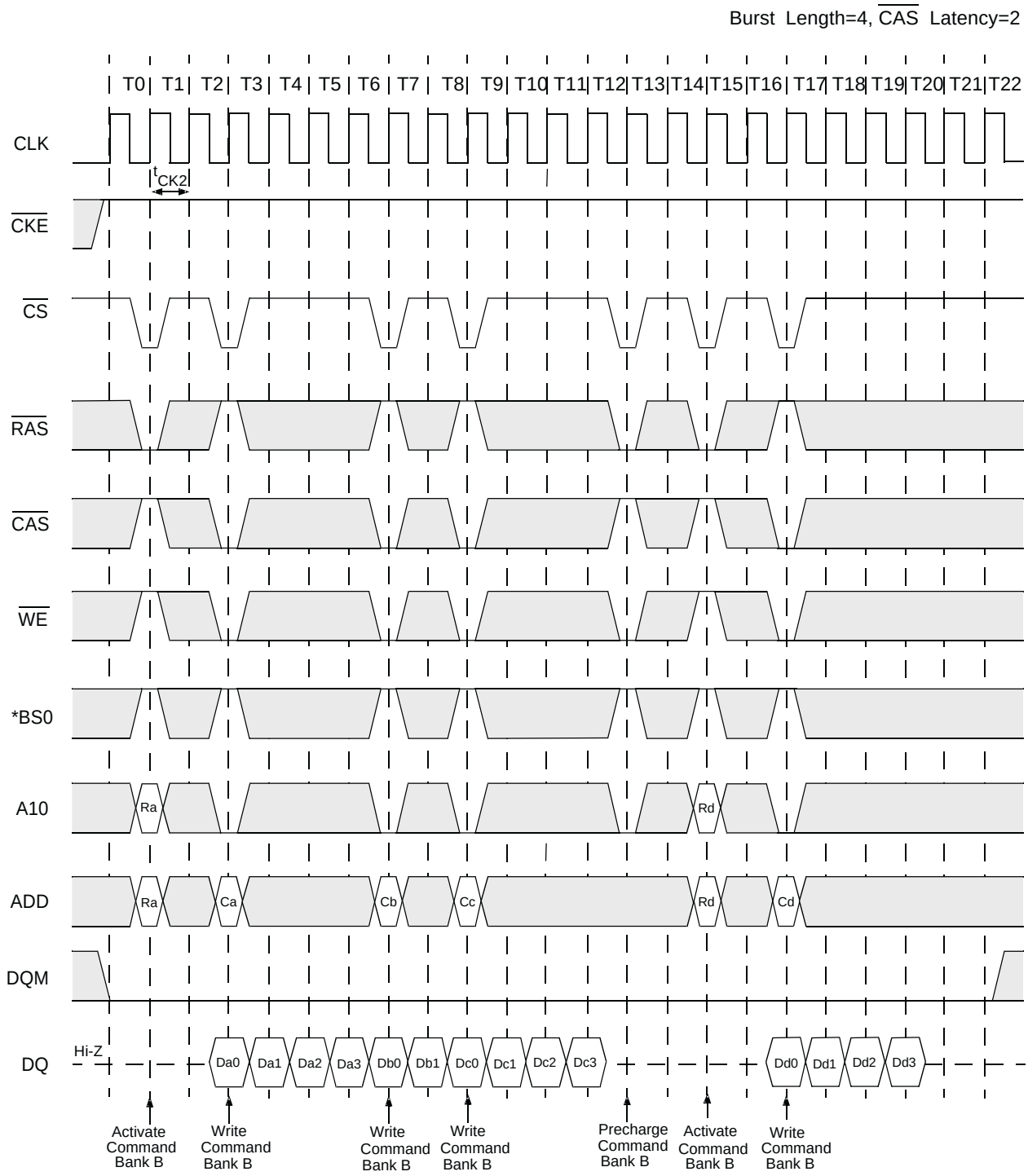
BS1="L", Bank C,D = Idle

Random Column Read (Page With Same Bank) (2 of 2)



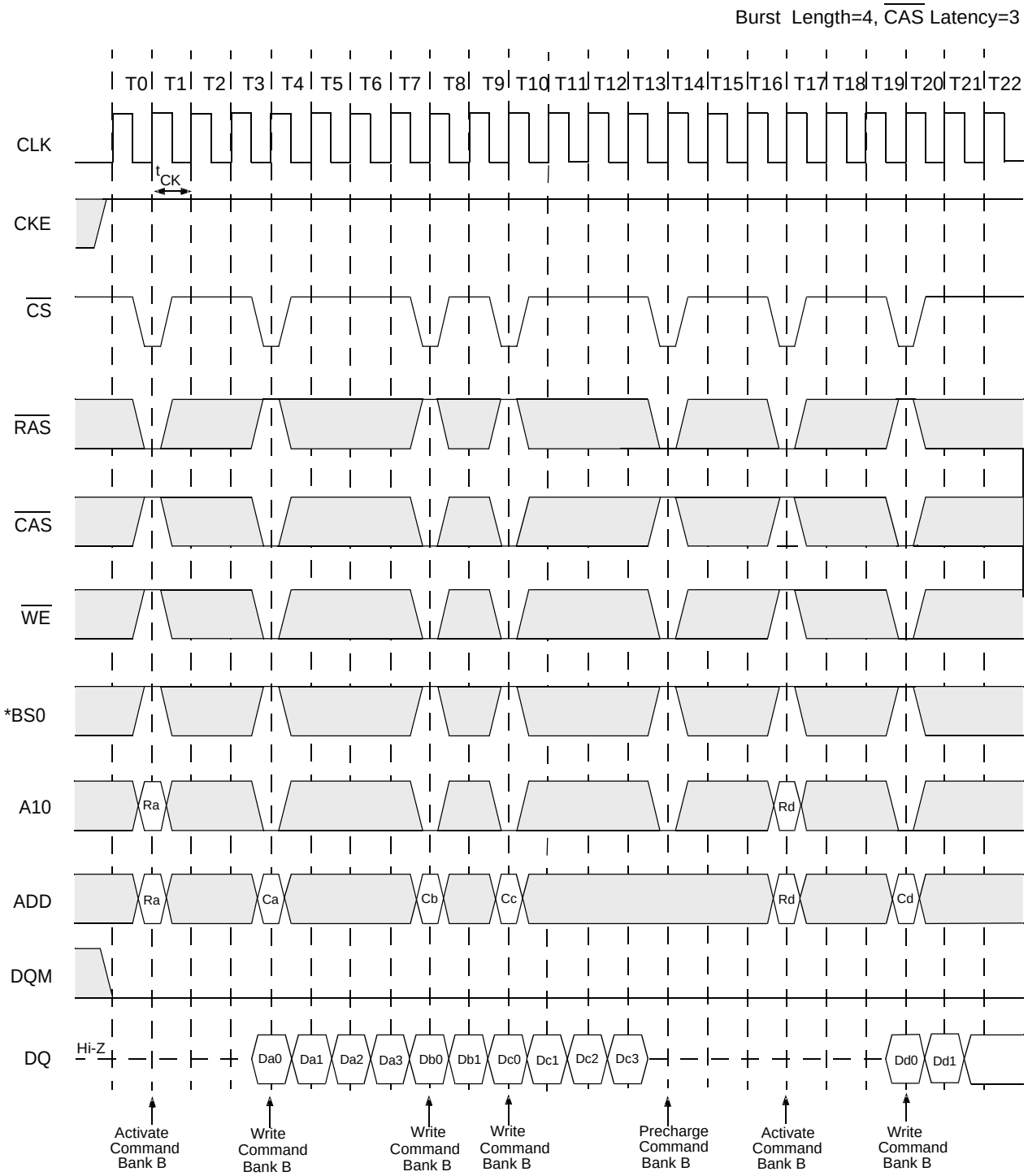
BS1="L", Bank C,D = Idle

Random Column Write (Page With Same Bank) (1 of 2)



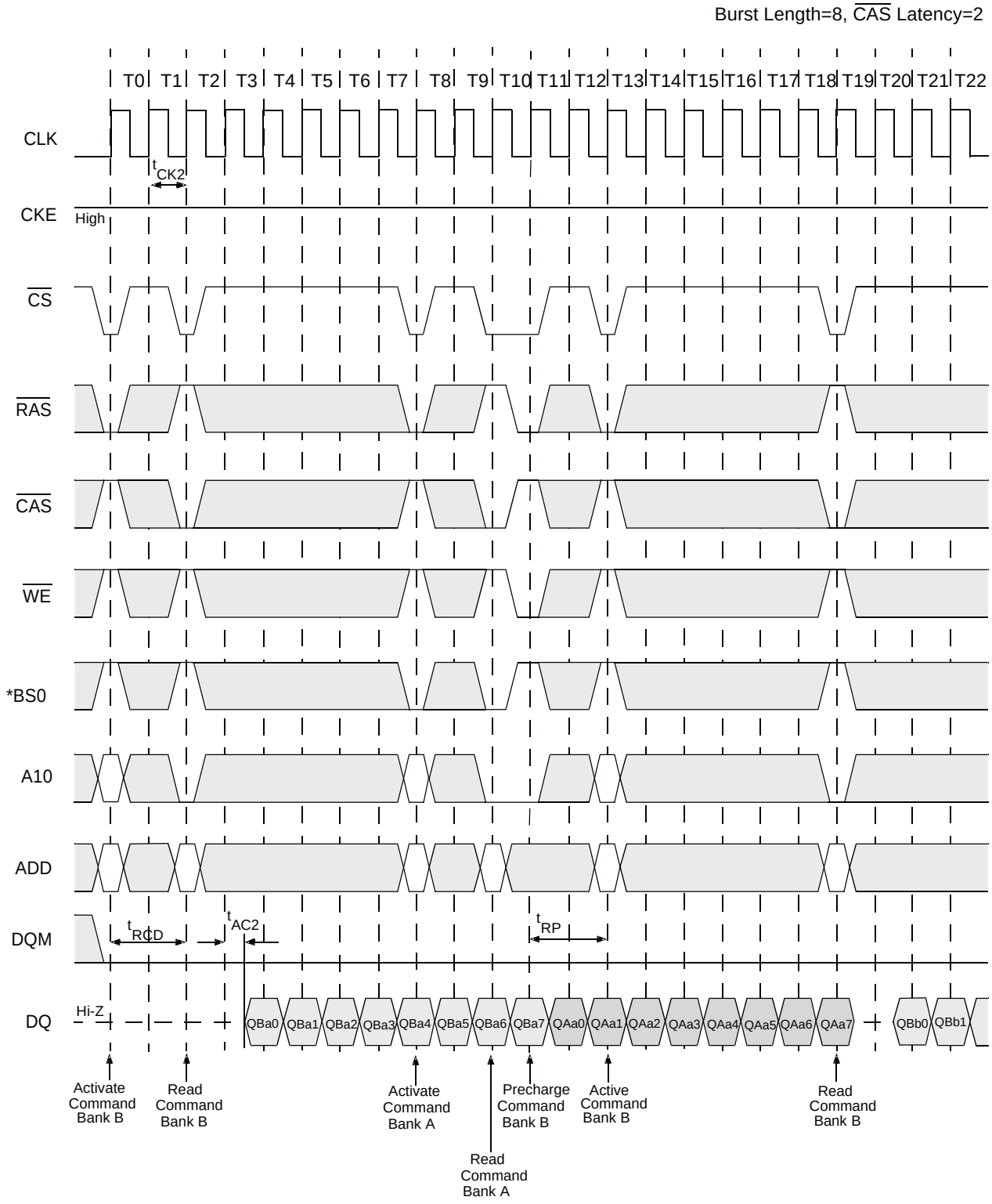
BS1="L", Bank C,D = Idle

Random Column Write (Page With Same Bank) (1 of 2)



BS1="L", Bank C,D = Idle

Random Row Read (Interleaving Banks) (1 of 2)

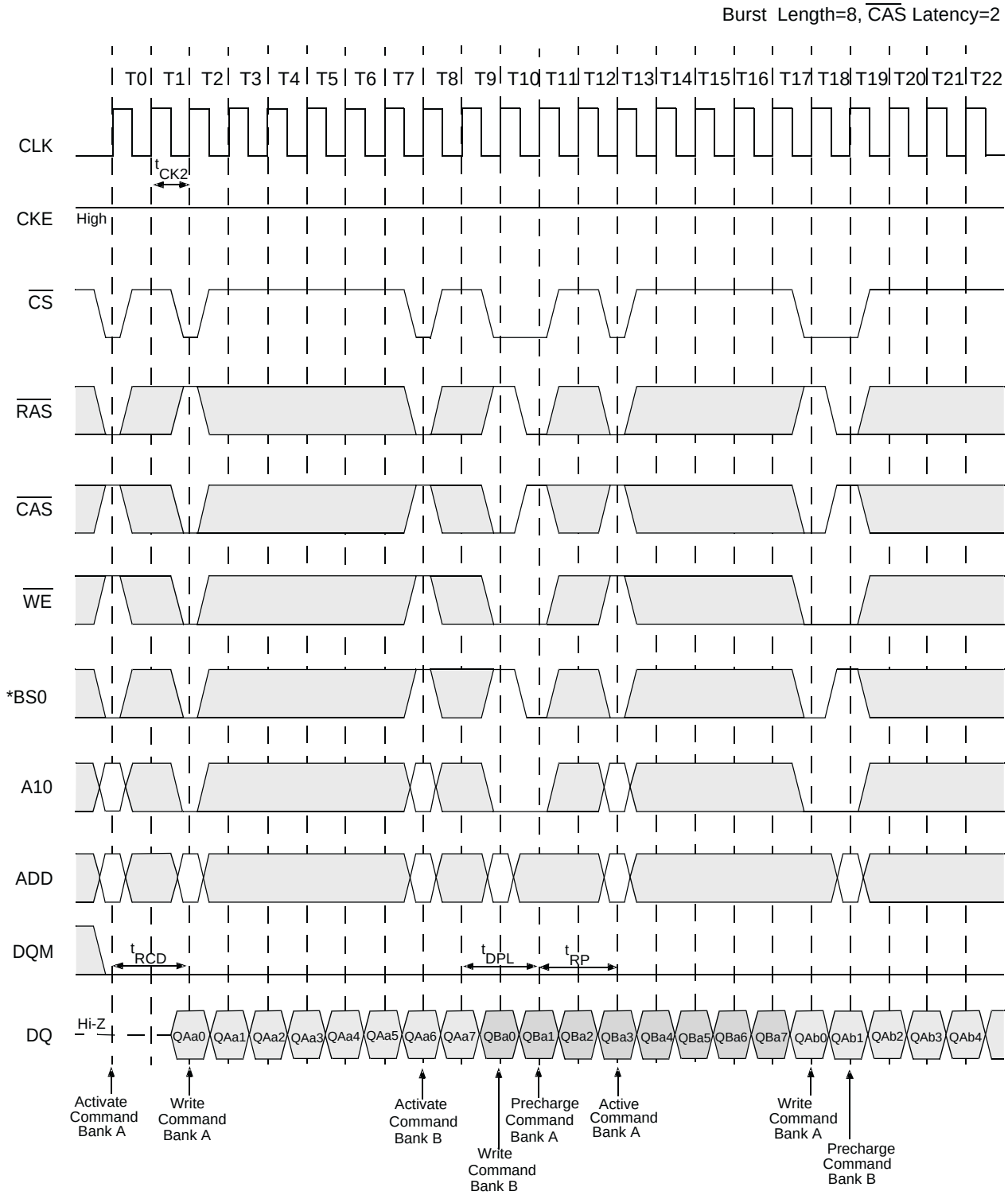


BS1="L", Bank C,D = Idle

Random Row Read (Interleaving Banks) (2 of 2)

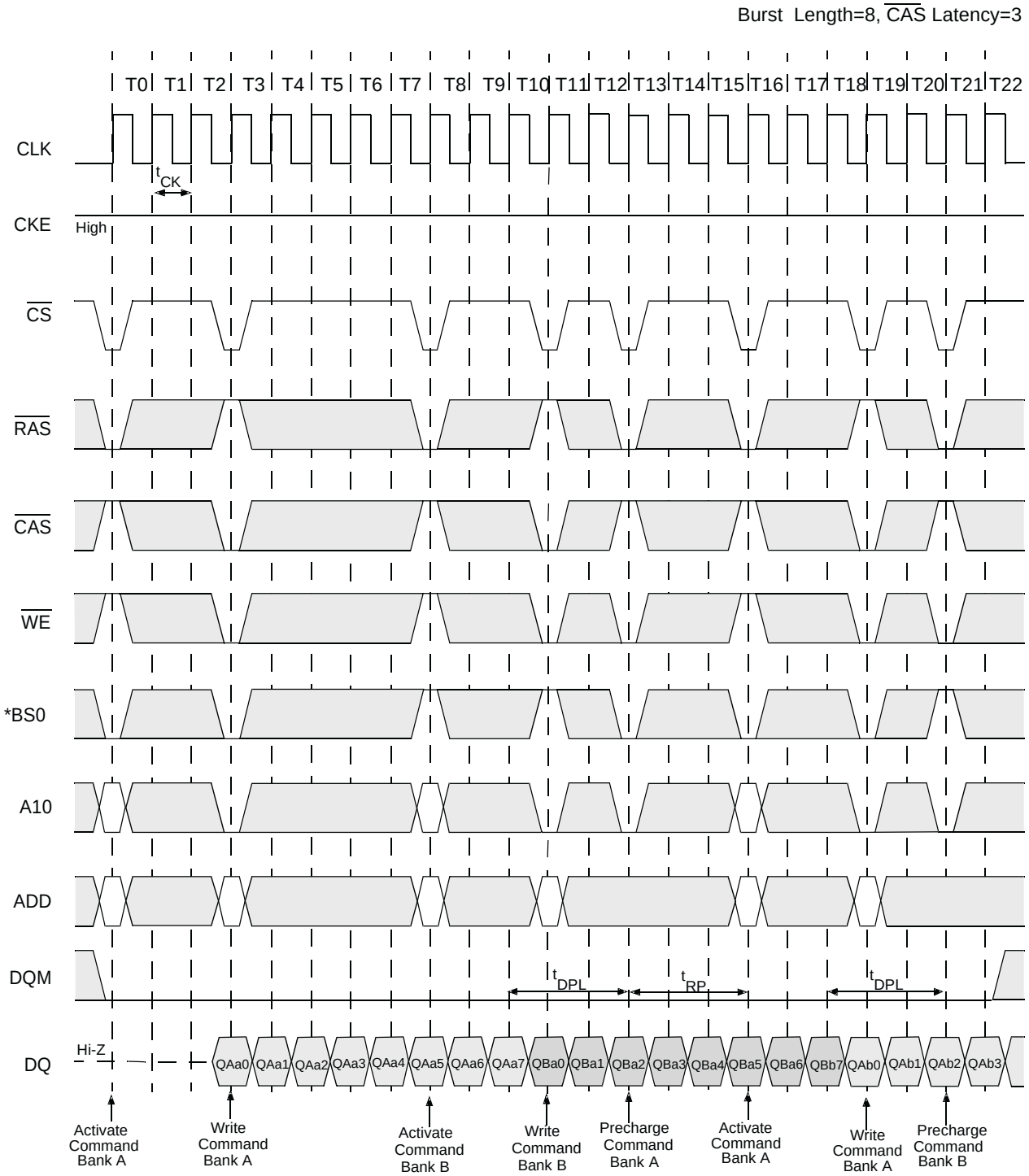
BS1="L", Bank C,D = Idle

Random Row Write (Interleaving Banks) (1 of 2)



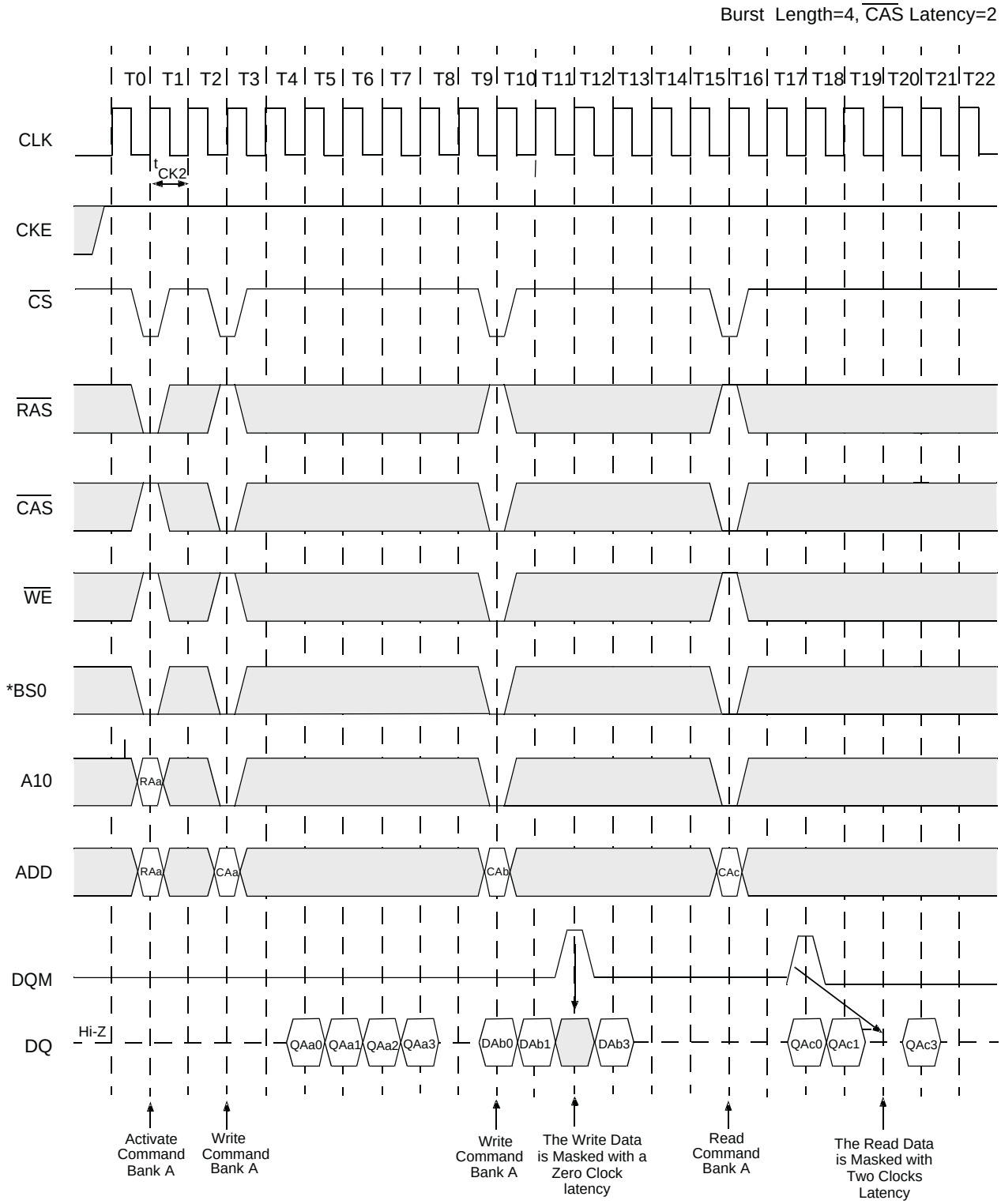
BS1="L", Bank C,D = Idle

Random Row Write (Interleaving Banks) (2 of 2)



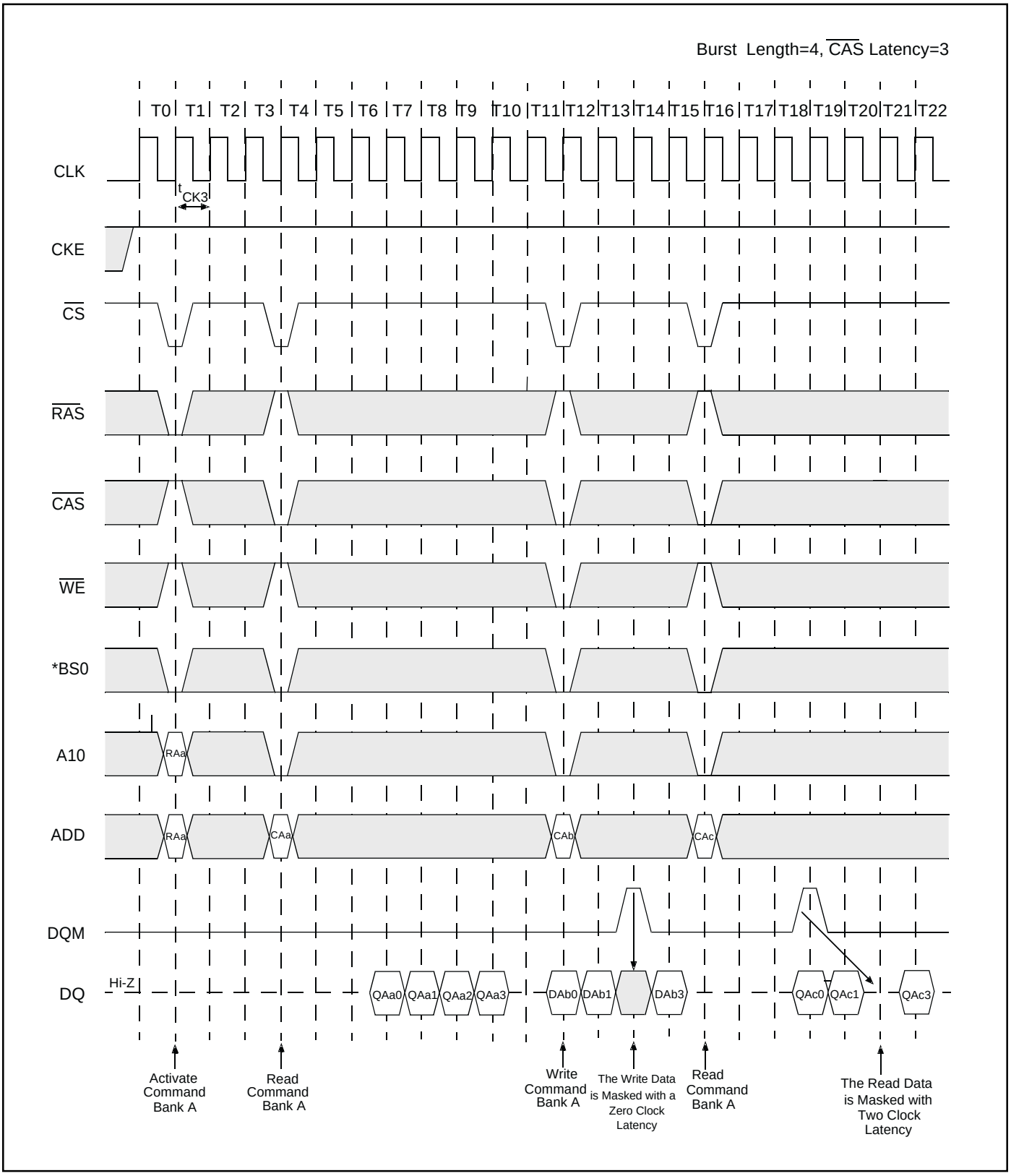
BS1="L", Bank C,D = Idle

Read and Write Cycle (1 of 2)



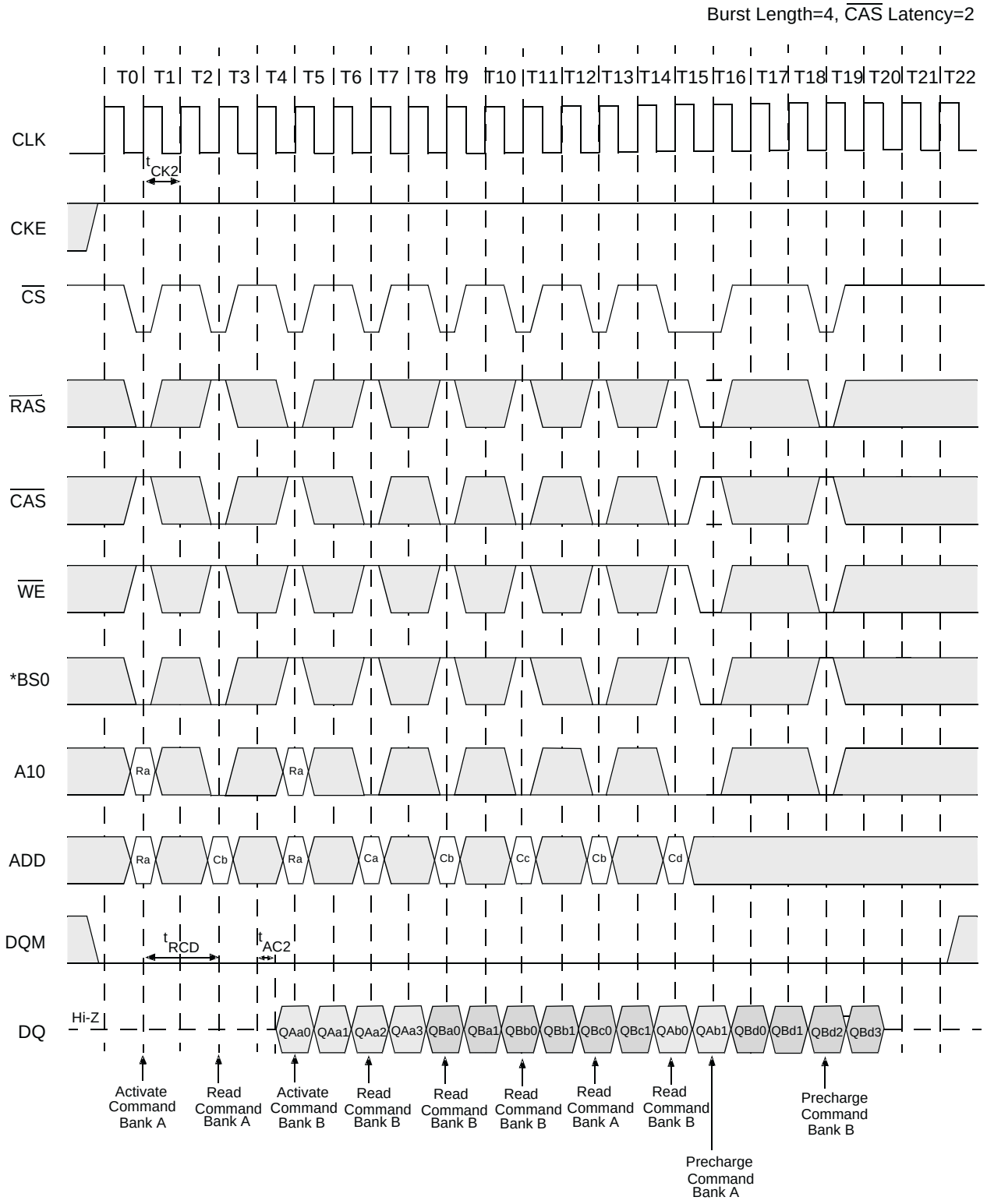
BS1="L", Bank C,D = Idle

Read and Write Cycle (2 of 2)



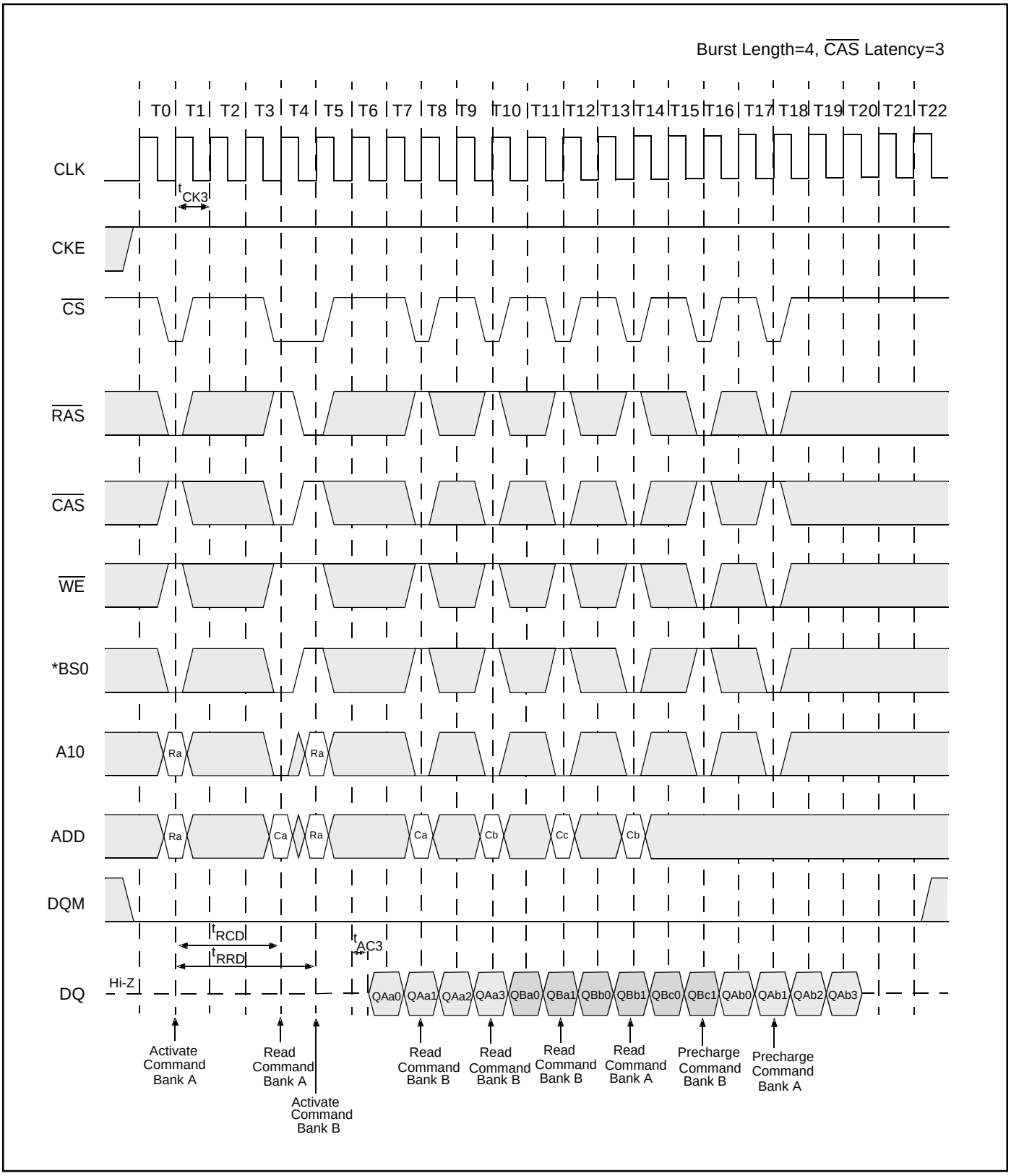
BS1="L", Bank C,D = Idle

Interleaved Column Read Cycle (1 of 2)



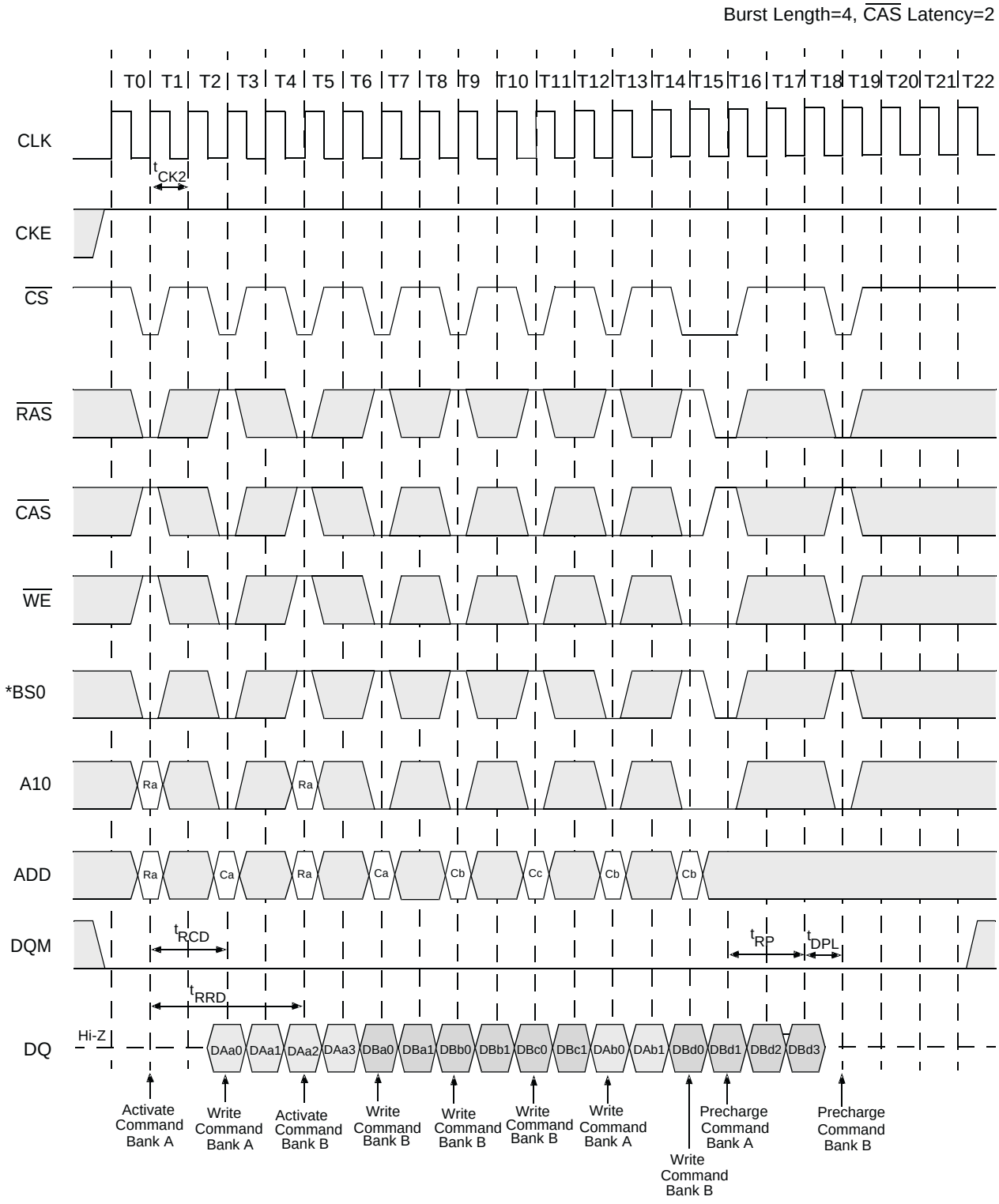
BS1="L", Bank C,D = Idle

Interleaved Column Read Cycle (2 of 2)



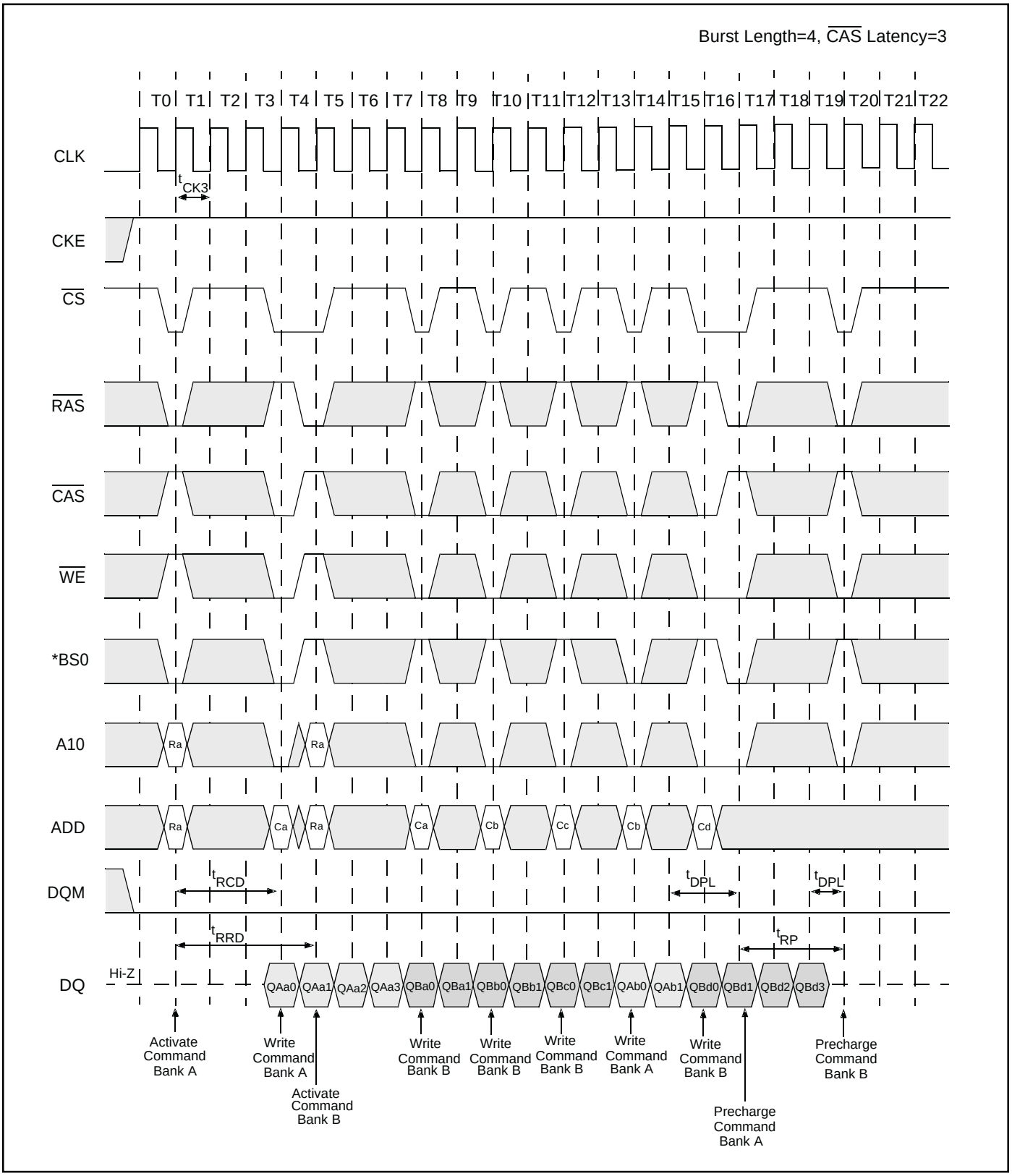
BS1="L", Bank C,D = Idle

Interleaved Column Write Cycle (1 of 2)



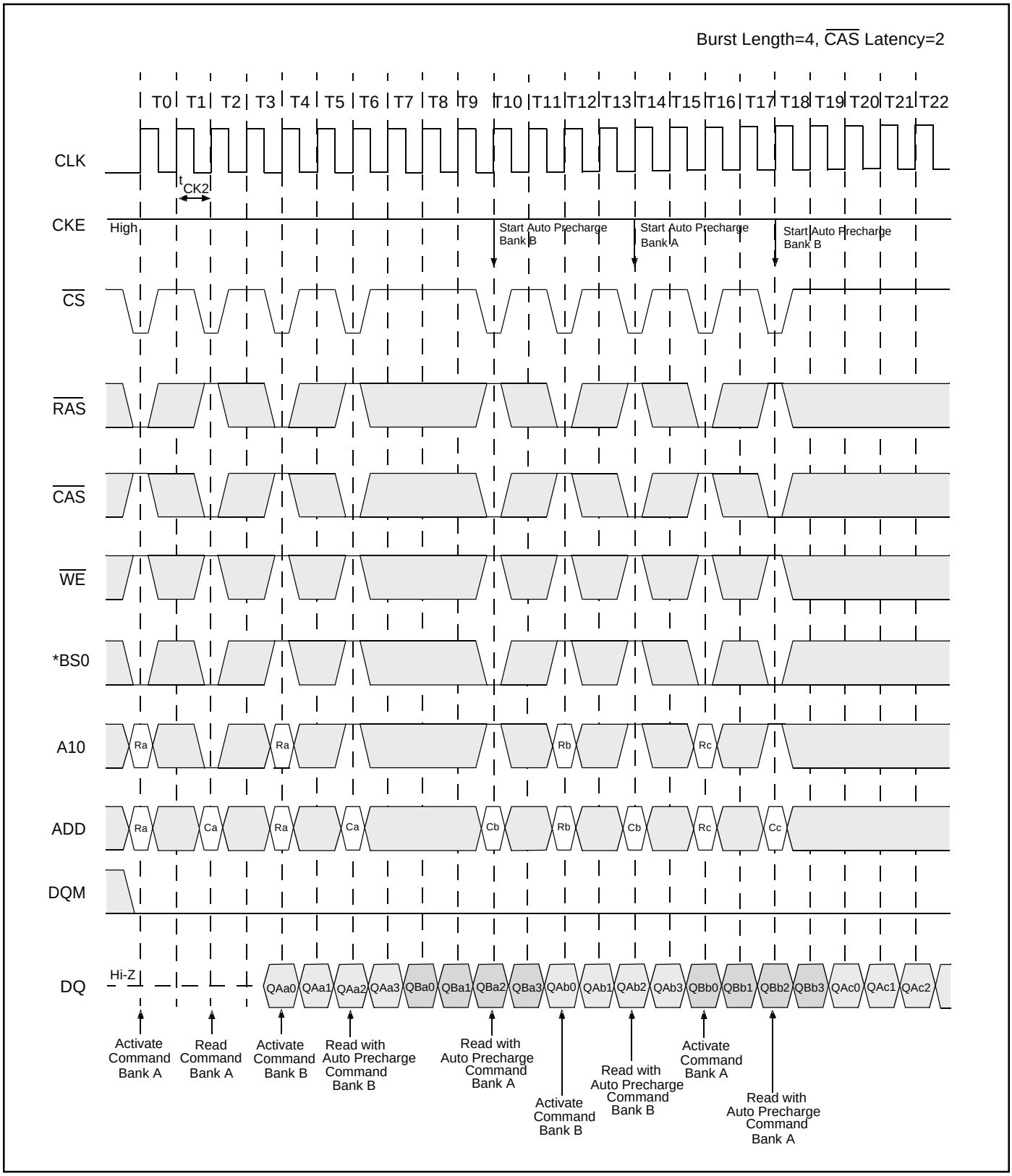
BS1="L", Bank C,D = Idle

Interleaved Column Write Cycle (2 of 2)



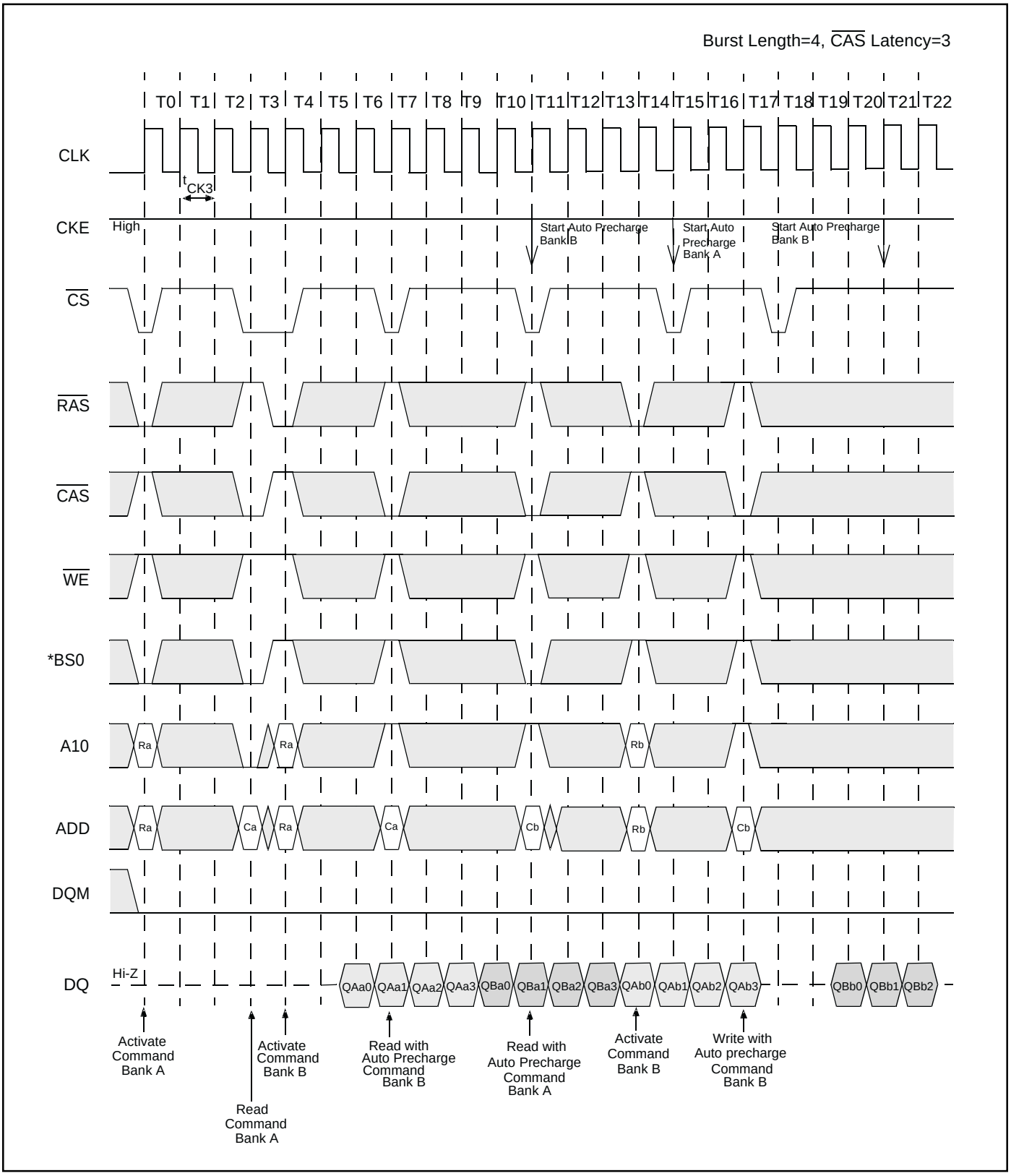
BS1="L", Bank C,D = Idle

Auto Precharge after Read Burst (1 of 2)



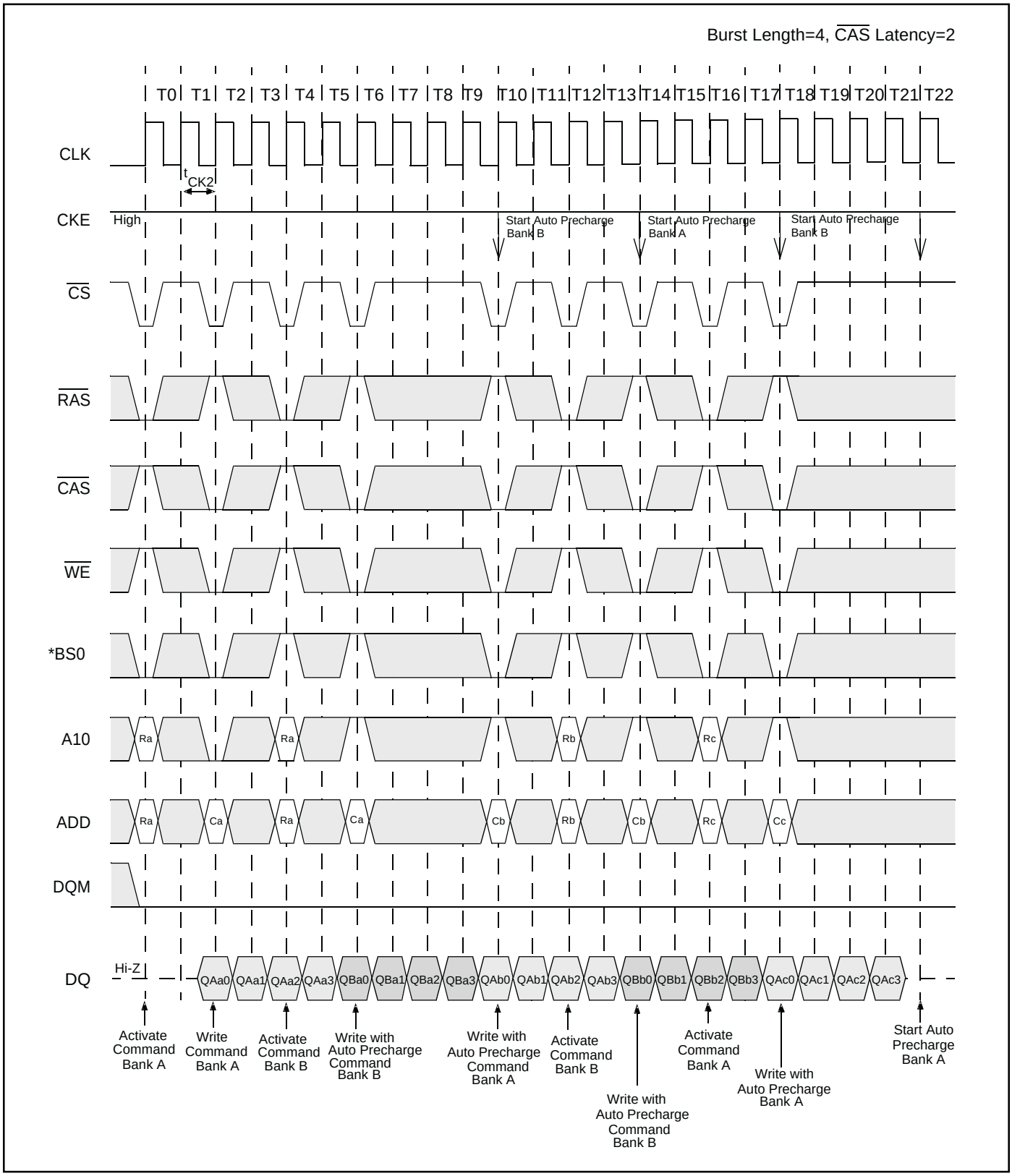
BS1="L", Bank C,D = Idle

Auto Precharge after Read Burst (2 of 2)



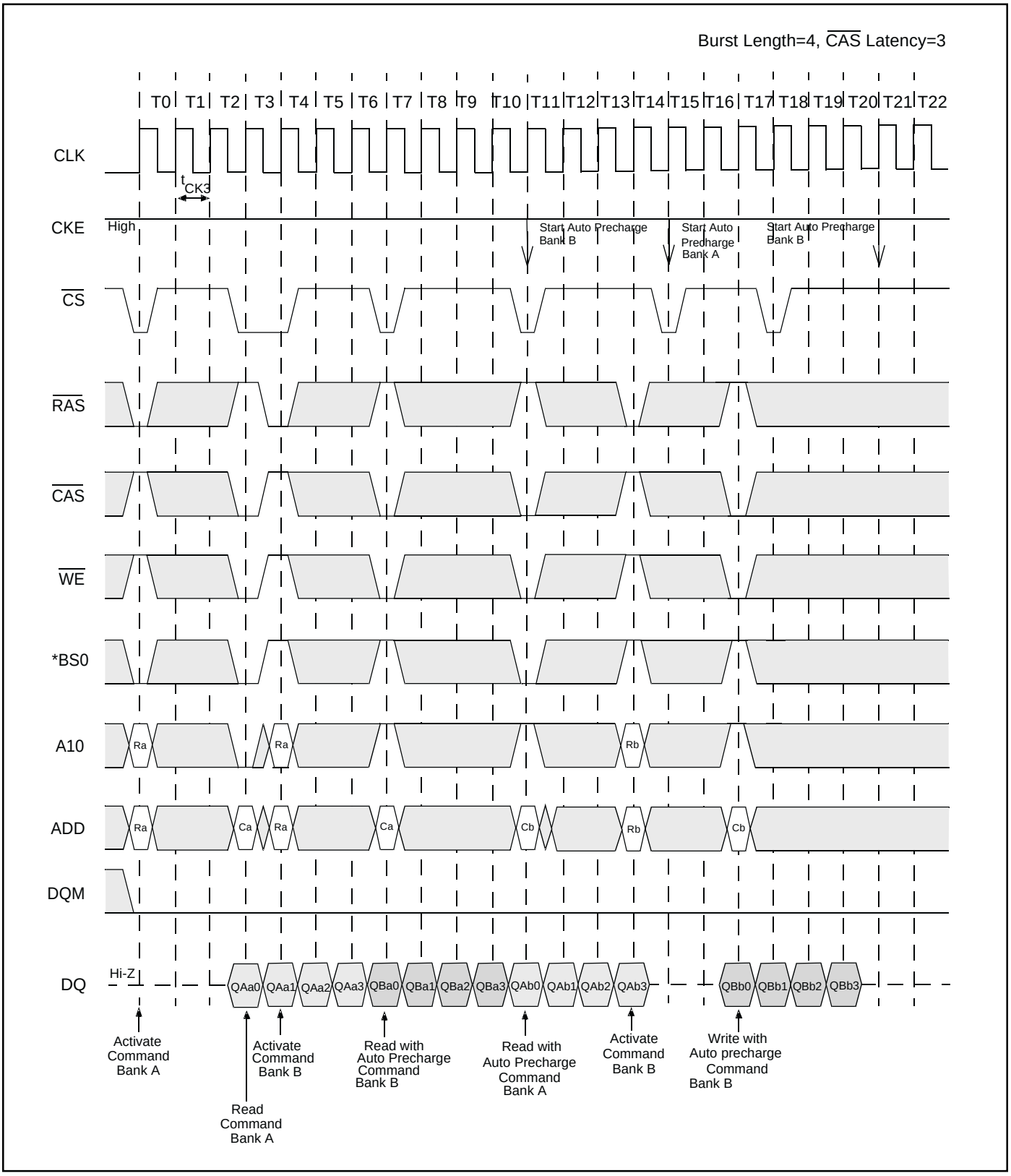
BS1="L", Bank C,D = Idle

Auto Precharge after Write Burst (1 of 2)



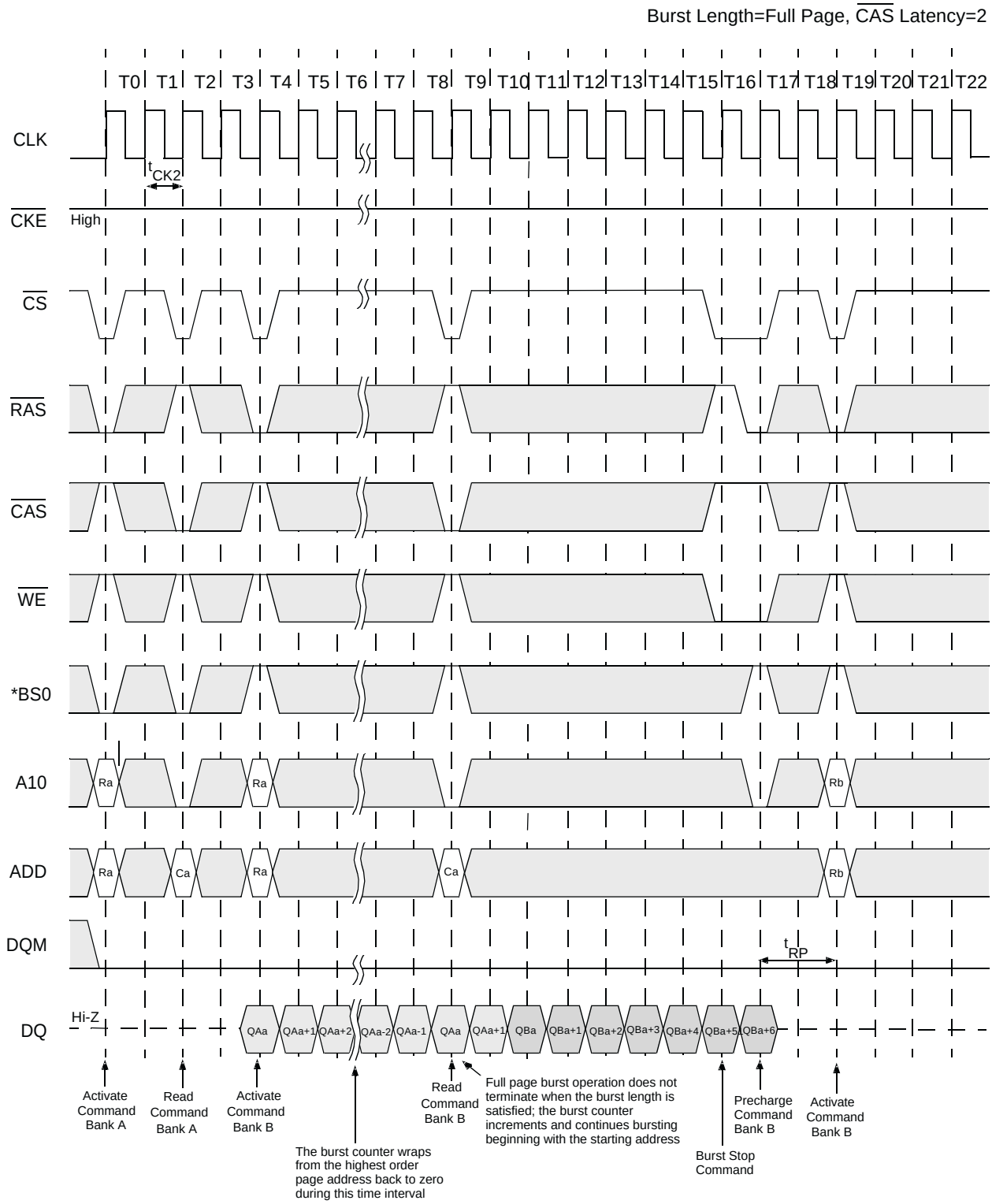
BS1="L", Bank C,D = Idle

Auto Precharge after Write Burst (2 of 2)



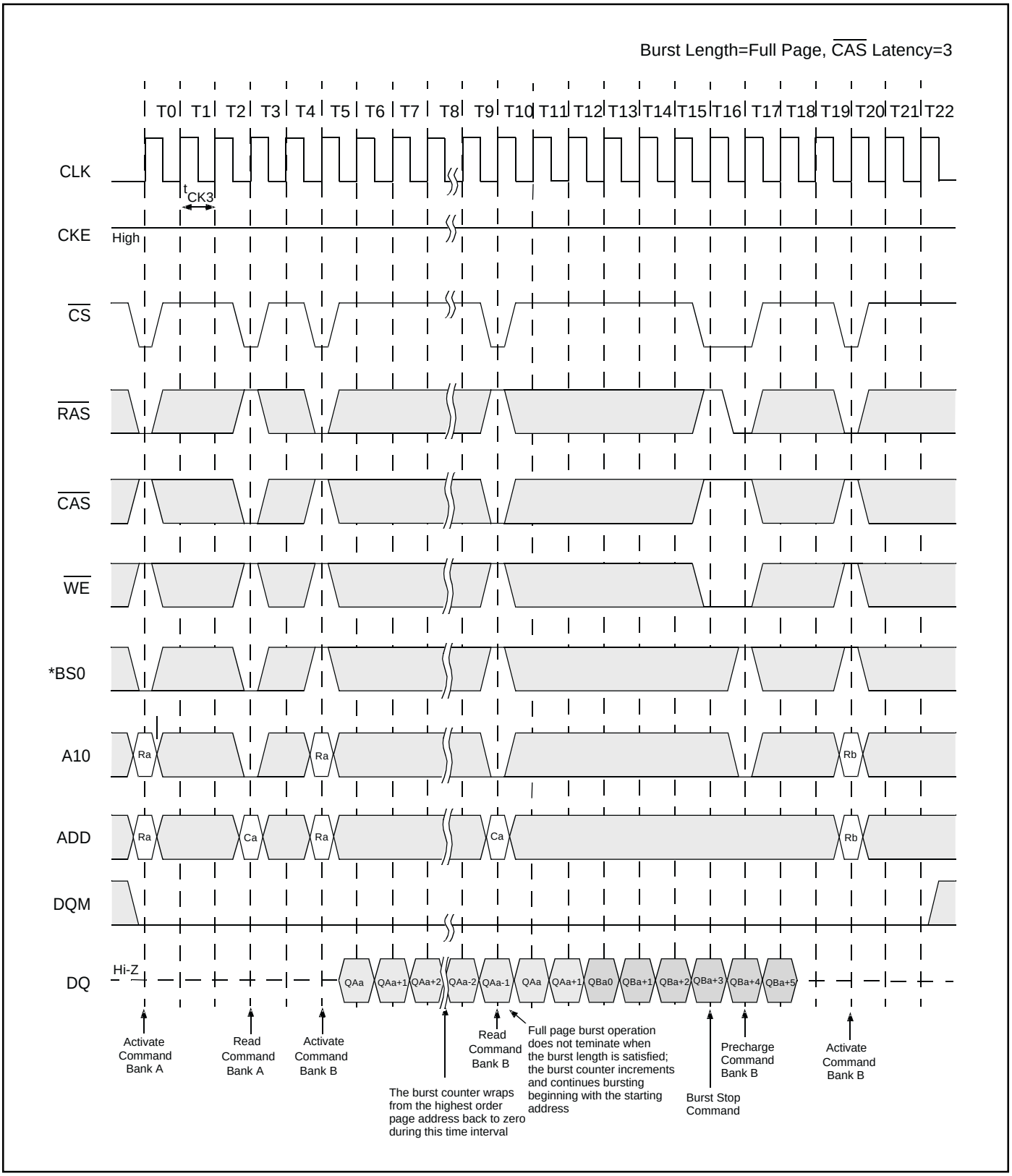
BS1="L", Bank C,D = Idle

Full Page Read Cycle (1 of 2)



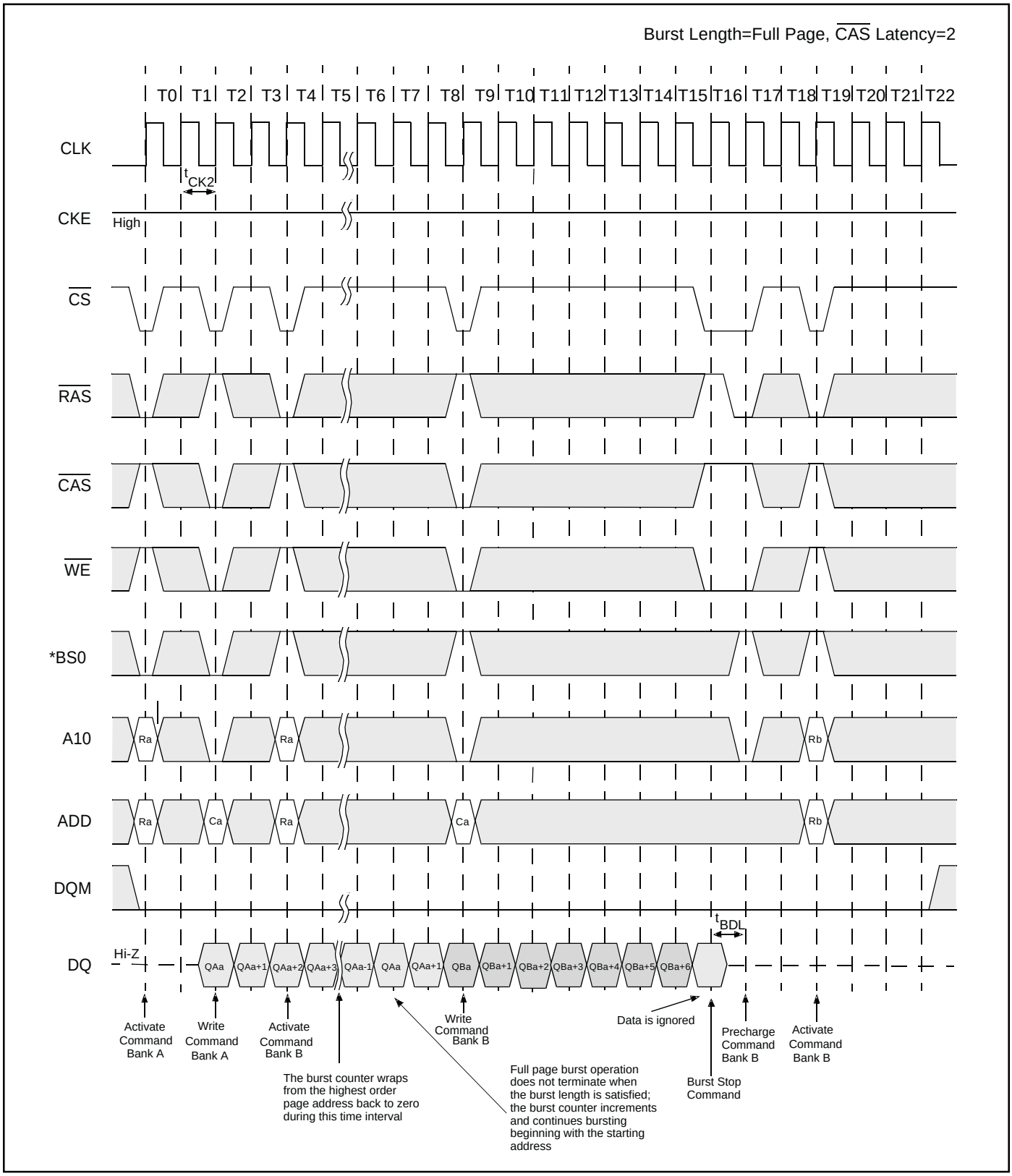
BS1="L", Bank C,D = Idle

Full Page Read Cycle (2 of 2)



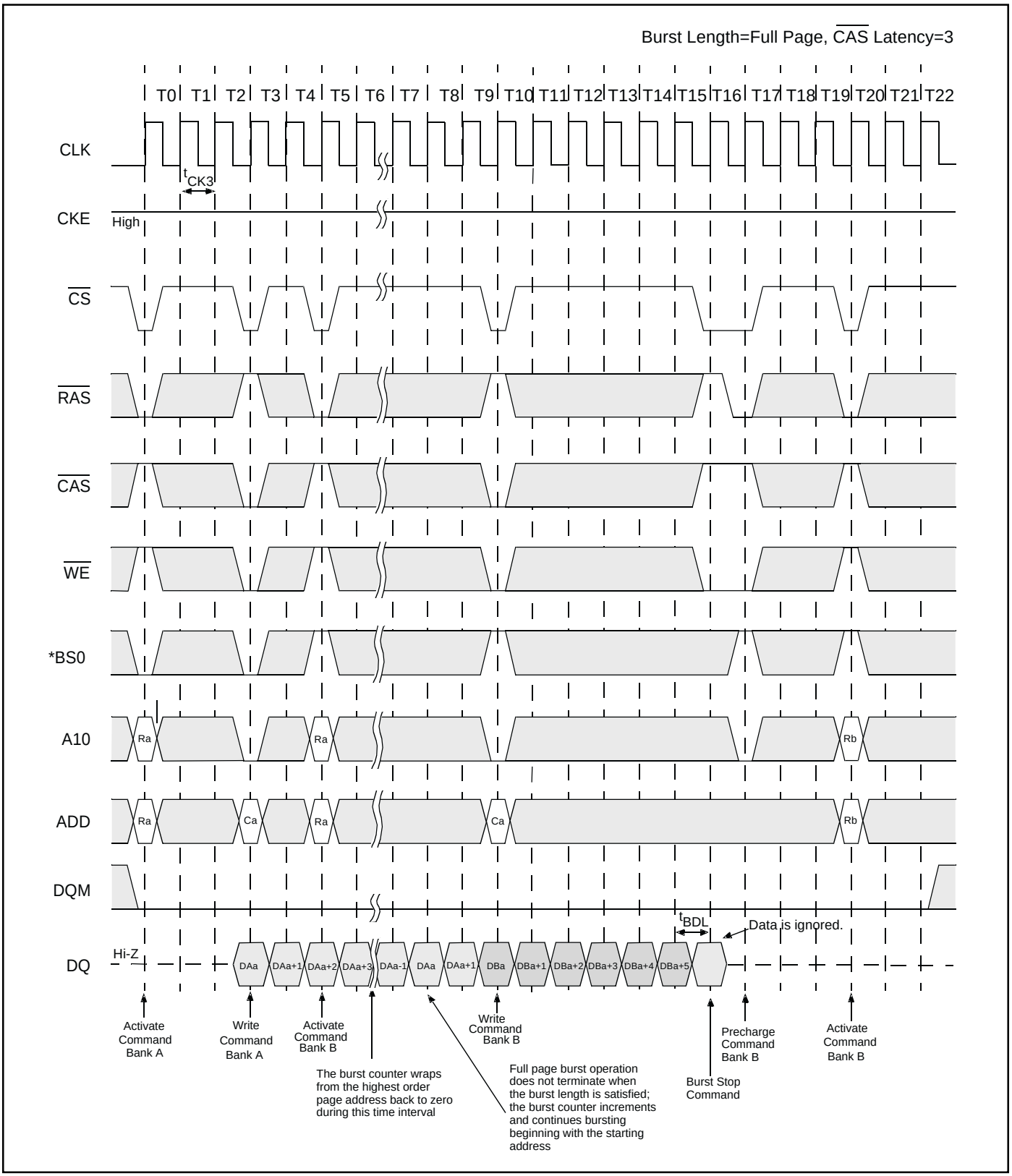
BS1="L", Bank C,D = Idle

Full Page Write Cycle (1 of 2)



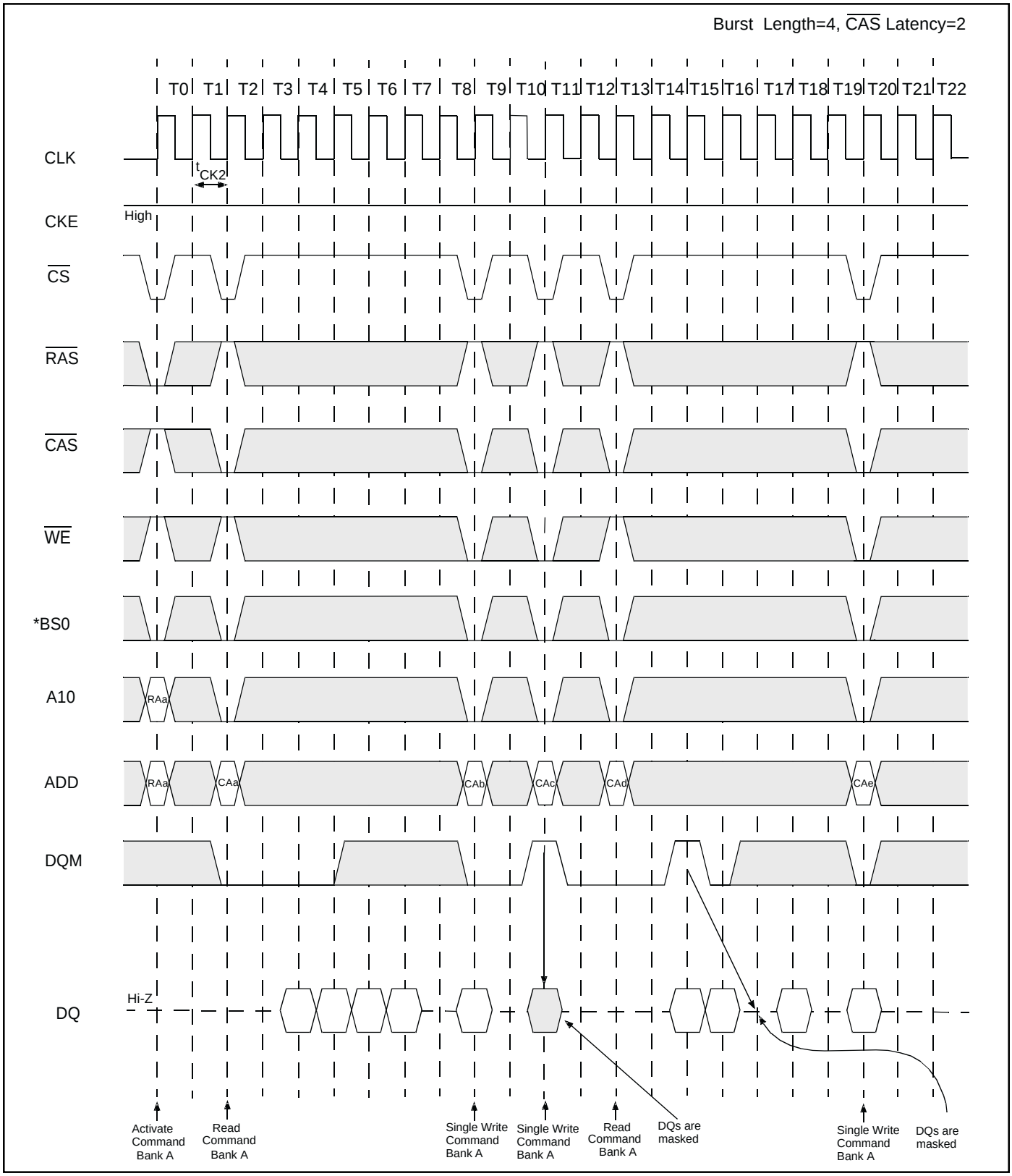
BS1="L", Bank C,D = Idle

Full Page Write Cycle (2 of 2)



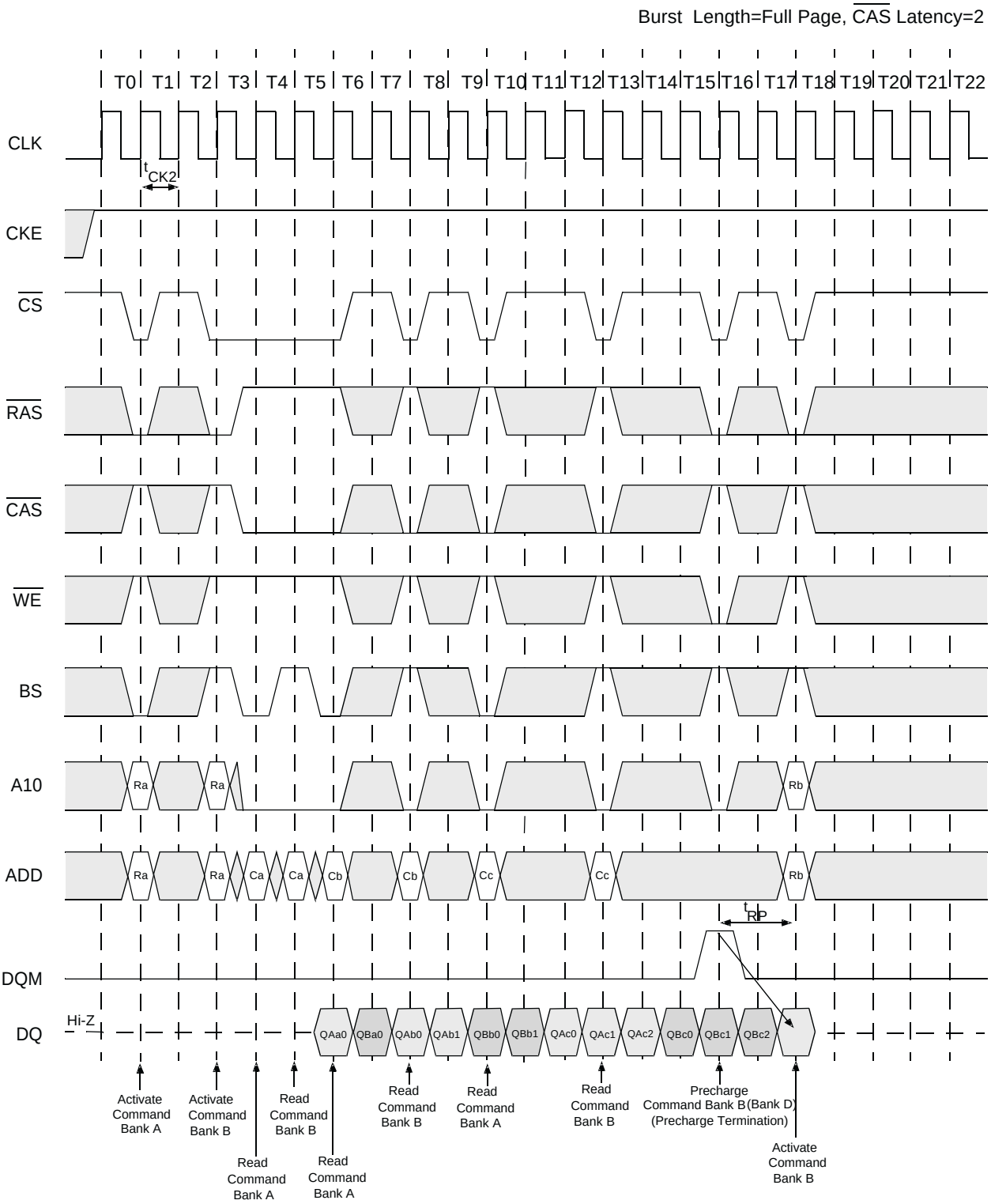
BS1="L", Bank C,D = Idle

Burst Read and Single Write Operation



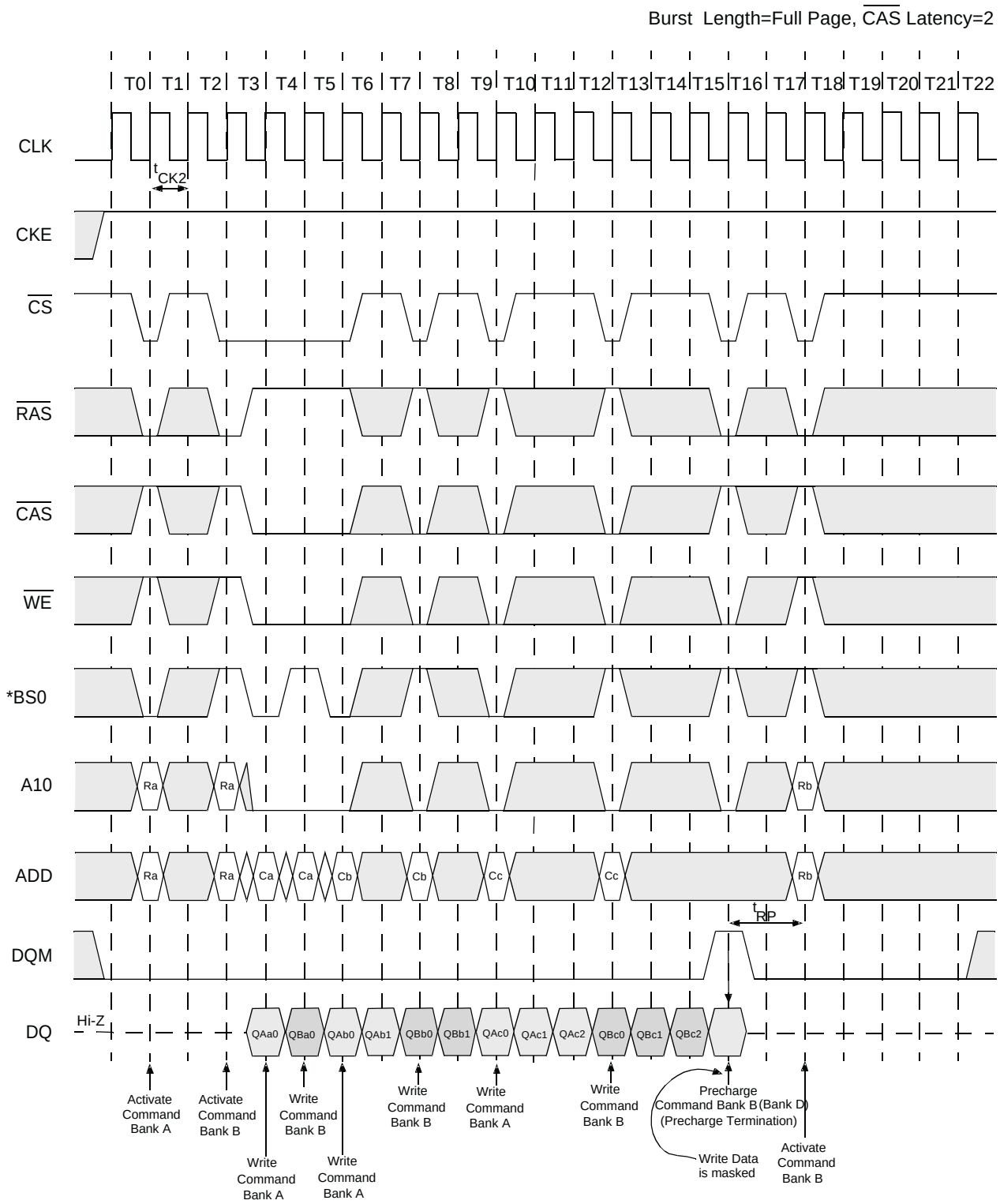
BS1="L", Bank C,D = Idle

Full Page Random Column Read



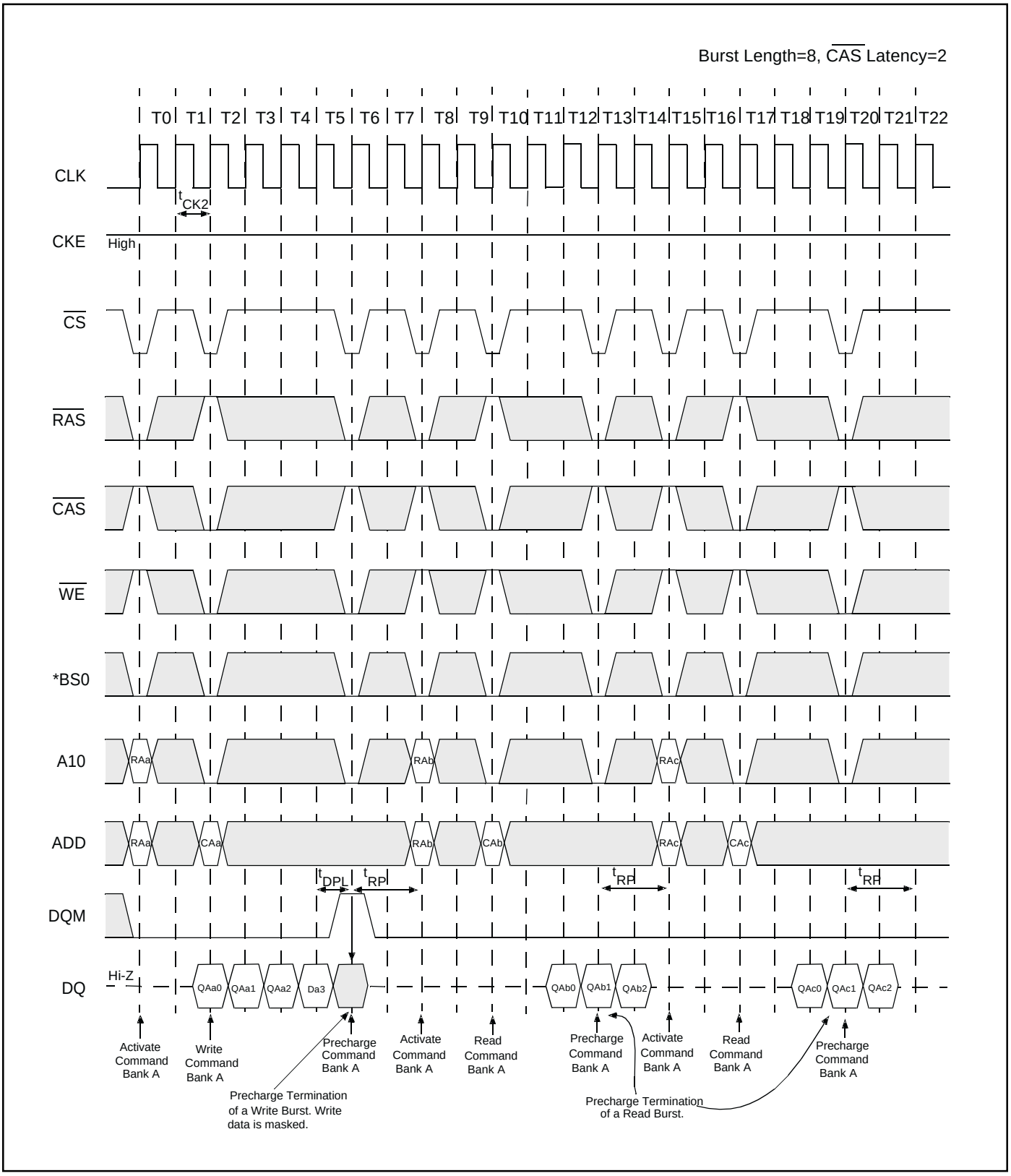
BS1="L", Bank C,D = Idle

Full Page Random Column Write



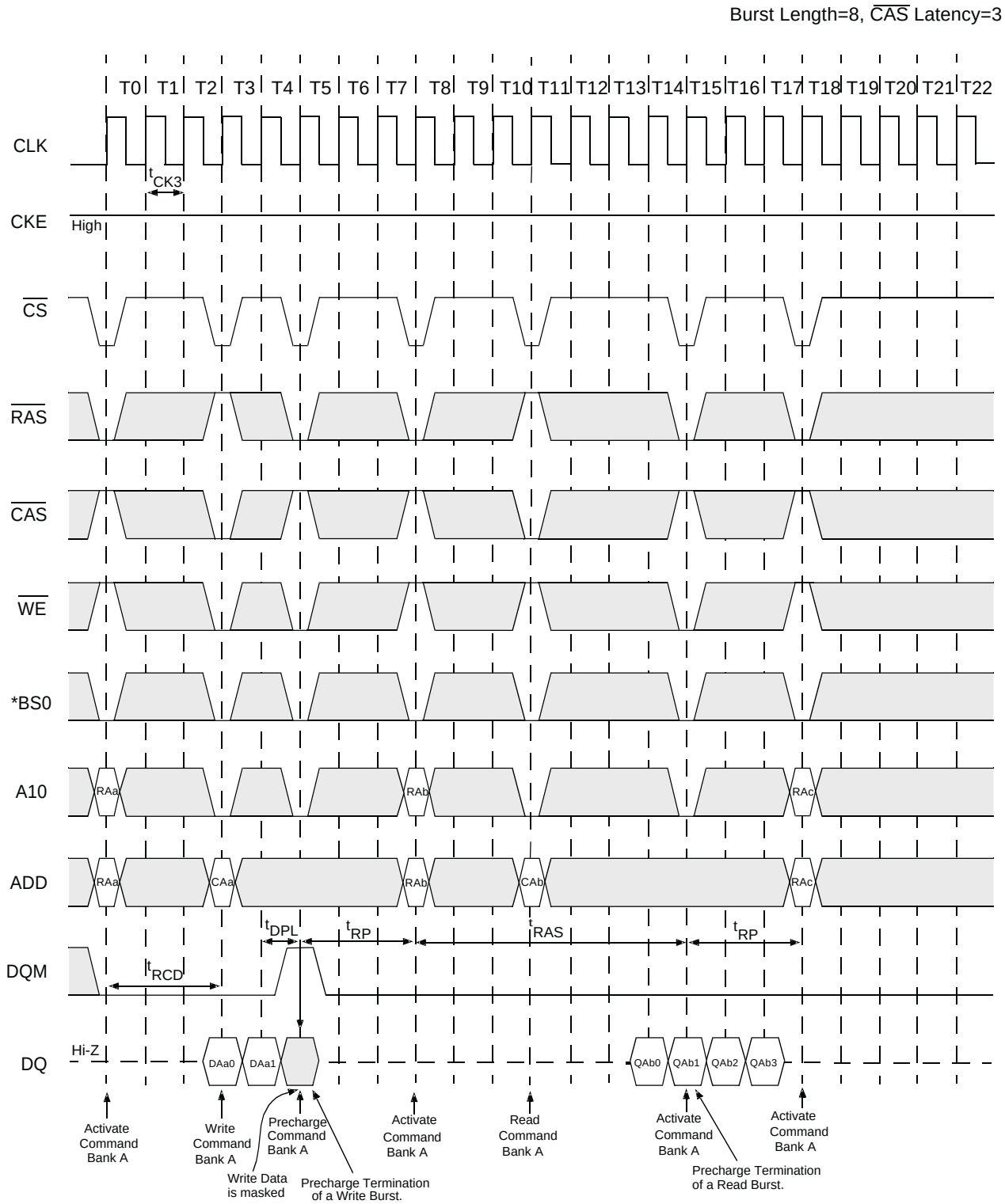
BS1="L", Bank C,D = Idle

Precharge Termination of a Burst (1 of 2)



BS1="L", Bank C,D = Idle

Precharge Termination of a Burst (2 of 2)



BS1="L", Bank C,D = Idle

ORDERING INFORMATION

Commercial Range: 0°C to 70°C

Speed (ns)	Order Part No.	Package
6	IC42S16400-6T	400mil TSOP-2
	IC42S16400-6TG	400mil TSOP-2(Pb-free)
	IC42S16400-6BG	60Ball VF-BGA(Pb-free)
7	IC42S16400-7T	400mil TSOP-2
	IC42S16400-7TG	400mil TSOP-2(Pb-free)
	IC42S16400-7BG	60Ball VF-BGA(Pb-free)

ORDERING INFORMATION

Industrial Temperature Range: -40°C to 85°C

Speed (ns)	Order Part No.	Package
6	IC42S16400-6TI	400mil TSOP-2
	IC42S16400-6TIG	400mil TSOP-2(Pb-free)
	IC42S16400-6BIG	60Ball VF-BGA(Pb-free)
7	IC42S16400-7TI	400mil TSOP-2
	IC42S16400-7TIG	400mil TSOP-2(Pb-free)
	IC42S16400-7BIG	60Ball VF-BGA(Pb-free)

Integrated Circuit Solution Inc.
HEADQUARTER:
NO.2, TECHNOLOGY RD. V, SCIENCE-BASED INDUSTRIAL PARK,
HSIN-CHU, TAIWAN, R.O.C.
TEL: 886-3-5780333
Fax: 886-3-5783000

BRANCH OFFICE:
7F, NO. 106, SEC. 1, HSIN-TAI 5TH ROAD,
HSICHIH TAIPEI COUNTY, TAIWAN, R.O.C.
TEL: 886-2-26962140
FAX: 886-2-26962252
http://www.icsi.com.tw