

**ADC71**

## 16-Bit ANALOG-TO-DIGITAL CONVERTER

### FEATURES

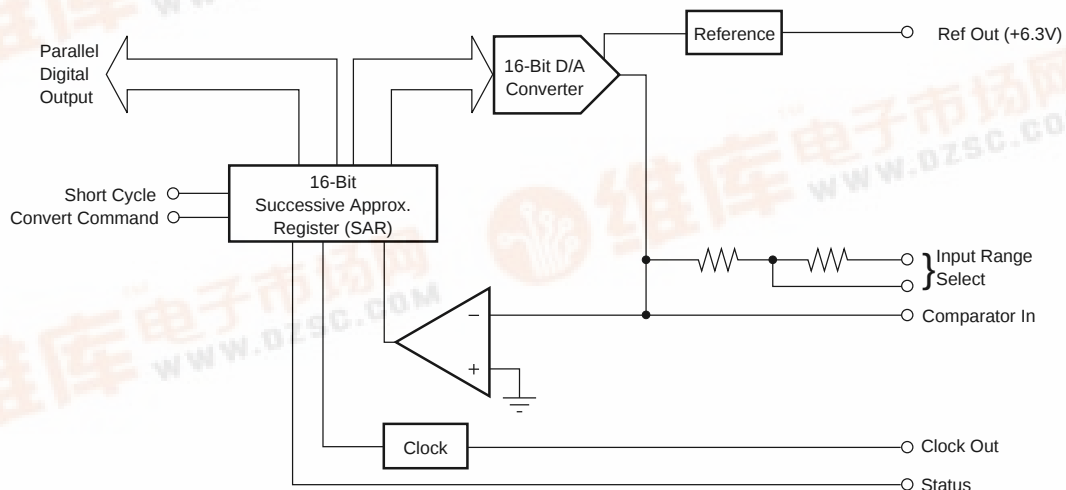
- **16-BIT RESOLUTION**
- **$\pm 0.003\%$  MAXIMUM NONLINEARITY**
- **COMPACT DESIGN: 32-pin Hermetic Ceramic Package**
- **CONVERSION SPEED:  $50\mu\text{s}$  max**

### DESCRIPTION

The ADC71 is a low cost, high quality, 16-bit successive approximation analog-to-digital converter. It uses laser-trimmed ICs and is packaged in a convenient 32-pin hermetic ceramic dual-in-line package. The converter is complete with internal reference, clock, comparator, and thin-film scaling resistors, which allow selection of analog input ranges of  $\pm 2.5\text{V}$ ,  $\pm 5\text{V}$ ,  $\pm 10\text{V}$ ,  $0$  to  $+5\text{V}$ ,  $0$  to  $+10\text{V}$  and  $0$  to  $+20\text{V}$ .

Data is available in parallel and serial form with corresponding clock and status output. All digital inputs and outputs are TTL-compatible.

Power supply voltages are  $\pm 15\text{VDC}$  and  $+5\text{VDC}$ .



# SPECIFICATIONS

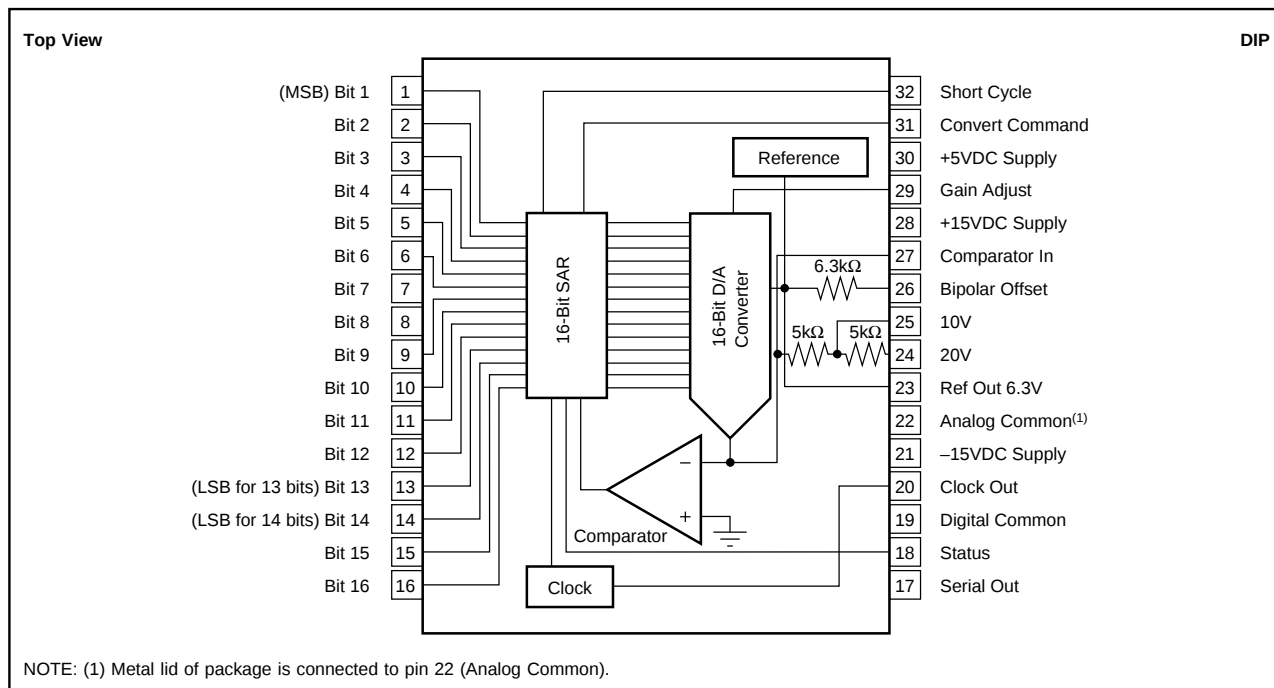
## ELECTRICAL

At +25°C and rated power supplies, unless otherwise noted.

| MODEL                                                                                                                                                                                                                                                                            | ADC71J, K                                                                                      |                                                                                              |                                          | ADC71A, B         |                                                                       |                                          | UNITS                                                                               |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------|------------------------------------------|-------------------|-----------------------------------------------------------------------|------------------------------------------|-------------------------------------------------------------------------------------|
|                                                                                                                                                                                                                                                                                  | MIN                                                                                            | TYP                                                                                          | MAX                                      | MIN               | TYP                                                                   | MAX                                      |                                                                                     |
| <b>RESOLUTION</b>                                                                                                                                                                                                                                                                |                                                                                                |                                                                                              | 16                                       |                   |                                                                       | 16                                       | Bits                                                                                |
| <b>INPUTS</b><br><b>ANALOG</b><br>Voltage Ranges: Bipolar<br>Unipolar<br><br>Input Impedance (Direct Input)<br>0 to +5V, ±2.5V<br>0 to +10V, ±5.0V<br>0 to +20V, ±10V                                                                                                            |                                                                                                | ±2.5, ±5, ±10<br>0 to +5, 0 to +10,<br>0 to +20<br><br>2.5<br>5<br>10                        |                                          |                   | ±2.5, ±5, ±10<br>0 to +5, 0 to +10,<br>0 to +20<br><br>2.5<br>5<br>10 |                                          | V<br>V<br><br>kΩ<br>kΩ<br>kΩ                                                        |
| <b>DIGITAL<sup>(4)</sup></b>                                                                                                                                                                                                                                                     | Convert Command Positive pulse 50ns wide (min) trailing edge ("1" to "0" initiates conversion) |                                                                                              |                                          |                   |                                                                       |                                          |                                                                                     |
| Logic Loading                                                                                                                                                                                                                                                                    |                                                                                                |                                                                                              | 1                                        |                   |                                                                       |                                          | TTL Load                                                                            |
| <b>TRANSFER CHARACTERISTICS</b><br><b>ACCURACY</b><br>Gain Error <sup>(2)</sup><br>Offset <sup>(2)</sup> : Unipolar<br>Bipolar<br>Linearity Error: K, B<br>J, A<br>Inherent Quantization Error<br>Differential Linearity Error                                                   |                                                                                                | ±0.1<br>±0.05<br>±0.1<br><br>±1/2<br>±0.003                                                  | ±0.2<br>±0.1<br>±0.2<br>±0.003<br>±0.006 |                   | ±0.1<br>±0.05<br>±0.1<br><br>±1/2<br>±0.003                           | ±0.2<br>±0.1<br>±0.2<br>±0.003<br>±0.006 | %<br>% of FSR <sup>(3)</sup><br>% of FSR<br>% of FSR<br>% of FSR<br>LSB<br>% of FSR |
| <b>POWER SUPPLY SENSITIVITY</b><br>±15VDC<br>+5VDC                                                                                                                                                                                                                               |                                                                                                | 0.003<br>0.001                                                                               |                                          |                   | 0.003<br>0.001                                                        |                                          | % of FSR/%V <sub>S</sub><br>% of FSR/%V <sub>S</sub>                                |
| <b>CONVERSION TIME<sup>(4)</sup></b><br>14 Bits                                                                                                                                                                                                                                  |                                                                                                |                                                                                              | 50                                       |                   |                                                                       | 50                                       | μs                                                                                  |
| <b>WARM-UP TIME</b>                                                                                                                                                                                                                                                              | 5                                                                                              |                                                                                              |                                          | *                 |                                                                       |                                          | min                                                                                 |
| <b>DRIFT</b><br>Gain<br>Offset: Unipolar<br>Bipolar<br>Linearity<br>No Missing Codes Temp Range<br>J, A (13 Bits)<br>K, B (14 Bits)                                                                                                                                              |                                                                                                | ±10<br>±2<br>±8<br>±2<br><br>0<br>0                                                          | ±15<br>±4<br>±10<br>±3<br><br>+70<br>+70 |                   | *<br><br>±5<br><br><br>-25<br>-25                                     | *<br><br>±10<br>±2<br><br>+85<br>+85     | ppm/°C<br>ppm of FSR/°C<br>ppm of FSR/°C<br>ppm of FSR/°C<br><br>°C<br>°C           |
| <b>OUTPUT</b><br><b>DIGITAL DATA</b><br>(All Codes Complementary)<br>Parallel Output Codes <sup>(5)</sup> : Unipolar<br>Bipolar<br><br>Output Drive<br>Serial Data Code (NRZ)<br>Output Drive<br>Status<br>Status Output Drive<br>Clock Output Drive<br>Frequency <sup>(7)</sup> |                                                                                                | CSB<br>COB, CTC <sup>(6)</sup><br><br>CSB, COB<br><br>Logic "1" During Conversion<br><br>280 | 2<br><br>2<br><br>2<br>2                 |                   |                                                                       | *<br><br>*<br>2<br>2                     | TTL Loads<br><br>TTL Loads<br><br>TTL Loads<br>TTL Loads<br>kHz                     |
| <b>INTERNAL REFERENCE VOLTAGE</b><br>Max External Current with<br>No Degradation of Specs<br>Temp Coefficient                                                                                                                                                                    | 6.0                                                                                            | 6.3                                                                                          | 6.6<br><br>±200<br>±10                   | 6.0               | 6.3                                                                   | 6.6<br><br>±200<br>*                     | V<br><br>μA<br>ppm/°C                                                               |
| <b>POWER SUPPLY REQUIREMENTS</b><br>Power Consumption<br>Rated Voltage, Analog<br>Rated Voltage, Digital<br>Supply Drain +15VDC<br>Supply Drain -15VDC<br>Supply Drain +5VDC                                                                                                     | ±11.4<br>+4.75                                                                                 | 655<br>±15<br>+5<br>+10<br>-28<br>+17                                                        | ±16<br>+4.75<br>+15<br>-35<br>+20        | *<br>*            | 655<br>*<br>*<br>*<br>*<br>*                                          | *<br>*<br>*<br>*<br>*                    | mW<br>VDC<br>VDC<br>mA<br>mA<br>mA                                                  |
| <b>TEMPERATURE RANGE</b><br>Specification<br>Operating (Derated Specs)<br>Storage                                                                                                                                                                                                | 0<br>-25<br>-55                                                                                |                                                                                              | +70<br>+85<br>+125                       | -25<br>-55<br>-55 |                                                                       | +85<br>+125<br>+125                      | °C<br>°C<br>°C                                                                      |

NOTES: (1) CMOS/TTL compatible, i.e., Logic "0" = 0.8V, max Logic "1" = 2.0V, min for inputs. For digital outputs Logic "0" = +0.4V, max Logic "1" = 2.4V min.  
(2) Adjustable to zero. (3) FSR means Full Scale Range. For example, unit connected for ±10V range has 20V FSR. (4) Conversion time may be shortened with "Short Cycle" set for lower resolution, see "Additional Connections Required" section. (5) See Table I. CSB = Complementary Straight Binary. COB = Complementary Offset Binary. CTC = Complementary Two's Complement. (6) CTC coding obtained by inverting MSB (Pin 1).

## PIN CONFIGURATION



## ABSOLUTE MAXIMUM SPECIFICATIONS

|                                 |                       |
|---------------------------------|-----------------------|
| +V <sub>CC</sub> to Common      | 0 to +16.5V           |
| -V <sub>CC</sub> to Common      | 0V to -16.5V          |
| +V <sub>DD</sub> to Common      | 0V to +7V             |
| Analog Common to Digital Common | ±0.5V                 |
| Logic Inputs to Common          | 0V to V <sub>DD</sub> |
| Maximum Power Dissipation       | 1000mW                |
| Lead Temperature (10s)          | 300°C                 |

## PACKAGE INFORMATION

| MODEL   | PACKAGE             | PACKAGE DRAWING NUMBER <sup>(1)</sup> |
|---------|---------------------|---------------------------------------|
| ADC71JG | 32-Pin Hermetic DIP | 172-5                                 |
| ADC71KG | 32-Pin Hermetic DIP | 172-5                                 |
| ADC71AG | 32-Pin Hermetic DIP | 172-5                                 |
| ADC71BG | 32-Pin Hermetic DIP | 172-5                                 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

## ORDERING INFORMATION

| MODEL   | TEMPERATURE RANGE | NONLINEARITY |
|---------|-------------------|--------------|
| ADC71JG | 0°C to +70°C      | ±0.006% FSR  |
| ADC71KG | 0°C to +70°C      | ±0.003% FSR  |
| ADC71AG | -25°C to +85°C    | ±0.006% FSR  |
| ADC71BG | -25°C to +85°C    | ±0.003% FSR  |

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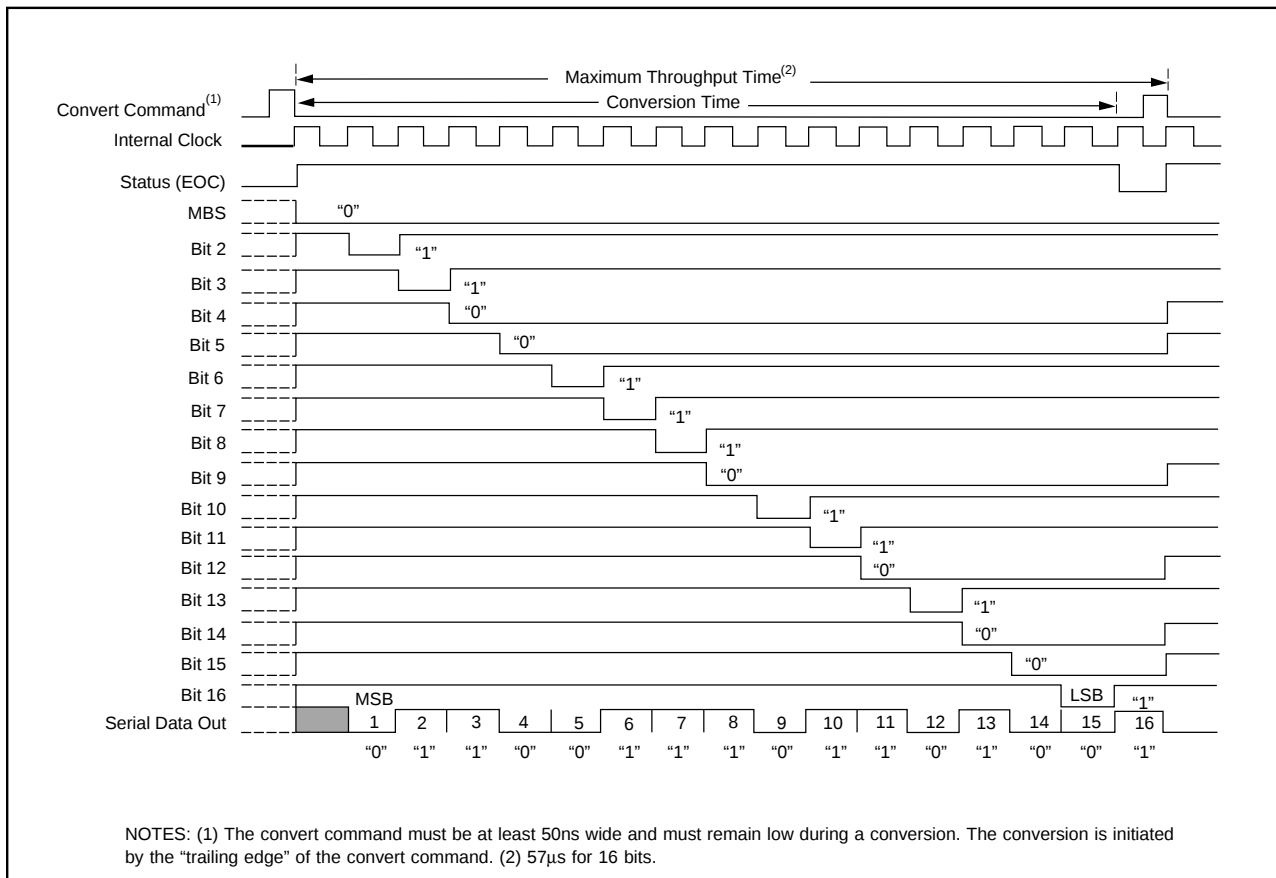


FIGURE 1. ADC71 Timing Diagram.

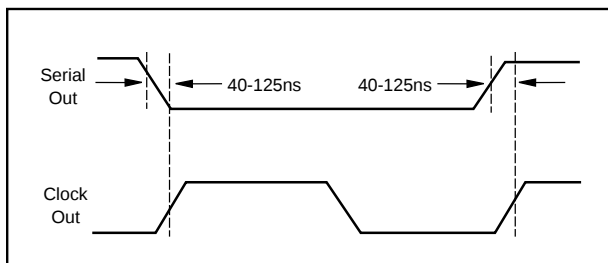


FIGURE 2. Timing Relationship of Serial Data to Clock.

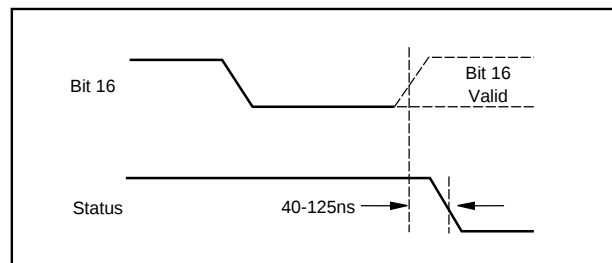


FIGURE 3. Timing Relationship of Valid Data to Status.

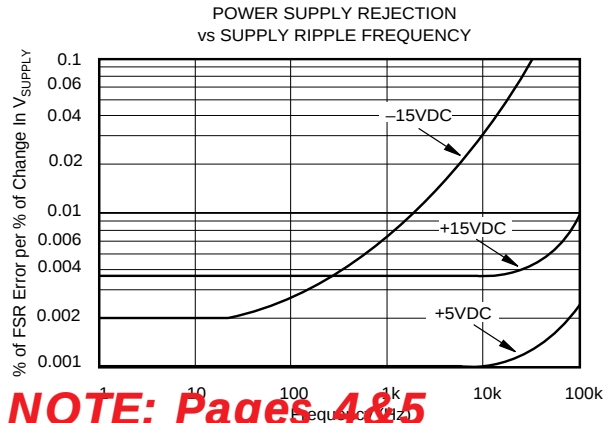
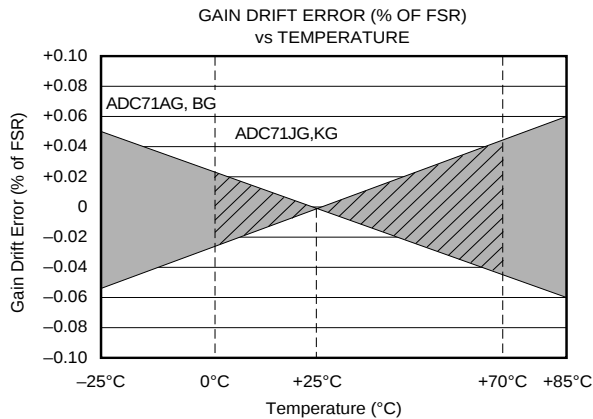
| Binary (BIN)<br>Output                                                                   | INPUT VOLTAGE RANGE AND LSB VALUES              |                                                 |                                                |                                              |                                                |                                              |                                                 |
|------------------------------------------------------------------------------------------|-------------------------------------------------|-------------------------------------------------|------------------------------------------------|----------------------------------------------|------------------------------------------------|----------------------------------------------|-------------------------------------------------|
| Analog Input<br>Voltage Range                                                            | Defined As:                                     | ±10V                                            | ±5V                                            | ±2.5V                                        | 0 to +10V                                      | 0 to +5V                                     | 0 to +20V                                       |
| Code<br>Designation                                                                      |                                                 | COB <sup>(1)</sup><br>or CTC <sup>(2)</sup>     | COB <sup>(1)</sup><br>or CTC <sup>(2)</sup>    | COB <sup>(1)</sup><br>or CTC <sup>(2)</sup>  | CSB <sup>(3)</sup>                             | CSB <sup>(3)</sup>                           | CSB <sup>(3)</sup>                              |
| One Least<br>Significant<br>Bit (LSB)                                                    | $\frac{FSR}{2^n}$<br>n = 12<br>n = 13<br>n = 14 | $\frac{20V}{2^n}$<br>4.88mV<br>2.44mV<br>1.22mV | $\frac{10V}{2^n}$<br>2.44mV<br>1.22mV<br>610μV | $\frac{5V}{2^n}$<br>1.22mV<br>610μV<br>305μV | $\frac{10V}{2^n}$<br>2.44mV<br>1.22mV<br>610μV | $\frac{5V}{2^n}$<br>1.22mV<br>610μV<br>305μV | $\frac{20V}{2^n}$<br>4.88mV<br>2.44mV<br>1.22mV |
| Transition Values<br>MSB LSB<br>000 ... 000 <sup>(4)</sup><br>011 ... 111<br>111 ... 110 | +Full Scale<br>Mid Scale<br>-Full Scale         | +10V-3/2LSB<br>0<br>-10V +1/2LSB                | +5V-3/2LSB<br>0<br>-5V +1/2LSB                 | +2.5V-3/2LSB<br>0<br>-2.5V +1/2LSB           | +10V-3/2LSB<br>+5V<br>0 +1/2LSB                | +5V-3/2LSB<br>+2.5V<br>0 +1/2LSB             | +20V-3/2LSB<br>+10V<br>0 +1/2LSB                |

NOTES: (1) COB = Complementary Offset Binary. (2) Complementary Two's Complement—obtained by inverting the most significant bit MSB (pin 1). (3) CSB = Complementary Straight Binary. (4) Voltages given are the nominal value for transition to the code specified.

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

## TYPICAL PERFORMANCE CURVES

At +25°C and rated power supplies unless otherwise noted.



**NOTE: Pages 4&5  
were switched for  
Abridged Version  
for '96 data book.**

## DISCUSSION OF PERFORMANCE

The accuracy of a successive approximation A/D converter is described by the transfer function shown in Figure 1. All successive approximation A/D converters have an inherent Quantization Error of  $\pm 1/2$  LSB. The remaining errors in the A/D converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including Gain, Offset, Linearity, Differential Linearity, and Power Supply Sensitivity. Initial Gain and Offset errors may be adjusted to zero. Gain drift over temperature rotates the line (Figure 1) about the zero or minus full scale point (all bits Off) and Offset drift shifts the line left or right over the operating temperature range. Linearity error is unadjustable and is the most meaningful indicator of A/D

converter accuracy. Linearity error is the deviation of an actual bit transition from the ideal transition value at any level over the range of the A/D converter. A Differential Linearity error of  $\pm 1/2$  LSB means that the width of each bit step over the range of the A/D converter is 1 LSB,  $\pm 1/2$  LSB.

The ADC71 is monotonic, assuring that the output digital code either increases or remains the same for increasing analog input signals. Burr-Brown guarantees that these converters will have no missing codes over a specified temperature range when short-cycled for 14-bit operation.

## TIMING CONSIDERATIONS

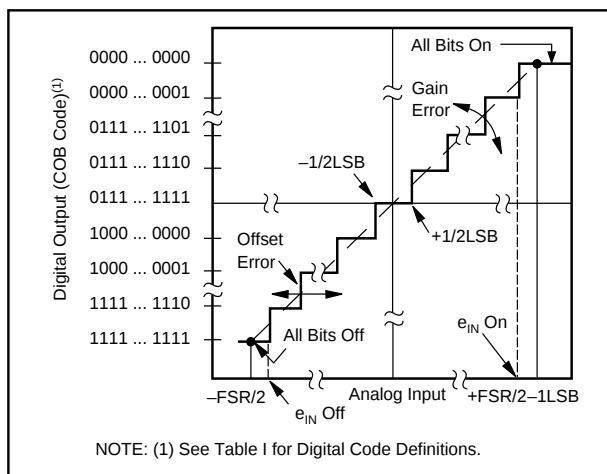
The timing diagram (Figure 2) assumes an analog input such that the positive true digital word 1001 1000 1001 0110 exists. The output will be complementary as shown in Figure 2 (0110 0111 0110 1001 is the digital output). Figures 3 and 4 are timing diagrams showing the relationship of serial data to clock and valid data to status.

## DEFINITION OF DIGITAL CODES

### Parallel Data

Two binary codes are available on the ADC71 parallel output; they are complementary (logic "0" is true) straight binary (CSB) for unipolar input signal ranges and complementary offset binary (COB) for bipolar input signal ranges. Complementary two's complement (CTC) may be obtained by inverting MSB (Pin 1).

Table I shows the LSB, transition values, and code definitions for each possible analog input signal range for 12-, 13- and 14-bit resolutions. Figure 5 shows the connections for 14-bit resolution, parallel data output, with  $\pm 10V$  input.



NOTE: (1) See Table I for Digital Code Definitions.

FIGURE 1. Input vs Output for an Ideal Bipolar A/D Converter.

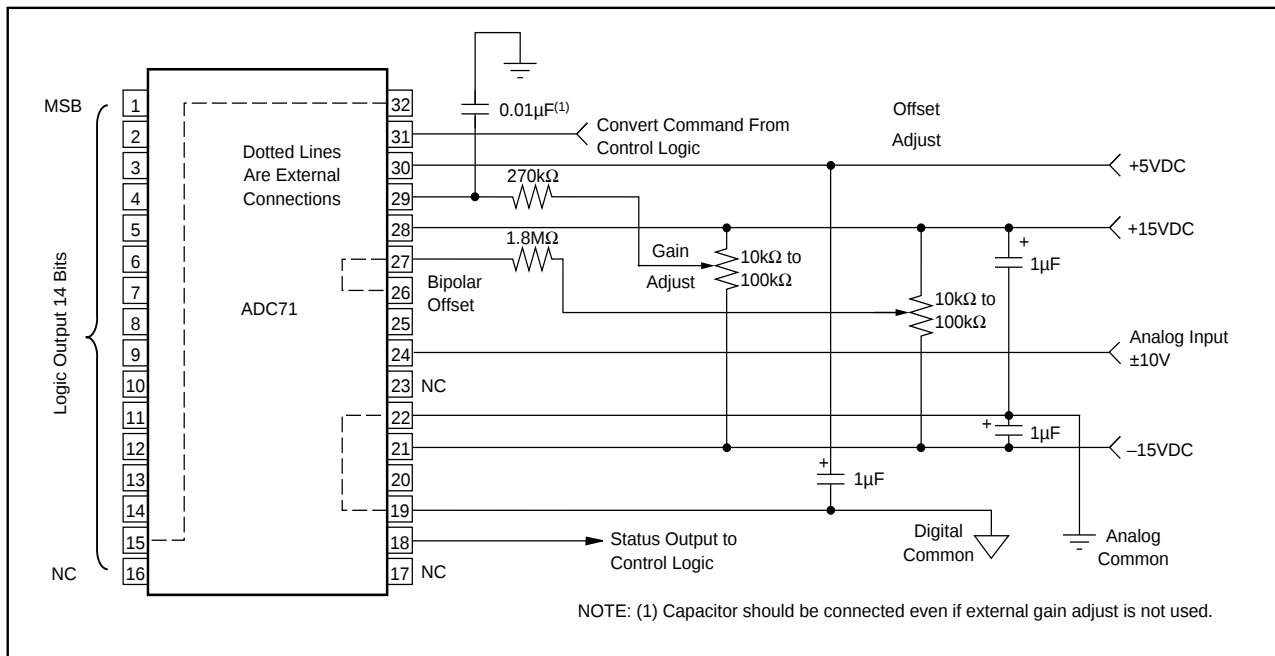


FIGURE 5. ADC71 Connections for:  $\pm 10\text{V}$  Analog Input, 14-Bit Resolution (Short-Cycled), Parallel Data Output.

## SERIAL DATA

Two straight binary (complementary) codes are available on the serial output line: CSB and COB. The serial data is available only during conversion and appears with MSB occurring first. The serial data is synchronous with the internal clock as shown in the timing diagrams of Figures 2 and 3. The LSB and transition values shown in Table I also apply to the serial data output except for the CTC code.

## DISCUSSION OF SPECIFICATIONS

The ADC71 is specified to provide critical performance criteria for a wide variety of applications. The most critical specifications for an A/D converter are linearity, drift, gain and offset errors. This ADC is factory-trimmed and tested for all critical key specifications.

## GAIN AND OFFSET ERROR

Initial Gain and Offset errors are factory-trimmed to typically  $\pm 0.1\%$  of FSR (typically  $\pm 0.05\%$  for unipolar offset) at  $25^\circ\text{C}$ . These errors may be trimmed to zero by connecting external trim potentiometers as shown in Figures 6 and 7.

## POWER SUPPLY SENSITIVITY

Changes in the DC power supplies will affect accuracy. The power supply sensitivity is specified for  $\pm 0.003\%$  of FSR/ $\% \Delta V_s$  for  $\pm 15\text{V}$  supplies and  $\pm 0.001\%$  of FSR/ $\% \Delta V_s$  for  $+5\text{V}$  supplies. Normally, regulated power supplies with 1% or less ripple are recommended for use with this ADC. See Layout Precautions, Power Supply Decoupling and Figure 8.

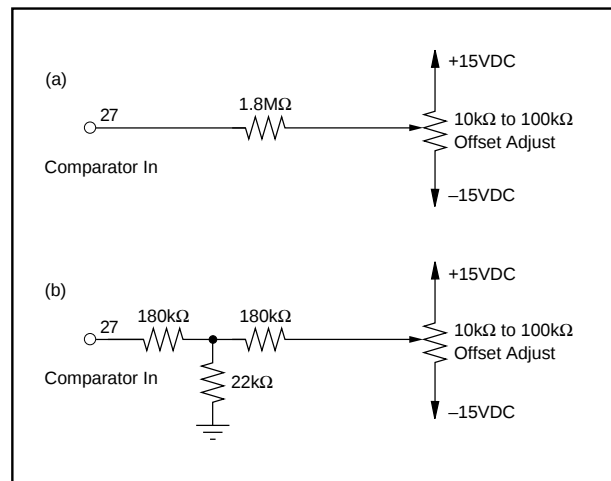


FIGURE 6. Two Methods of Connecting Optional Offset Adjust with a 0.4% of FSR of Adjustment.

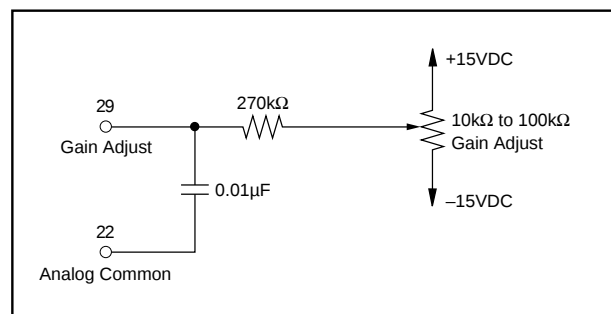


FIGURE 7. Connecting Optional Gain Adjust with a 0.2% Range of Adjustment.

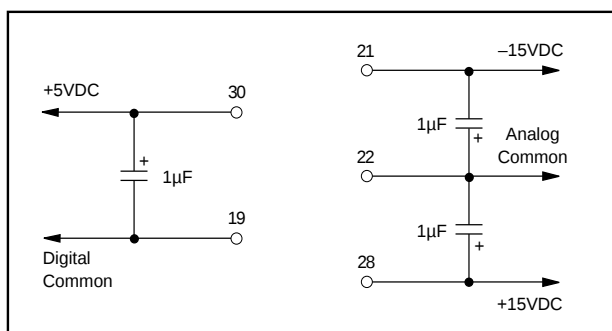


FIGURE 8. Recommended Power Supply Decoupling.

## LAYOUT AND OPERATING INSTRUCTIONS

### Layout Precautions

Analog and digital common are not connected internally in the ADC71 but should be connected together as close to the unit as possible, preferably to a large plane under the ADC. If these grounds must be run separately, use wide conductor patterns and a 0.01µF to 0.1µF non-polarized bypass capacitor between analog and digital commons at the unit. Low impedance analog and digital commons returns are essential for low noise performance. Coupling between analog inputs and digital lines should be minimized by careful layout. The comparator input (Pin 27) is extremely sensitive to noise. Any connection to this point should be as short as possible and shielded by Analog Common patterns.

### POWER SUPPLY DECOUPLING

The power supplies should be bypassed with tantalum capacitors as shown in Figure 8 to obtain noise free operation. These capacitors should be located close to the ADC.

### INPUT SCALING

The analog input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 9 for circuit details.

| INPUT SIGNAL RANGE | OUTPUT CODE               | CONNECT PIN 26 TO PIN | CONNECT PIN 24 TO | CONNECT INPUT SIGNAL TO PIN |
|--------------------|---------------------------|-----------------------|-------------------|-----------------------------|
| ±10V               | COB or CTC <sup>(1)</sup> | 27                    | Input Signal      | 24                          |
| ±5V                | COB or CTC <sup>(1)</sup> | 27                    | Open              | 25                          |
| ±2.5V              | COB or CTC <sup>(1)</sup> | 27                    | Pin 27            | 25                          |
| 0 to +5V           | CSB                       | 22                    | Pin 27            | 25                          |
| 0 to +10V          | CSB                       | 22                    | Open              | 25                          |
| 0 to +20V          | CSB                       | 22                    | Input Signal      | 24                          |

NOTE: (1) Obtained by inverting MSB pin 1.

TABLE II. ADC71 Input Scaling Connections.

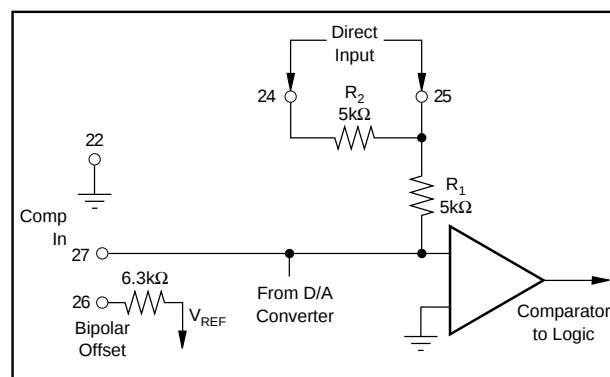


FIGURE 9. ADC71 Input Scaling Circuit.

### OPTIONAL EXTERNAL GAIN AND OFFSET ADJUSTMENTS

Gain and Offset errors may be trimmed to zero using external gain and offset trim potentiometers connected to the ADC as shown in Figure 6 and 7. Multiturn potentiometers with 100ppm/°C or better TCRs are recommended for minimum drift over temperature and time. These pots may be any value from 10kΩ to 100kΩ. All resistors should be 20% carbon or better. Pin 29 (Gain Adjust) and Pin 27 (Offset Adjust) may be left open if no external adjustment is required.

### ADJUSTMENT PROCEDURE

**OFFSET** — Connect the Offset potentiometer (make sure  $R_1$  is as close to pin 27 as possible) as shown in Figure 6. Sweep the input through the end point transition voltage that should cause an output transition to all bits Off ( $E_{IN}$ ).

Adjust the Offset potentiometer until the actual end point transition voltage occurs at  $E_{IN}$ . The ideal transition voltage values of the input are given in Table I.

**GAIN** — Connect the Gain Adjust potentiometer as shown in Figure 7. Sweep the input through the end point transition voltage that should cause an output transition to all bits on ( $E_{IN}$ ). Adjust the Gain potentiometer until the actual end point transition voltage occurs at  $E_{IN}$ .

Table I details the transition voltage levels required.

### CONVERT COMMAND CONSIDERATIONS

Convert command resets the converter whenever taken high. This insures a valid conversion on the first conversion after power-up.

Convert command must stay low during a conversion unless it is desired to reset the converter during a conversion.

### ADDITIONAL CONNECTIONS REQUIRED

The ADC71 may be operated at faster speeds by connecting the Short-Cycle Input, pin 32, as shown in Table III. Conversion speeds, linearity, and resolutions are shown for reference.

## OUTPUT DRIVE

Normally all ADC71 logic outputs will drive two standard TTL loads; however, if long digital lines must be driver, external logic buffers are recommended.

## HEAT DISSIPATION

The ADC71 dissipates approximately 0.6W (typical) and the packages have a case-to-ambient thermal resistance ( $\theta_{CA}$ ) of 25°C/W. For operation above 85°C,  $\theta_{CA}$  should be lowered by a heat sink or by forced air over the surface of the package. See Figure 10 for  $\theta_{CA}$  requirement above 85°C. If the converter is mounted on a PC card, improved thermal contact with the copper ground plane under the case can be achieved using a silicone heat sink compound. On a 0.062" thick PC card with a 16 square in (min) area, this techniques will allow operation to 85°C.

| RESOLUTION (Bits)                                  | 16                   | 14                   | 13     | 12     |
|----------------------------------------------------|----------------------|----------------------|--------|--------|
| Connect Pin 32 to                                  | Open                 | Pin 15               | Pin 14 | Pin 13 |
| Maximum Conversion Speed ( $\mu$ s) <sup>(1)</sup> | 57                   | 50                   | 46.5   | 43     |
| Maximum Nonlinearity at 25°C (% of FSR)            | 0.003 <sup>(2)</sup> | 0.003 <sup>(2)</sup> | 0.006  | 0.006  |

NOTES: (1) Max conversion time to maintain specified nonlinearity error.  
(2) BH and KH models only.

TABLE III. Short-Cycle Connections and Specifications for 12- to 14-Bit Resolutions.

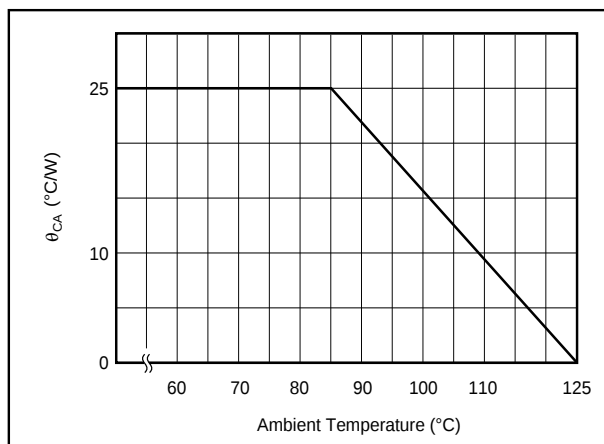


FIGURE 10.  $\theta_{CA}$  Requirement Above 85°C.

This datasheet has been download from:

[www.datasheetcatalog.com](http://www.datasheetcatalog.com)

Datasheets for electronics components.