# TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor
SCHS056D – Revised August 2003

# CD4071B, CD4072B, CD4075B Types

## CMOS OR Gates

### High-Voltage Types (20-Volt Rating)
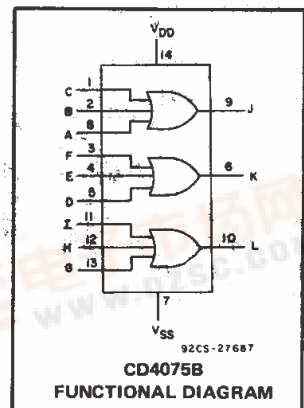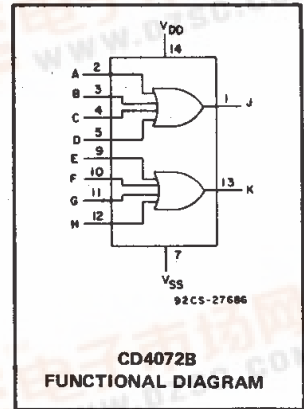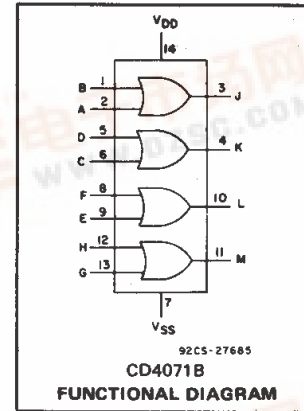
CD4071B    Quad  2-Input   OR   Gate
CD4072B    Dual  4-Input   OR   Gate
CD4075B    Triple 3-Input  OR   Gate

■ CD4071B, CD4072B, and CD4075B OR gates provide the system designer with direct implementation of the positive-logic OR function and supplement the existing family of CMOS gates.

The CD4071B, CD4072B, and CD4075B types are supplied in 14-lead hermetic dual-in-line ceramic packages (F3A suffix), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, MT, M96, and NSR suffixes), and 14-lead thin shrink small-outline packages (PW and PWR suffixes).

### Features:

■ Medium-Speed Operation-$t_{PLH}$, $t_{PHL}$ = 60 ns (typ.) at $V_{DD}$ = 10 V
■ 100% tested for quiescent current at 20 V
■ Maximum input current of 1 $\mu$A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
■ Standardized, symmetrical output characteristics
■ Noise margin (over full package temperature range)
    1 V at $V_{DD}$ = 5 V
    2 V at $V_{DD}$ = 10 V
    2.5 V at $V_{DD}$ = 15 V
■ 5-V, 10-V, and 15-V parametric ratings
■ Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"



CD4071B
FUNCTIONAL DIAGRAM
92CS-27685



CD4072B
FUNCTIONAL DIAGRAM
92CS-27686



CD4075B
FUNCTIONAL DIAGRAM
92CS-27687

## RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

| CHARACTERISTIC | LIMITS | | UNITS |
|---|---|---|---|
| | MIN. | MAX. | |
| Supply-Voltage Range (For $T_A$ = Full Package-Temperature Range) | 3 | 18 | V |

## STATIC ELECTRICAL CHARACTERISTICS

| CHARACTER-ISTIC | CONDITIONS | | | LIMITS AT INDICATED TEMPERATURES (°C) | | | | | +25 | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | $V_O$ (V) | $V_{IN}$ (V) | $V_{DD}$ (V) | −55 | −40 | +85 | +125 | Min. | Typ. | Max. | |
| Quiescent Device Current, $I_{DD}$ Max. | -- | 0,5 | 5 | 0.25 | 0.25 | 7.5 | 7.5 | -- | 0.01 | 0.25 | $\mu$A |
| | -- | 0,10 | 10 | 0.5 | 0.5 | 15 | 15 | -- | 0.01 | 0.5 | |
| | -- | 0,15 | 15 | 1 | 1 | 30 | 30 | -- | 0.01 | 1 | |
| | -- | 0,20 | 20 | 5 | 5 | 150 | 150 | -- | 0.02 | 5 | |
| Output Low (Sink) Current $I_{OL}$ Min. | 0.4 | 0,5 | 5 | 0.64 | 0.61 | 0.42 | 0.36 | 0.51 | 1 | -- | mA |
| | 0.5 | 0,10 | 10 | 1.6 | 1.5 | 1.1 | 0.9 | 1.3 | 2.6 | -- | |
| | 1.5 | 0,15 | 15 | 4.2 | 4 | 2.8 | 2.4 | 3 4 | 6.8 | -- | |
| Output High (Source) Current, $I_{OH}$ Min. | 4.6 | 0,5 | 5 | −0.64 | −0.61 | −0.42 | −0.36 | −0.51 | −1 | -- | |
| | 2.5 | 0,5 | 5 | −2 | −1.8 | −1.3 | −1.15 | −1.6 | −3.2 | -- | |
| | 9.5 | 0,10 | 10 | −1.6 | −1.5 | −1.1 | −0.9 | −1.3 | −2.6 | -- | |
| | 13.5 | 0,15 | 15 | −4.2 | −4 | −2.8 | −2.4 | −3.4 | −6.8 | -- | |
| Output Voltage: Low-Level, $V_{OL}$ Max. | -- | 0,5 | 5 | 0.05 | | | | -- | 0 | 0.05 | V |
| | -- | 0,10 | 10 | 0.05 | | | | -- | 0 | 0.05 | |
| | -- | 0,15 | 15 | 0.05 | | | | -- | 0 | 0.05 | |
| Output Voltage: High-Level, $V_{OH}$ Min. | -- | 0,5 | 5 | 4.95 | | | | 4.95 | 5 | -- | |
| | -- | 0,10 | 10 | 9.95 | | | | 9.95 | 10 | -- | |
| | -- | 0,15 | 15 | 14.95 | | | | 14.95 | 15 | -- | |
| Input Low Voltage, $V_{IL}$ Max. | 0.5, 4.5 | -- | 5 | 1.5 | | | | -- | -- | 1.5 | |
| | 1, 9 | -- | 10 | 3 | | | | -- | -- | 3 | |
| | 1.5,13.5 | -- | 15 | 4 | | | | -- | -- | 4 | V |
| Input High Voltage, $V_{IH}$ Min. | 4.5 | -- | 5 | 3.5 | | | | 3.5 | -- | -- | |
| | 9 | -- | 10 | 7 | | | | 7 | -- | -- | |
| | 13.5 | -- | 15 | 11 | | | | 11 | -- | -- | |
| Input Current, $I_{IN}$ Max. | | 0,18 | 18 | ±0.1 | ±0.1 | ±1 | ±1 | -- | $\pm 10^{-5}$ | ±0.1 | $\mu$A |

# CD4071B, CD4072B, CD4075B Types

**MAXIMUM RATINGS,** *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, ($V_{DD}$)
  Voltages referenced to $V_{SS}$ Terminal) .................................................. −0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS ...................................................... −0.5V to $V_{DD}$ +0.5V
DC INPUT CURRENT, ANY ONE INPUT ........................................................ ±10mA
POWER DISSIPATION PER PACKAGE ($P_D$):
  For $T_A$ = −55°C to +100°C ................................................................ 500mW
  For $T_A$ = +100°C to +125°C ................................................ Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
  FOR $T_A$ = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ........................ 100mW
OPERATING-TEMPERATURE RANGE ($T_A$) ................................................ −55°C to +125°C
STORAGE TEMPERATURE RANGE ($T_{stg}$) ................................................ −65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
  At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ........................ +265°C
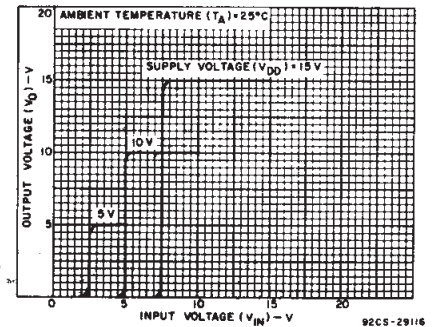


Fig. 1 — Typical voltage transfer characteristics.

**DYNAMIC ELECTRICAL CHARACTERISTICS** at $T_A$ = 25°C, Input $t_r$, $t_f$ = 20 ns, and $C_L$ = 50 pF, $R_L$ = 200 kΩ

| CHARACTERISTIC | TEST CONDITIONS | ALL TYPES LIMITS | | | UNITS |
|---|---|---|---|---|---|
| | | $V_{DD}$ VOLTS | TYP. | MAX. | |
| Propagation Delay Time, $t_{PHL}$, $t_{PLH}$ | | 5 | 125 | 250 | ns |
| | | 10 | 60 | 120 | |
| | | 15 | 45 | 90 | |
| Transition Time, $t_{THL}$, $t_{TLH}$ | | 5 | 100 | 200 | ns |
| | | 10 | 50 | 100 | |
| | | 15 | 40 | 80 | |
| Input Capacitance, $C_{IN}$ | Any Input | — | 5 | 7.5 | pF |
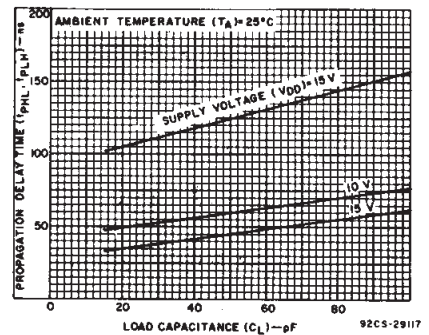


Fig. 2 — Typical propagation delay time as a function of load capacitance.
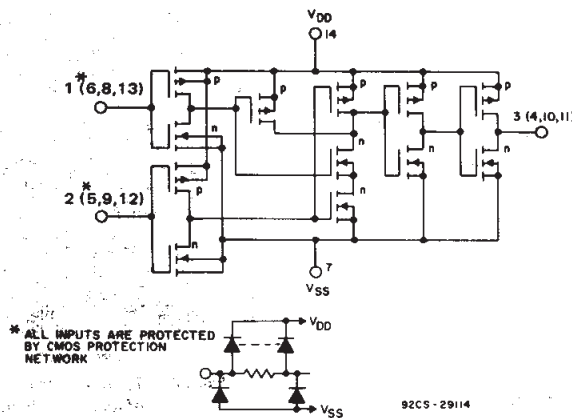
Fig. 3 — Schematic diagram for CD4071B (1 of 4 identical gates).

* ALL INPUTS ARE PROTECTED BY CMOS PROTECTION NETWORK



Fig. 4 — Typical output low (sink) current characteristics.



Fig. 5 — Logic diagram for CD4071B (1 of 4 identical gates).



Fig. 6 — Minimum output low (sink) current characteristics.

*INVERTERS 2,3 AND 4 ARE IDENTICAL TO INVERTER I.

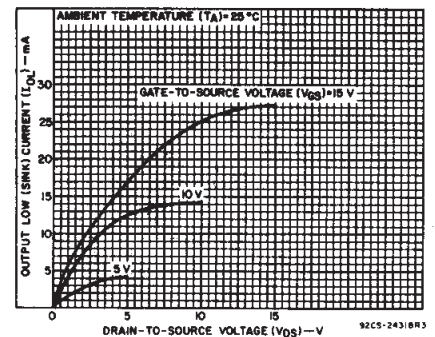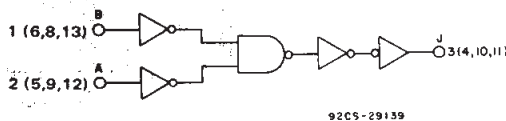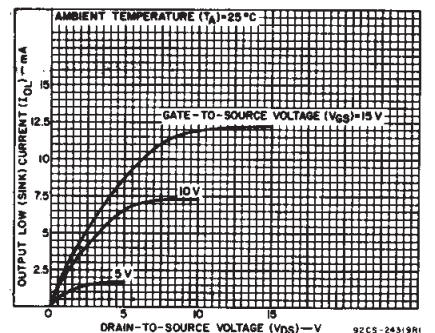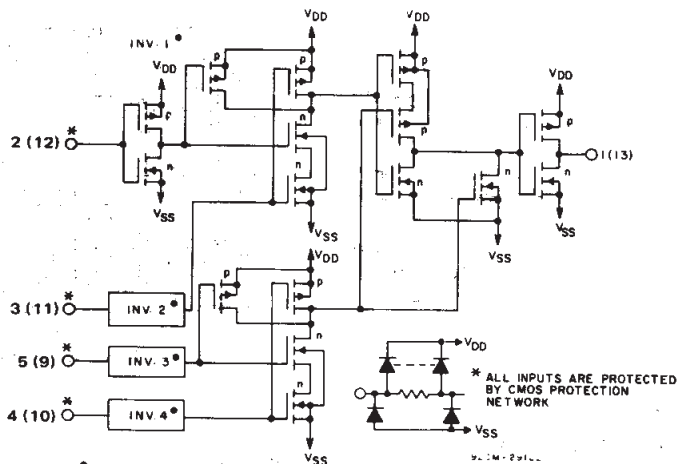Fig. 7 – Schematic diagram for CD4072B (1 of 2 identical gates).



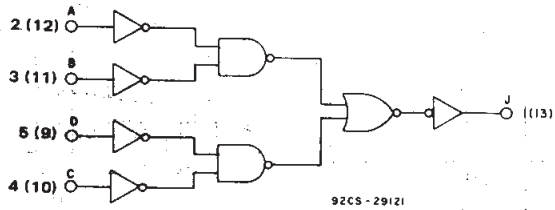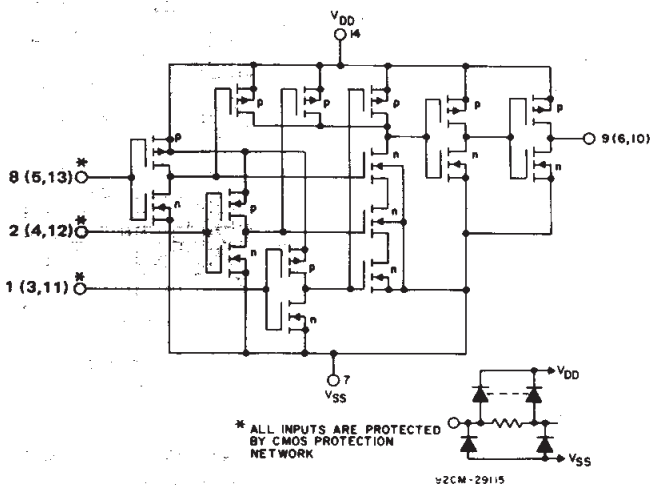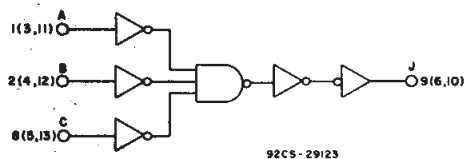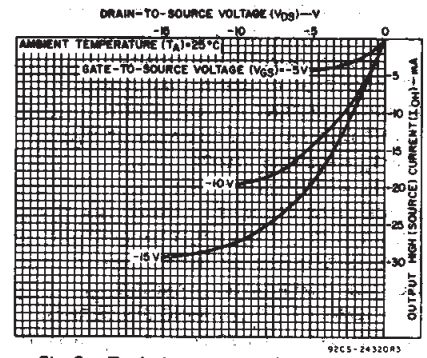Fig. 9 – Logic diagram for CD4072B (1 of 2 identical gates).



Fig. 8 – Typical output high (source) current characteristics.
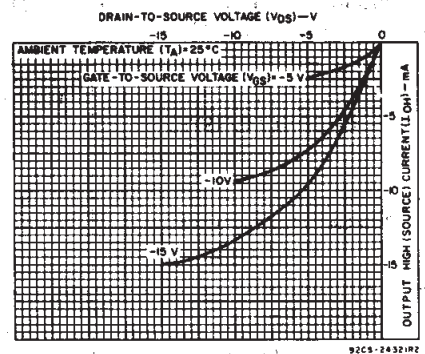


Fig. 10 – Minimum output high (source) current characteristics.



* ALL INPUTS ARE PROTECTED BY CMOS PROTECTION NETWORK

Fig. 11 – Schematic diagram for CD4075B (1 of 3 identical gates).



Fig. 13 – Logic diagram for CD4075B (1 of 3 identical gates).
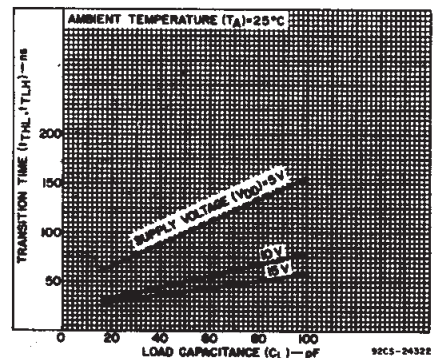


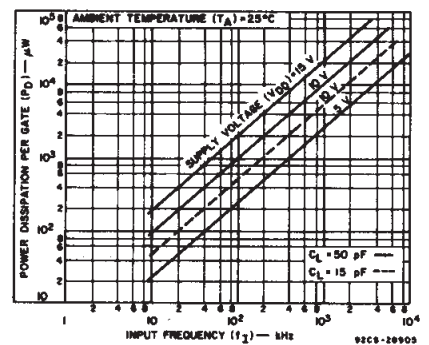Fig. 12 – Typical transition time as a function of load capacitance.



Fig. 14 – Typical dyanamic power dissipation as a function of frequency.

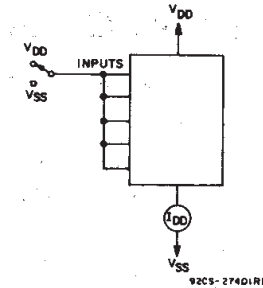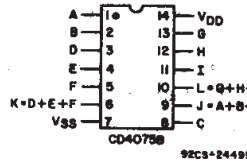# CD4071B, CD4072B, CD4075B Types

## TERMINAL ASSIGNMENTS (TOP VIEW)



**CD4071B**
92CS-24494

**CD4072B**
NC = NO CONNECTION 92CS-24496R2

**CD4075B**
92CS-24495
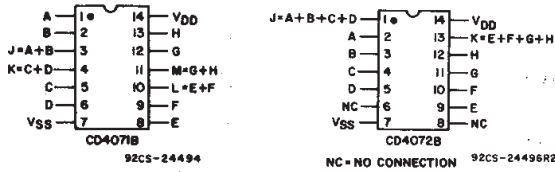


Fig. 15 — Quiescent device current test circuit.



NOTE:
MEASURE INPUTS SEQUENTIALLY, TO BOTH $V_{DD}$ AND $V_{SS}$. CONNECT ALL UNUSED INPUTS TO EITHER $V_{DD}$ OR $V_{SS}$.

92CS-27402
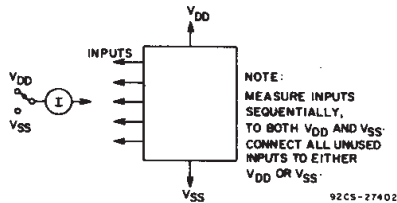
Fig. 16 — Input current test circuit.



NOTE:
TEST ANY COMBINATION OF INPUTS

92CS-27441R1
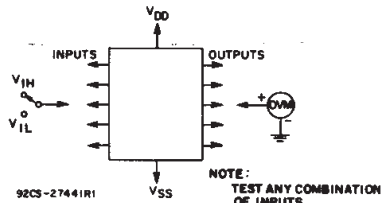
Fig. 17 — Input-voltage test circuit.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ($10^{-3}$ inch).
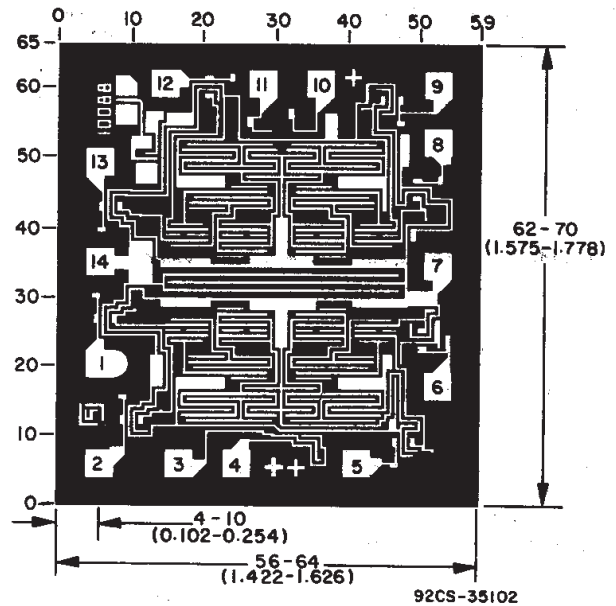


62-70
(1.575-1.778)

4-10
(0.102-0.254)

56-64
(1.422-1.626)

92CS-35102

Chip dimensions and pad layout for CD4071B.



51-59
(1.295-1.498)

4-10
(0.102-0.254)

58-66
(1.474-1.676)

92CS-32209

Chip dimensions and pad layout for CD4072B.



60-68
(1.524-1.727)

4-10
(0.102-0.254)

58-66
(1.474-1.676)

92CS-29120
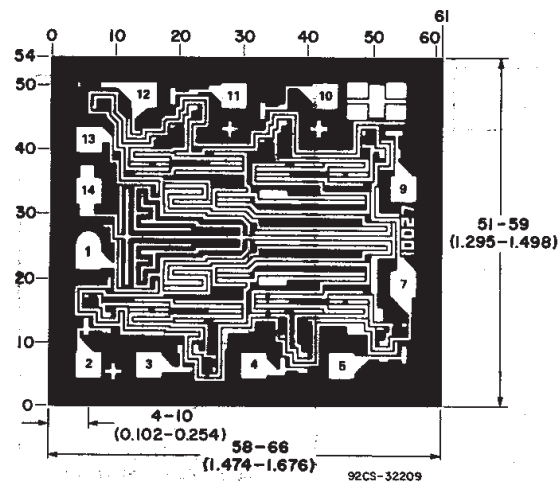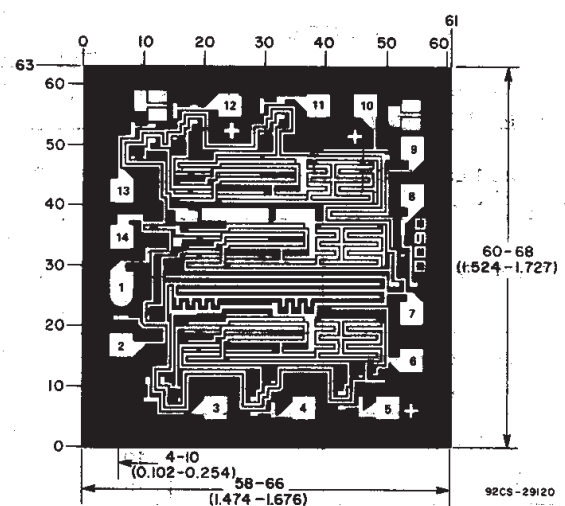
Chip dimensions and pad layout for CD4075B.

## PACKAGING INFORMATION

| Orderable Device | Status [1] | Package Type | Package Drawing | Pins | Package Qty | Eco Plan [2] | Lead/Ball Finish | MSL Peak Temp [3] |
|---|---|---|---|---|---|---|---|---|
| 7706002CA | ACTIVE | CDIP | J | 14 | 1 | None | Call TI | Level-NC-NC-NC |
| CD4071BE | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | Level-NC-NC-NC |
| CD4071BF | ACTIVE | CDIP | J | 14 | 1 | None | Call TI | Level-NC-NC-NC |
| CD4071BF3A | ACTIVE | CDIP | J | 14 | 1 | None | Call TI | Level-NC-NC-NC |
| CD4071BM | ACTIVE | SOIC | D | 14 | 50 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| CD4071BM96 | ACTIVE | SOIC | D | 14 | 2500 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| CD4071BMT | ACTIVE | SOIC | D | 14 | 250 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| CD4071BNSR | ACTIVE | SO | NS | 14 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| CD4071BPW | ACTIVE | TSSOP | PW | 14 | 90 | Pb-Free (RoHS) | CU NIPDAU | Level-1-250C-UNLIM |
| CD4071BPWR | ACTIVE | TSSOP | PW | 14 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-1-250C-UNLIM |
| CD4072BE | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | Level-NC-NC-NC |
| CD4072BF | ACTIVE | CDIP | J | 14 | 1 | None | Call TI | Level-NC-NC-NC |
| CD4072BF3A | ACTIVE | CDIP | J | 14 | 1 | None | Call TI | Level-NC-NC-NC |
| CD4072BM | ACTIVE | SOIC | D | 14 | 50 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| CD4072BM96 | ACTIVE | SOIC | D | 14 | 2500 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| CD4072BMT | ACTIVE | SOIC | D | 14 | 250 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| CD4072BNSR | ACTIVE | SO | NS | 14 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| CD4072BPW | ACTIVE | TSSOP | PW | 14 | 90 | Pb-Free (RoHS) | CU NIPDAU | Level-1-250C-UNLIM |
| CD4072BPWR | ACTIVE | TSSOP | PW | 14 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-1-250C-UNLIM |
| CD4075BE | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | Level-NC-NC-NC |
| CD4075BF | ACTIVE | CDIP | J | 14 | 1 | None | Call TI | Level-NC-NC-NC |
| CD4075BF3A | ACTIVE | CDIP | J | 14 | 1 | None | Call TI | Level-NC-NC-NC |
| CD4075BM | ACTIVE | SOIC | D | 14 | 50 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| CD4075BM96 | ACTIVE | SOIC | D | 14 | 2500 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| CD4075BMT | ACTIVE | SOIC | D | 14 | 250 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| CD4075BNSR | ACTIVE | SO | NS | 14 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| CD4075BPW | ACTIVE | TSSOP | PW | 14 | 90 | Pb-Free (RoHS) | CU NIPDAU | Level-1-250C-UNLIM |
| CD4075BPWR | ACTIVE | TSSOP | PW | 14 | 2000 | Pb-Free | CU NIPDAU | Level-1-250C-UNLIM |

| Orderable Device | Status [1] | Package Type | Package Drawing | Pins | Package Qty | Eco Plan [2] | Lead/Ball Finish | MSL Peak Temp [3] |
|---|---|---|---|---|---|---|---|---|
| | | | | | | (RoHS) | | |
| JM38510/17101BCA | ACTIVE | CDIP | J | 14 | 1 | None | Call TI | Level-NC-NC-NC |
| JM38510/17103BCA | ACTIVE | CDIP | J | 14 | 1 | None | Call TI | Level-NC-NC-NC |

[1] The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

[2] Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**None:** Not yet available Lead (Pb-Free).
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

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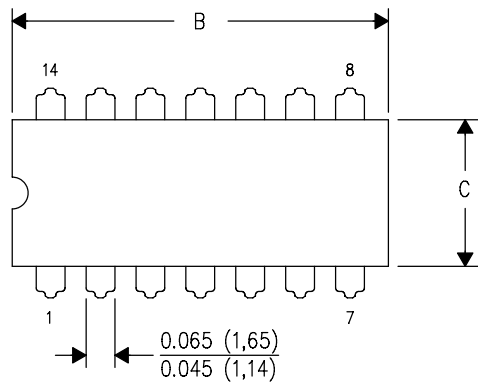
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
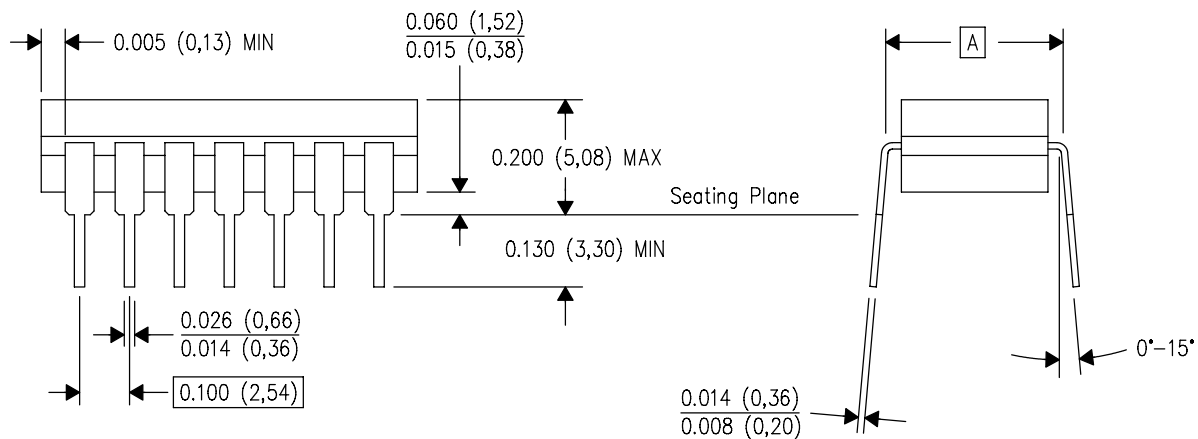
| DIM ╲ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |

B

14          8

0.065 (1,65)
0.045 (1,14)

C

1          7

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

A

0°−15°

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)

0.014 (0,36)
0.008 (0,20)

4040083/F 03/03

NOTES:    A.  All linear dimensions are in inches (millimeters).
          B.  This drawing is subject to change without notice.
          C.  This package is hermetically sealed with a ceramic lid using glass frit.
          D.  Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
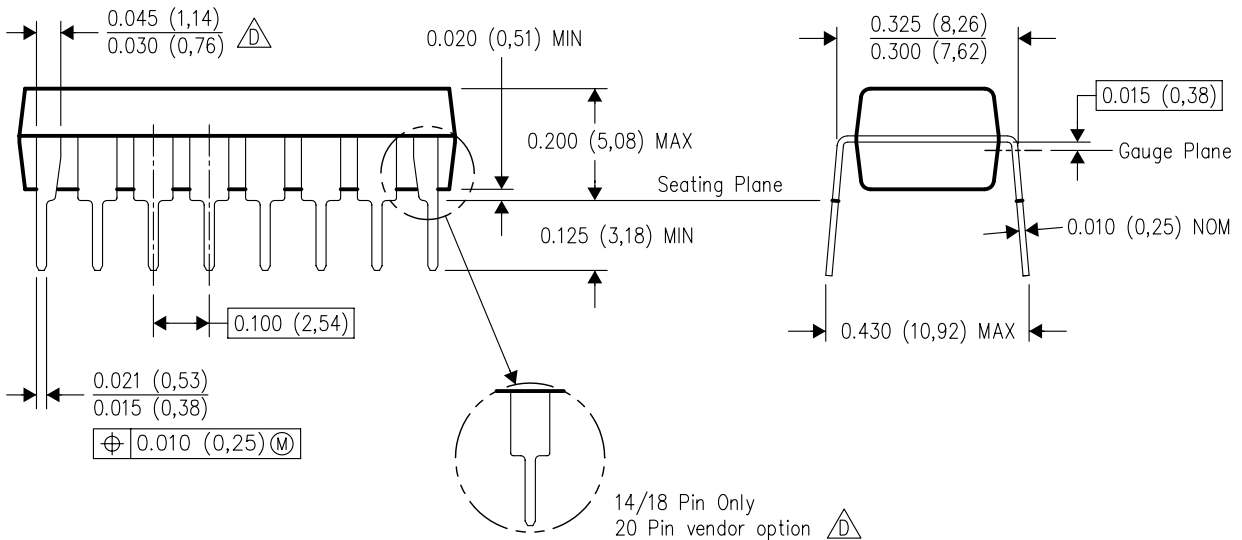          E.  Falls within MIL STD 1835 GDIP1−T14, GDIP1−T16, GDIP1−T18 and GDIP1−T20.

## N (R−PDIP−T**)
16 PINS SHOWN

## PLASTIC DUAL−IN−LINE PACKAGE
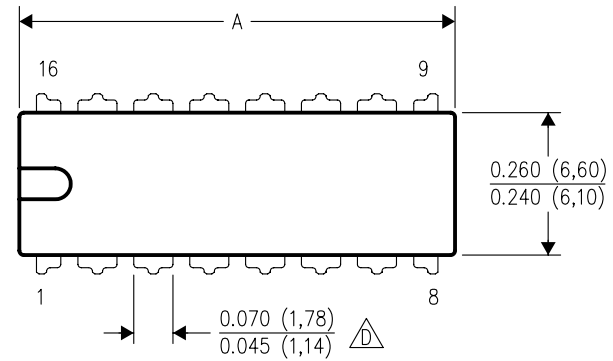


| DIM | PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|---|
| A MAX | | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS−001 VARIATION | | AA | BB | AC | AD |

0.260 (6,60)
0.240 (6,10)

0.070 (1,78)
0.045 (1,14) D

0.045 (1,14)
0.030 (0,76) D

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) M

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX
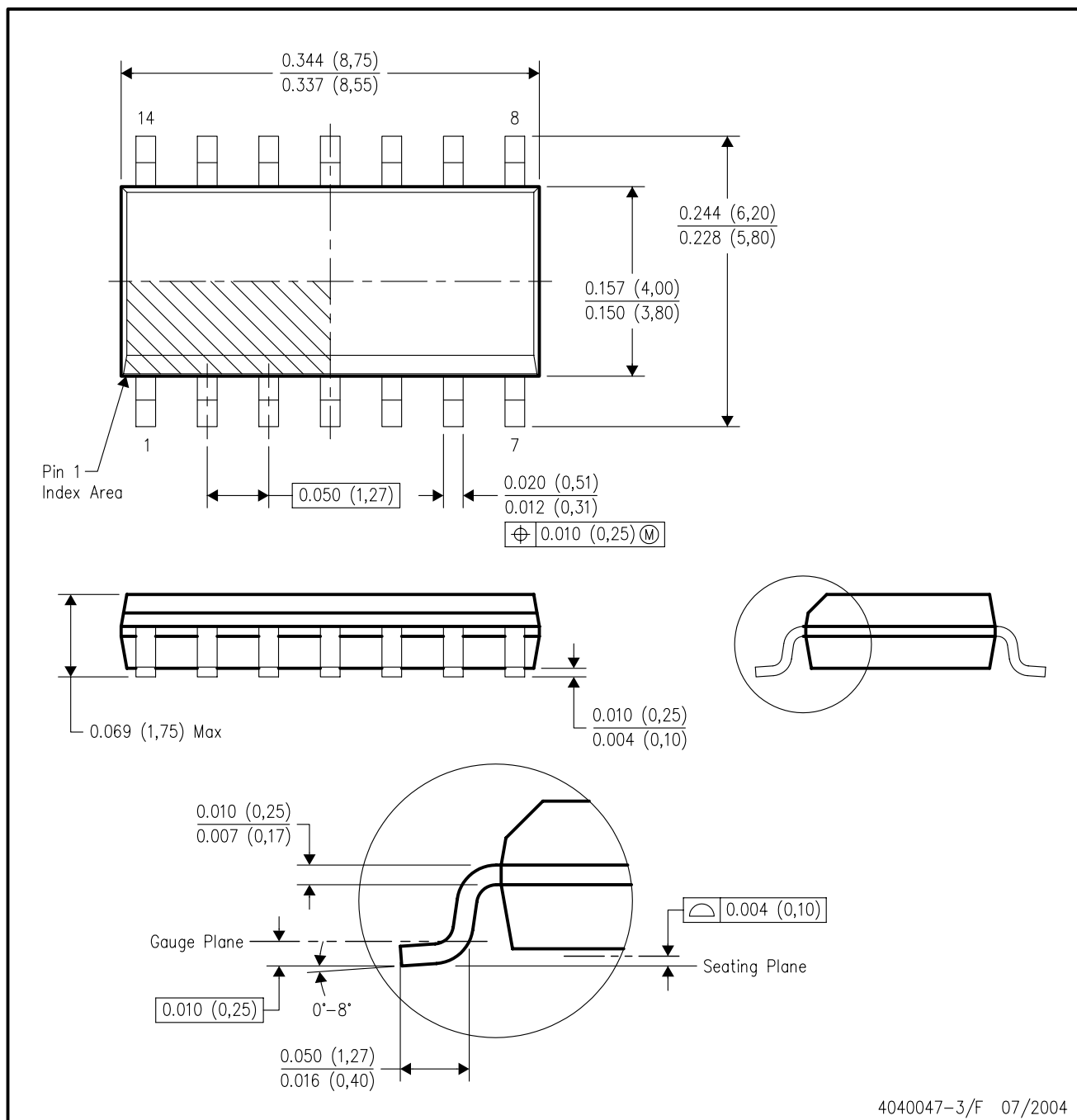
14/18 Pin Only
20 Pin vendor option D

4040049/E  12/2002

NOTES:  A.  All linear dimensions are in inches (millimeters).
B.  This drawing is subject to change without notice.
C.  Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
D.  The 20 pin end lead shoulder width is a vendor option, either half or full width.

## D (R−PDSO−G14)                    PLASTIC SMALL−OUTLINE PACKAGE

0.344 (8,75)
0.337 (8,55)

14          8

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)

1           7

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.007 (0,17)

Gauge Plane

⌂ 0.004 (0,10)

Seating Plane

0.010 (0,25)

0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−3/F  07/2004
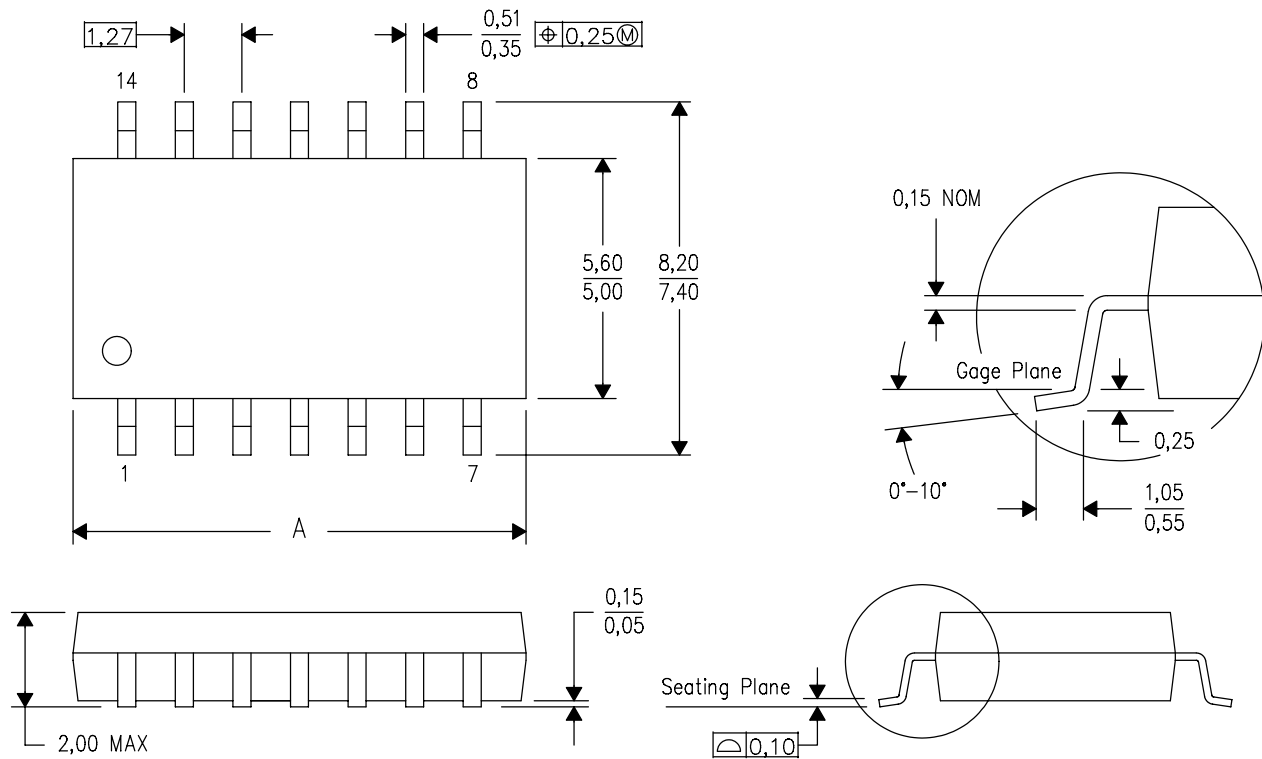
NOTES:   A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
         D.   Falls within JEDEC MS−012 variation AB.

## MECHANICAL DATA

**NS (R-PDSO-G\*\*)**                                         **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**

| DIM \ PINS \*\* | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A   MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A   MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

NOTES:   A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
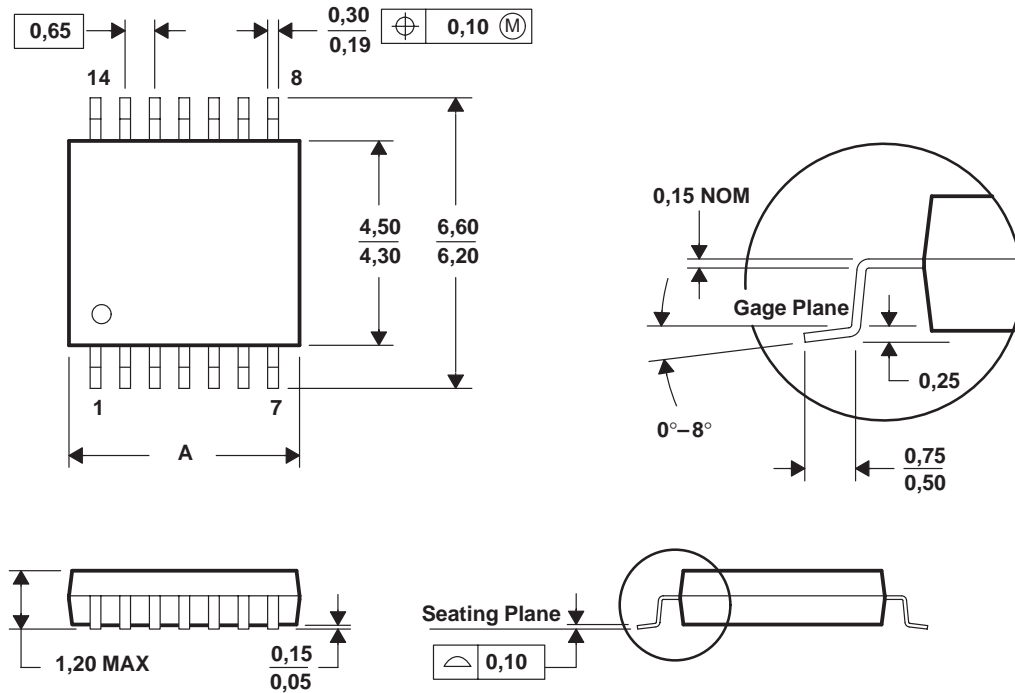         C.   Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

# MECHANICAL DATA

**PW (R-PDSO-G\*\*)**　　　　　　　　　　　　　　　　　　　**PLASTIC SMALL-OUTLINE PACKAGE**

**14 PINS SHOWN**

| DIM \ PINS \*\* | 8 | 14 | 16 | 20 | 24 | 28 |
|---|---|---|---|---|---|---|
| A MAX | 3,10 | 5,10 | 5,10 | 6,60 | 7,90 | 9,80 |
| A MIN | 2,90 | 4,90 | 4,90 | 6,40 | 7,70 | 9,60 |

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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