



義隆電子股份有限公司
ELAN MICROELECTRONICS CORP.

EM78871

8-BIT MICRO-CONTROLLER

Version 1.5

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Version History

Specification Revision History		
Preliminary Version	Content	Release Date
EM78871		
1.0	Initial version	2003/06/05
1.1	Remove Package	2003/06/18
1.2	Modify Idle mode current	2003/08/07
1.3	Modify Code option	2004/02/09
1.4	Modify Package type	2004/03/15
1.5	Remove Idle Mode Function	2004/08/23



User Application Note

1. ROM, OTP, ICE

ROM	OTP	ICE
EM78871	EM78P808	ICE 808

2. The difference between ICE 808 , EM78P808 and EM78871 are listed in the table

	ICE 808	EM78P808	EM78871
Comparator reference voltage	VDD	VDD or 2V	VDD or 2V
Stack pointer	O	O	X
Data Rom	O	O	X (R6 page1 bit0-7&R7 page1 bit0- 7&R8 page1 bit0-7& R9 page1 bit0-1 unused)
RE page1 bit4	O	O	X(unused)
IOCE page1 bit0-1	O	O	X(unused)
RE page1 bit7-6 IOCE page2 bit0-2, bit4-6 code option bit0	O	O	X(unused)

3. "While switching main clock (regardless of high freq to low freq or on the other hand), adding 6 instructions delay (NOP) is required."

4. For DATA RAM least address(A0~A7), when using "INC" instruction and overflow occur, the middle address will auto_increase. If using "DEC" instruction and least address from 0x00→0xFF, the middle address can't auto_decrease.

5. When Tip and Ring signals come, user cans choice one of FSK or DTMF receiver to decode.

The Operation Registers Setup as follows:

FSK (RA PAGE0 bit 3)	DTMF (IOC9 PAGE1 bit 7)	FSK or DTMF
0	0	All decoder off
0	1	DTMF on FSK off
1	X (don't care)	FSK on DTMF off

6.Die Pin difference

	EM78P808	EM78871
Pin	136 pins	132 pins
EGIN1	V	X
EGIN2	V	X
Power PAD	2(VDD pin & AVDD pin)	1(VDD/AVDD pin)
Gnd PAD	2(AVSS pin & GND pin)	1(AVSS/GND pin)

7.Don't switch to sleep mode from normal mode directly. Before do this, please switch to green mode first.

8.Don't allow enable Idle Mode Function. (RA Page0 bit 7 don't allow set to 1)



I. General Description

The EM78871 is an 8-bit CID (Call Identification) RISC type microprocessor with low power, high speed CMOS technology. Integrated onto a single chip are on chip watchdog (WDT), RAM, program ROM, programmable real time clock/counter, external/internal interrupt, power down mode, LCD driver, FSK decoder, Call waiting decoder, DTMF receiver, Programming Tone generator, build-in KEY TONE clock generation, Comparator and tri-state I/O. The EM78871 provides a single chip solution to design a CID of calling message display.

II. Feature

➤ CPU

- Operating voltage range : 2.2V~5.5V(Normal mode), 2.0V~5.5V(Green mode)
- 32K×13 on chip Program ROM
- 4K×8 on chip data RAM
- 144 byte working register
- Up to 51 bi-directional tri-state I/O ports (32 shared with LCD Segment pins)
- IO with internal Pull high, wake-up and interrupt functions
- STACK: 32 level stack for subroutine nesting
- TCC: 8-bit real time clock/counter (TCC) with 8-bit prescaler
- COUNTER1: 8-bit counter with 8-bit prescaler can be an interrupt source
- COUNTER2: 8-bit counter with 8-bit prescaler can be an interrupt source
- Watch Dog : Programmable free running on chip watchdog timer
- CPU modes:

Mode	CPU status	Main clock	32.768kHz clock status
Sleep mode	Turn off	Turn off	Turn off
Green mode	Turn on	Turn off	Turn on
Normal mode	Turn on	Turn on	Turn on

- 13 interrupt source , 8 external , 5 internal
- Key Scan : Port key scan function up to 16x4 keys
- Sub-Clock: 32.768KHz crystal
- Main-clock: 3.5862MHz multiplied by 0.25, 0.5, 1 or 3 generated by internal PLL
- Key tone output :4KHz, 2KHz ,1KHz (shared with IO)
- Comparator: 3-channel comparators: internal (16 level) or external reference voltage. (shared with IO)
- Serial Peripheral Interface (SPI): Interrupt flag available for the read buffer full, Programmable baud rates of communication, Three-wire synchronous communication. (shared with IO)

➤ Current D/A

- Operation Voltage : 2.5V 5.5V
- 7-bit resolution and 3-bit output level control
- Current DA output can drive speaker through a transistor for sound playing. (shared with IO)

➤ Programmable Tone Generators

- Operation Voltage 2.2V 5.5V
- Programmable Tone1 and Tone2 generators
- Independent single tone generation for Tone1 and Tone2
- Mixed dual tone generation by Tone1 and Tone2 with 2dB difference
- Can be programmed for DTMF tone generation
- Can be programmed for FSK signal (Bell202 or V.23) generation

➤ CID

- Operation Voltage 2.7V 5.5V for FSK
- Operation Voltage 2.7V 5.5V for DTMF receiver
- Compatible with Bellcore GR-30-CORE (formerly as TR-NWT-000030)
- Compatible with British Telecom (BT) SIN227 & SIN242
- FSK demodulator for Bell 202 and ITU-T V.23 (formerly as CCITT V.23)

➤ CALL WAITING

- Operation Voltage 2.6V 5.5V



- Compatible with Bellcore special report SR-TSV-002476
- Call-Waiting (2130Hz plus 2750Hz) Alert Signal Detector
- Good talkdown and talkoff performance
- Sensitivity compensated by adjusting input OP gain

➤ **LCD (8x80, 9x80, 16x80, 24x72)**

- Maximum common driver pins : 16/24
- Maximum segment driver pins : 80(SEG0..SEG79)/72(SEG8..SEG79)
- Shared COM16 ~ COM23 pins with SEG0 ~ SEG7 pins
- 1/4 bias for 8, 9 and 16 common mode and 1/5 bias for 24 common mode
- 1/8, 1/9, 1/16, 1/24 duty
- 16 Level LCD contrast control (software)
- Internal resistor circuit for LCD bias
- Internal voltage follower for better display

➤ **Die type**

- 132 pin die : EM78871H
- 128 pin package : (EM78871AQ POVD disable, EM78871BQ POVD enable)

III.Application

1. adjunct units
2. answering machines
3. feature phones

	SEG13	128	1	102	SEG39
	SEG14	127	2	101	SEG40
	SEG15	126	3	100	SEG41
	SEG16	125	4	99	SEG42
	SEG17	124	5	98	SEG43
	SEG18	123	6	97	SEG44
	SEG19	122	7	96	SEG45
	SEG20	121	8	95	SEG46
	SEG21	120	9	94	SEG47
	SEG22	119	10	93	SEG48/PB0
	SEG23	118	11	92	SEG49/PB1
	SEG24	117	12	91	SEG50/PB2
	SEG25	116	13	90	SEG51/PB3
	SEG26	115	14	89	SEG52/PB4
	SEG27	114	15	88	SEG53/PB5
	SEG28	113	16	87	SEG54/PB6
	SEG29	112	17	86	SEG55/PB7
	SEG30	111	18	85	SEG60/PC4
	SEG31	110	19	84	SEG61/PC5
	SEG32	109	20	83	SEG62/PC6
	SEG33	108	21	82	SEG63/PC7
	SEG34	107	22	81	SEG64/P80
	SEG35	106	23	80	SEG65/P81
	SEG36	105	24	79	SEG66/P82
	SEG37	104	25	78	SEG67/P83
	SEG38	103	26	77	SEG68/P84
			27	76	SEG69/P85
			28	75	SEG70/P86
			29	74	SEG71/P87
			30	73	SEG72/P90
			31	72	SEG73/P91
			32	71	SEG74/P92
			33	70	SEG75/P93
			34	69	SEG76/P94
			35	68	SEG77/P95
			36	67	SEG78/P96
			37	66	SEG79/P97
			38	65	VC5
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V.Functional Block Diagram

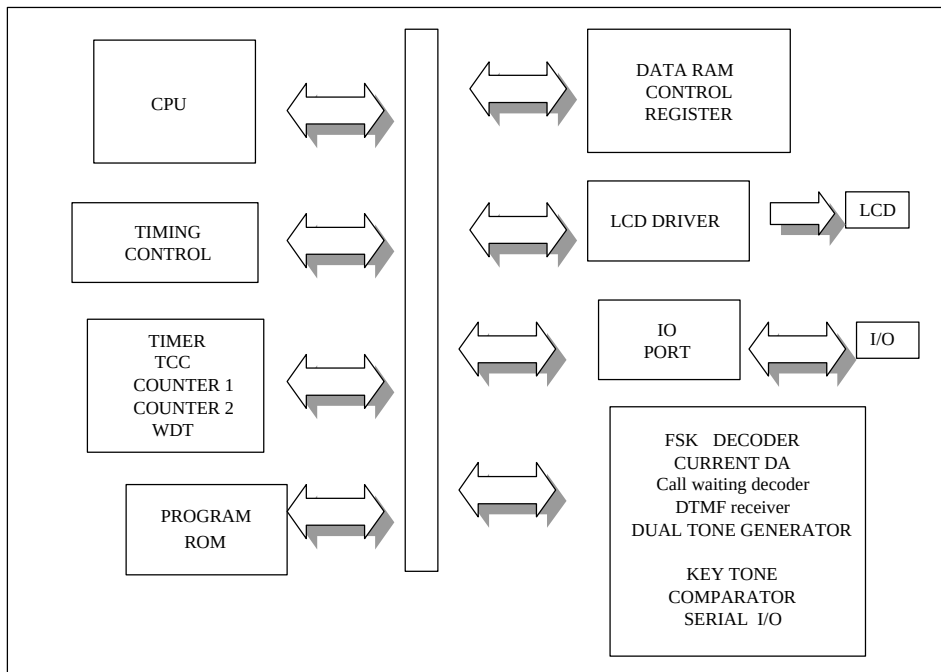


Fig.2 Block diagram1

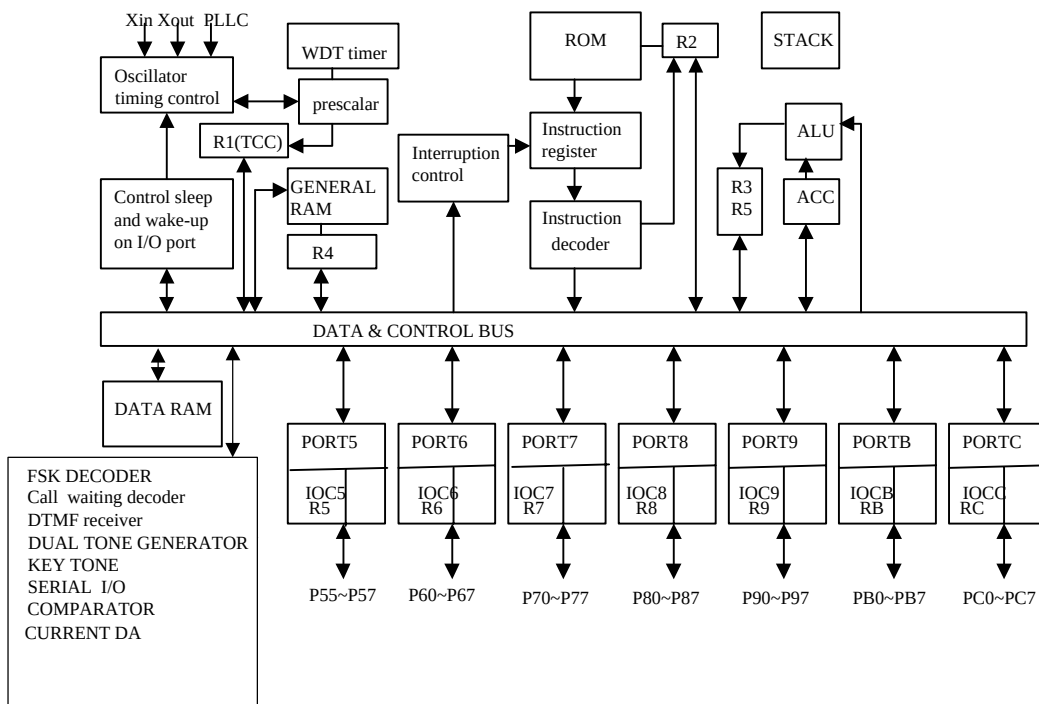


Fig.3 Block diagram2



VI.Pin Descriptions

PIN	I/O	DESCRIPTION
POWER		
VDD AVDD	POWER	Digital power Analog power They connect together when package as 128 pin QFP.
GND AVSS	POWER	Digital ground Analog ground They connect together when package as 128 pin QFP.
CLOCK		
XIN	I	Input pin for 32.768 kHz oscillator
XOUT	O	Output pin for 32.768 kHz oscillator
PLLC	I	Phase loop lock capacitor, connect a capacitor 0.01u to 0.047u with GND
LCD		
COM0..COM15	O	Common driver pins of LCD drivers
SEG0..SEG7 SEG8...SEG47 SEG48..SEG55 SEG56..SEG63 SEG64..SEG71 SEG72..SEG79	O(COM16..COM23) O O (I/O : PORTB) O (I/O : PORTC) O (I/O : PORT8) O (I/O : PORT9)	Segment driver pins of LCD drivers SEG0 to SEG7 are shared with COM16 to COM23 SEG48 to SEG79 are shared with IO PORT.
VC1..VC5	I	Reference voltage input. Each one connect a capacitor (0.1u) with GND.
FSK , TONE , KTONE		
TIP	I	Should be connected with TIP side of twisted pair lines for FSK.
RING	I	Should be connected with RING side of twisted pair lines for FSK.
TONE	O	Dual tone output pin
KTONE	O (PORT67)	Key tone output. Shared with PORT67.
CW		
CWGS	O	Gain adjustment of single-ended input OP Amp
CWIN	I	Single-ended input OP Amp for call waiting decoder
DTMF receiver		
EST	O	Early steering output. Presents a logic high immediately when the digital algorithm detects a recognizable tone-pair (signal condition). Any momentary loss of signal condition will cause EST to return to a logic low. This pin shared with PORT56.
STGT	I/O	Steering input/guard time output (bi-directional). A voltage greater than V _{tst} detected at ST causes the device to register the detected tone-pair and update the output latch. A voltage less than V _{tst} frees the device to accept a new tone-pair. The GT output acts to reset the external steering time-constant; its state is a function of EST and the voltage on ST . This pin shared with PORT55.
SERIAL IO		
SCK	IO (PORT60)	Master: output pin, Slave: input pin. This pin shared with PORT60.
SDO	O (PORT61)	Output pin for serial data transferring. This pin shared with PORT61.
SDI	I (PORT62)	Input pin for receiving data. This pin shared with PORT62.
Comparator		



CMP1	I (PORT63)	Comparator input pins. Shared with PORT63, PORT64 and PORT65.
CMP2	I (PORT64)	
CMP3	I (PORT65)	
CURRENT DA		
DAOUT	O (PORT66)	Current DA output pin. It can be a control signal for sound generating. Shared with PORT66.
IO		
P55 ~P57	I/O	PORT 5 can be INPUT or OUTPUT port each bit.
P60 ~P67	I/O	PORT 6 can be INPUT or OUTPUT port each bit. Internal pull high.
P70 ~ P77	I/O	PORT 7 can be INPUT or OUTPUT port each bit. Internal Pull high function. Auto key scan function. Interrupt function.
P80 ~ P87	I/O	PORT 8 can be INPUT or OUTPUT port each bit. Shared with LCD Segment signal.
P90 ~ P97	I/O	PORT 9 can be INPUT or OUTPUT port each bit. Shared with LCD Segment signal.
PB0 ~ PB7	I/O	PORT B can be INPUT or OUTPUT port each bit. Shared with LCD Segment signal.
PC0 ~ PC7	I/O	PORT C can be INPUT or OUTPUT port each bit. Shared with LCD Segment signal.
INT0	PORT70..73	Interrupt sources which has the same interrupt flag. Any pin from PORT70 to PORT73 has a falling edge signal, it will generate a interruption.
INT1	PORT74..76	Interrupt sources which has the same interrupt flag. Any pin from PORT74 to PORT76 has a falling edge signal, it will generate a interruption.
INT2	PORT77	Interrupt source. Once PORT77 has a falling edge or rising edge signal (controlled by CONT register), it will generate a interruption.
TEST	I	Test pin into test mode for factory test only. Connect it ground in application.
/RESET	I	Low reset

VII.Functional Descriptions

VII.1 Operational Registers

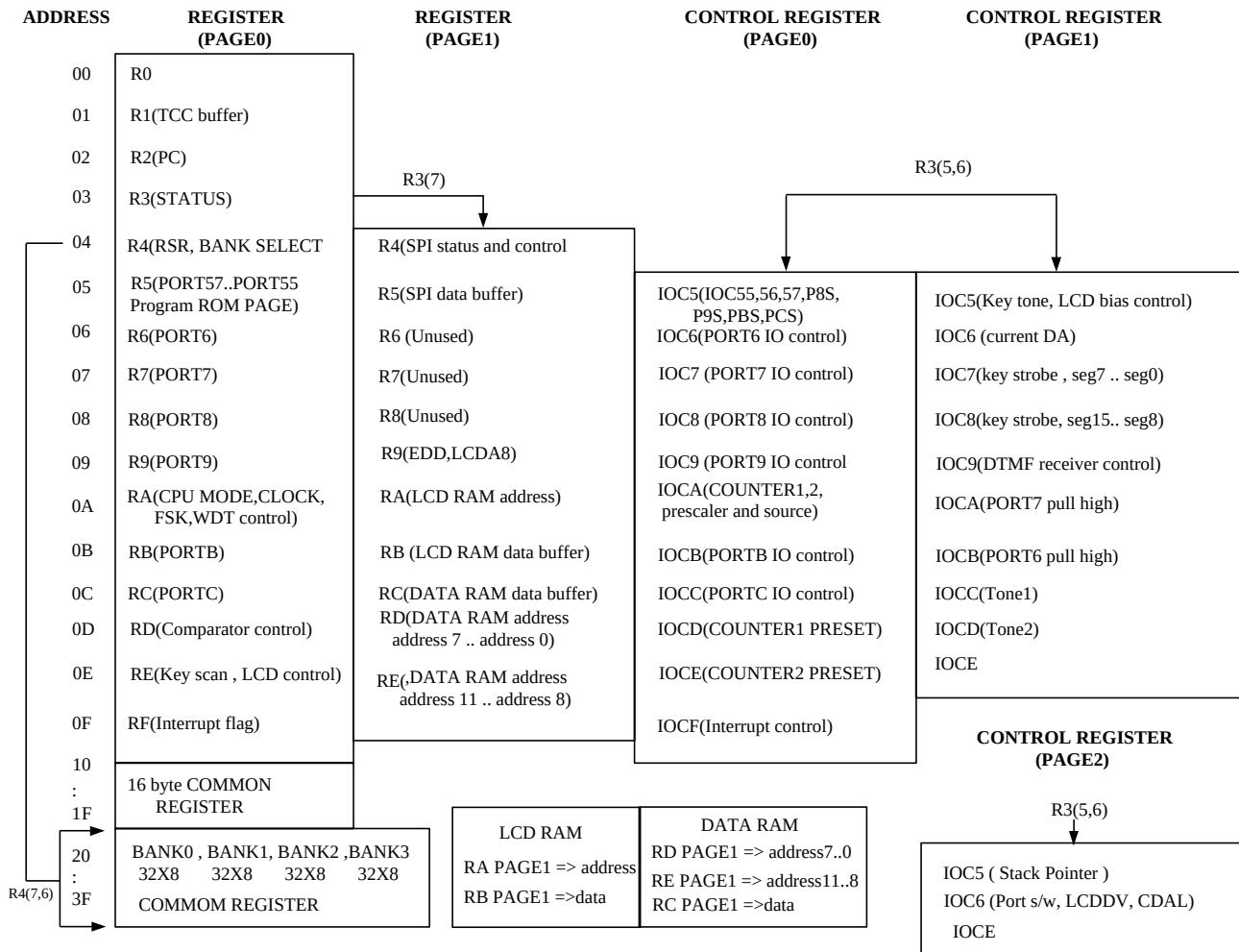


Fig.4 control register configuration

VII.2 Operational Register Detail Description

R0 (Indirect Addressing Register)

R0 is not a physically implemented register. It is useful as indirect addressing pointer. Any instruction using R0 as register actually accesses data pointed by the RAM Select Register (R4).

Example:

```
Mov a,@0x20 ;store a address at R4 for indirect addressing
Mov 0x04,A
Mov a,@0xAA ;write data 0xAA to R20 at bank0 through R0
Mov 0x00,A
```

R1 (TCC)

TCC data buffer. Increased by 16.38KHz or by the instruction cycle clock (controlled by CONT register).
Written and read by the program as any other register.

R2 (Program Counter)

The structure is depicted in Fig. 5.

Generates $32K \times 13$ on-chip PROGRAM ROM addresses to the relative programming instruction codes.

"JMP" instruction allows the direct loading of the low 10 program counter bits.

"CALL" instruction loads the low 10 bits of the PC, PC+1, and then push into the stack.

"RET" ("RETL k", "RETI") instruction loads the program counter with the contents at the top of stack.

"MOV R2,A" allows the loading of an address from the A register to the PC, and the ninth and tenth bits are cleared to "0".

"ADD R2,A" allows a relative address be added to the current PC, and contents of the ninth and tenth bits are cleared to "0".

"TBL" allows a relative address be added to the current PC, and contents of the ninth and tenth bits don't change. The most significant bit (A10~A14) will be loaded with the content of bit PS0~PS3 in the status register (R5) upon the execution of a "JMP", "CALL", "ADD R2,A", or "MOV R2,A" instruction.

If a interrupt trigger, PROGRAM ROM will jump to address8 at page0. The CPU will store ACC,R3 status and R5 PAGE automatically, it will restore after instruction RETI.

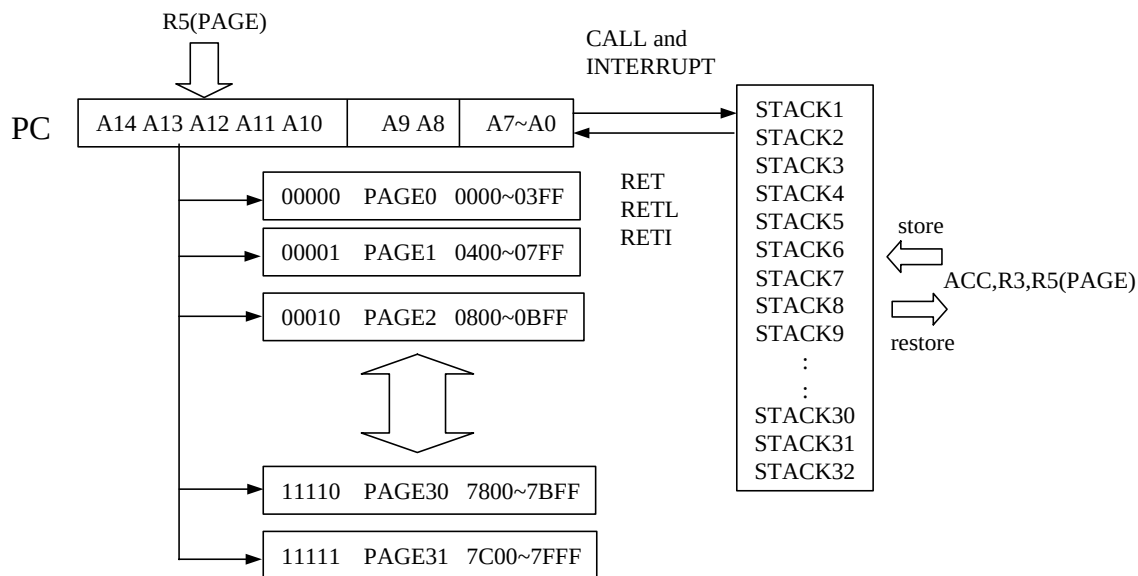


Fig.5 Program counter organization

R3 (Status Register)

7	6	5	4	3	2	1	0
PAGE	IOCP1S	IOCPAGE	T	P	Z	DC	C

Bit 0 (C) : Carry flag

Bit 1 (DC) : Auxiliary carry flag

Bit 2 (Z) : Zero flag

Bit 3 (P) : Power down bit.

Set to 1 during power on or by a "WDTC" command and reset to 0 by a "SLEP" command.

Bit 4 (T) : Time-out bit.

Set to 1 by the "SLEP" and "WDTC" command, or during power up and reset to 0 by WDT timeout.

EVENT	T	P	REMARK
WDT wake up from sleep mode	0	0	
WDT time out (not sleep mode)	0	1	
/RESET wake up from sleep	1	0	
Power up	1	1	
Low pulse on /RESET	x	X	x : don't care

Bit 5(IOC PAGE) : change IOC5 ~ IOCE to another page

Please refer to Fig.4 control register configuration for details.

0/1 → page0 / page1

Bit 6(IOC P1S) : change IOC PAGE1 and PAGE2 to another option register

Please refer to Fig.4 control register configuration for details.

0/1 → page1 /page2

Bit 6(IOC P1S)	Bit 5 (IOC PAGE)	PAGE SELECT
X	0	PAGE 0
0	1	PAGE 1
1	1	PAGE 2

Bit 7(PAGE) : change R4 ~ RE to another page

Please refer to Fig.4 control register configuration for details.

0/1 → page0 / page1

R4 (RAM selection for common registers R20 ~ R3F, SPI)

PAGE0 (RAM selection register)

7	6	5	4	3	2	1	0
RB1	RB0	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0

Bit 0 ~ Bit 5 (RSR0 ~ RSR5) : Indirect addressing for common registers R20 ~ R3F

RSR bits are used to select up to 32 registers (R20 to R3F) in the indirect addressing mode.

Bit 6 ~ Bit 7 (RB0 ~ RB1) : Bank selection bits for common registers R20 ~ R3F

These selection bits are used to determine which bank is activated among the 4 banks for 32 register (R20 to R3F)..

Please refer to Fig.4 control register configuration for details.

PAGE1 (SPI control register)

7	6	5	4	3	2	1	0
RBF	SPIE	SRO	SE	SCES	SBR2	SBR1	SBR0

Fig. 6 shows how SPI to communicate with other device by SPI module. If SPI is a master controller, it sends clock through the SCK pin. An 8-bit data is transmitted and received at the same time. If SPI, however, is defined as a slave, its SCK pin could be programmed as an input pin. Data will continue to be shifted on a basis of both the clock rate and the selected edge.

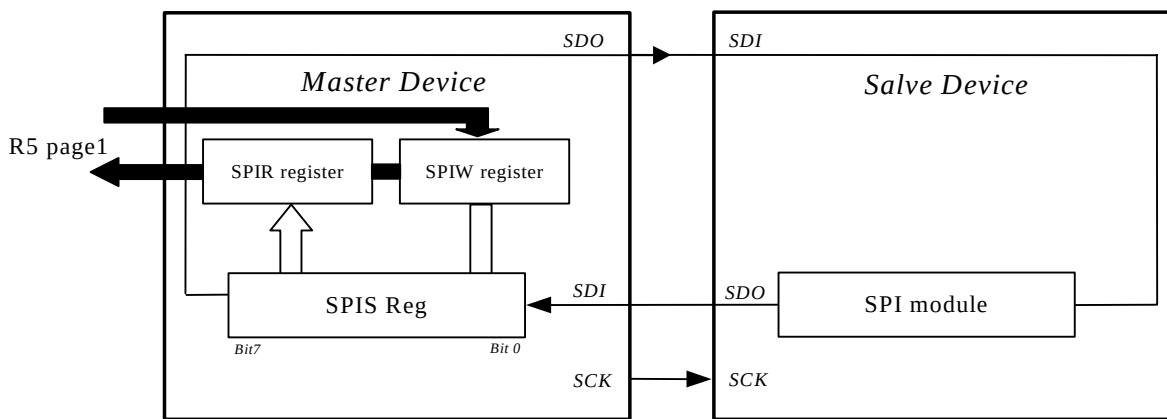


Fig.6 Single SPI Master / Slave Communication

Bit 0 ~ Bit 2 (SBR0 ~ SBR2) : SPI baud rate selection bits

SBR2	SBR1	SBR0	Mode	Baud rate
0	0	0	Master	Fsco
0	0	1	Master	Fsco/2
0	1	0	Master	Fsco/4
0	1	1	Master	Fsco/8
1	0	0	Master	Fsco/16
1	0	1	Master	Fsco/32
1	1	0	Slave	
1	1	1	X	

<Note> F_{sco} = CPU instruction clock

For example :

If PLL enable and RA PAGE0 (Bit5, Bit4)=(1,1), instruction clock is $3.58\text{MHz}/2 \rightarrow F_{\text{SCO}}=3.5862\text{MHz}/2$

If PLL enable and RA PAGE0 (Bit5, Bit4)=(0,0), instruction clock is $0.895\text{MHz}/2 \rightarrow F_{\text{SCO}}=0.895\text{MHz}/2$

If PLL disable, instruction clock is $32.768\text{kHz}/2 \rightarrow F_{\text{sc}} = 32.768\text{kHz}/2$.

Bit 3 (SCES) : SPI clock edge selection bit

1→Data shifts out on falling edge, and shifts in on rising edge. Data is hold during the high level.

0→Data shifts out on rising edge, and shifts in on falling edge. Data is hold during the low level.

Bit 4 (SE) : SPI shift enable bit

1 → Start to shift, and keep on 1 while the current byte is still being transmitted.

0 → Reset as soon as the shifting is complete, and the next byte is ready to shift.

<Note> This bit has to be reset in software.

Bit 5 (SRO) : SPI read overflow bit

1 ➔ A new data is received while the previous data is still being hold in the SPIB register. In this situation, the data in SPIS register will be destroyed. To avoid setting this bit, users had better to read SPIB register even if the transmission is implemented only.

0 $\Rightarrow$ No overflow

<Note> This can only occur in slave mode.

Bit 6 (SPIE) : SPI enable bit

1 ➔ Enable SPI mode

0 ➔ Disable SPI mode

Bit 7 (RBF) : SPI read buffer full flag

1 → Receive is finished, SPIB is full.

0 ➔ Receive is not finish yet, SPIB is empty.

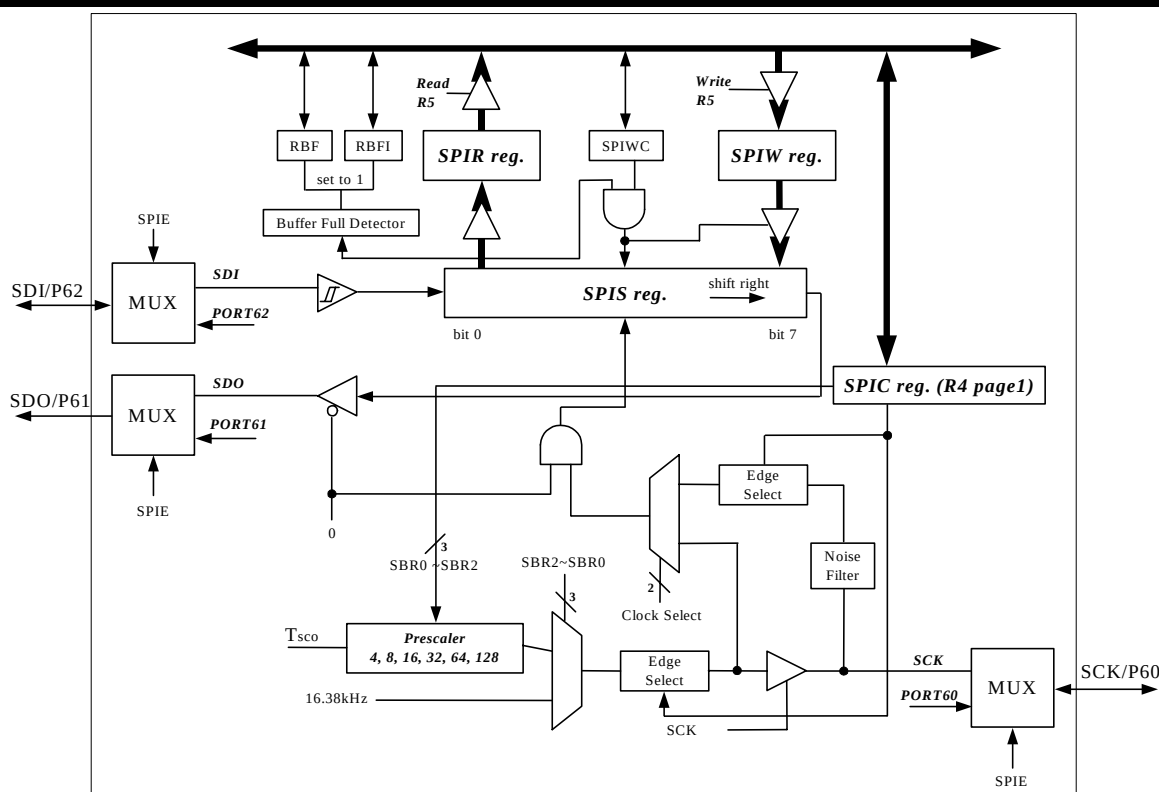


Fig.7 SPI structure

SPIC reg. : SPI control register

SDO/P61 : Serial data out

SDI/P62 : Serial data in

SCK/P60 : Serial clock

RBF : Set by buffer full detector, and reset in software.

RBFI : Interrupt flag. Set by buffer full detector, and reset in software.

Buffer Full Detector : Sets to 1, while an 8-bit shifting is complete.

SE : Loads the data in SPIW register, and begin to shift

SPIE : SPI control register

SPIS reg. : Shifting byte out and in. The MSB will be shifted first. Both the SPIS register and the SPIW register are loaded at the same time. Once data being written to, SPIS starts transmission / reception. The received data will be moved to the SPIR register, as the shifting of the 8-bit data is complete. The RBF (Read Buffer Full) flag and the RBFi(Read Buffer Full Interrupt) flag are set.

SPIR reg. : Read buffer. The buffer will be updated as the 8-bit shifting is complete. The data must be read before the next reception is finished. The RBF flag is cleared as the SPIR register read.

SPIW reg. : Write buffer. The buffer will deny any write until the 8-bit shifting is complete. The SE bit will be kept in 1 if the communication is still under going. This flag must be cleared as the shifting is finished. Users can determine if the next write attempt is available.

SBR2 ~ SBR0: Programming the clock frequency/rates and sources.

Clock select : Selecting either the internal instruction clock or the external 16.338KHz clock as the shifting clock.

Edge Select : Selecting the appropriate clock edges by programming the SCES bit

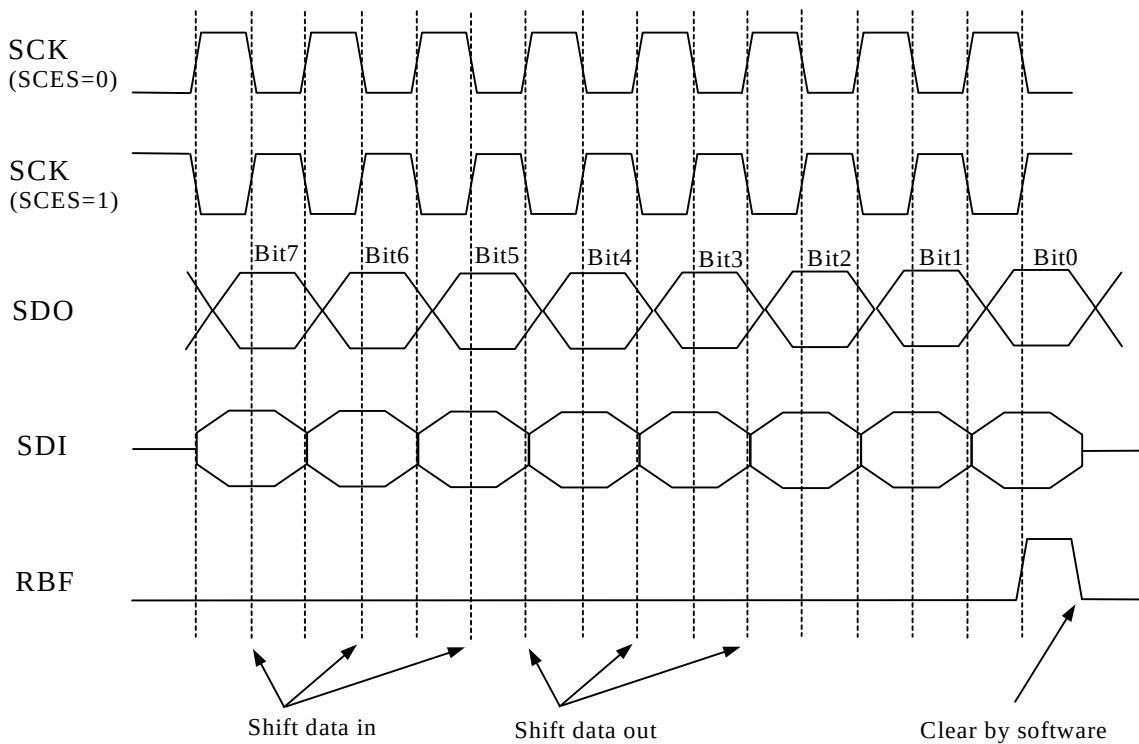


Fig.8 SPI timing

R5 (PORT5 I/O data, Program page selection, SPI data)

PAGE0 (PORT5 I/O data register, Program page register)

7	6	5	4	3	2	1	0
R57	R56	R55	PS4	PS3	PS2	PS1	PS0

Bit 0 ~ Bit 4 (PS0 ~ PS4) : Program page selection bits

PS4	PS3	PS2	PS1	PS0	Program memory page (Address)
0	0	0	0	0	Page 0
0	0	0	0	1	Page 1
0	0	0	1	0	Page 2
0	0	0	1	1	Page 3
:	:	:	:	:	:
:	:	:	:	:	:
1	1	1	1	0	Page 30
1	1	1	1	1	Page 31

User can use PAGE instruction to change page to maintain program page by user. Otherwise, user can use far jump (FJMP) or far call (FCALL) instructions to program user's code. And the program page is maintained by EMC's compiler. It will change user's program by inserting instructions within program.

Bit 5 ~ Bit 6 (P55 ~ P57) : 3-bit PORT5(5~7) I/O data register

User can use IOC register to define input or output each bit.

**PAGE1 (SPI data buffer)**

7	6	5	4	3	2	1	0
SPIB7	SPIB6	SPIB5	SPIB4	SPIB3	SPIB2	SPIB1	SPIB0

Bit 0 ~ Bit 7 (SPIB0 ~ SPIB7) : SPI data buffer

If you write data to this register, the data will write to SPIW register. If you read this data, it will read the data from SPIR register. Please refer to figure7

R6 (PORT6 I/O data)**PAGE0 (PORT6 I/O data register)**

7	6	5	4	3	2	1	0
P67	P66	P65	P64	P63	P62	P61	P60

Bit 0 ~ Bit 7 (P60 ~ P67) : 8-bit PORT6(0~7) I/O data register

User can use IOC register to define input or output each bit..

PAGE1 (Unused)

7	6	5	4	3	2	1	0

Bit 0 ~ Bit 7 : unused

R7 (PORT7 I/O data)**PAGE0 (PORT7 I/O data register)**

7	6	5	4	3	2	1	0
P77	P76	P75	P74	P73	P72	P71	P70

Bit 0 ~ Bit 7 (P70 ~ P77) : 8-bit PORT7(0~7) I/O data register

User can use IOC register to define input or output each bit.

PAGE1 (Unused)

7	6	5	4	3	2	1	0

Bit 0 ~ Bit 7 : unused

R8 (PORT8 I/O data)**PAGE0 (PORT8 I/O data register)**

7	6	5	4	3	2	1	0
P87	P86	P85	P84	P83	P82	P81	P80

Bit 0 ~ Bit 7 (P80 ~ P87) : 8-bit PORT8 (0~7) I/O data register

User can use IOC register to define input or output each bit.

PAGE1 (Unused)

7	6	5	4	3	2	1	0

Bit 0 ~ Bit 7 : unused



R9 (PORT9 I/O data, extra LCD address bit)

PAGE0 (PORT9 I/O data register)

7	6	5	4	3	2	1	0
P97	P96	P95	P94	P93	P92	P91	P90

Bit 0 ~ Bit 7 (P90 ~ P97) : 8-bit PORT9 (0~7) I/O data register

User can use IOC register to define input or output each bit.

PAGE1 (LCD address MSB bit)

7	6	5	4	3	2	1	0
LCDA8							

Bit 0 ~ Bit 6 : unused

Bit 7 (LCDA8) : MSB of LCD address for LCD RAM reading or writing

Other LCD address bits LCDA7 ~ LCDA0 are set from RA PAGE1 Bit 7 ~ Bit 0.

For LCD address access over 0xFFH, set this bit to "1"; otherwise set this bit to "0".

RA (CPU power saving, PLL, Main clock selection, FSK, Watchdog timer, LCD address)

PAGE0 (CPU power saving bit, PLL, Main clock selection bits, FSK , Watchdog timer enable bit)

7	6	5	4	3	2	1	0
SLEEP_N	PLLEN	CLK1	CLK0	FSKPWR	FSKDATA	/CD	WDTEN

Bit 0 (WDTEN) : Watch dog control register

User can use WDTC instruction to clear watch dog counter. The counter 's clock source is 32768/2 Hz. If the prescaler assigns to TCC. Watch dog will time out by $(1/32768) * 2 * 256 = 15.616\text{ms}$. If the prescaler assigns to WDT, the time of time out will be more times depending on the ratio of prescaler.

0/1 → disable/enable

Bit 1 (/CD) : FSK carrier detect indication

0/1 → Carrier Valid/Carrier Invalid

It's a read only signal. If FSK decoder detect the energy of mark or space signal. The Carrier signal will go to low level. Otherwise it will go to high.. Note!! Should be at normal mode.

Bit 2 (FSKDATA) : FSK decoding data output

It's a read only signal. If FSK decode the mark or space signal , it will output high level signal or low level signal at this register. It's a raw data type. That means the decoder just decode the signal and has no process on FSK signal. Note!! Should be at normal mode.

User can use FSK data falling edge interrupt function to help data decoding.

Ex:

MOV A,@01000000

IOW IOCF ;enable FSK interrupt function

CLR RF

ENI ;wait for FSK data's falling edge

:

0 = Space data (2200Hz)

1 = Mark data (1200Hz)

Bit 3 (FSKPWR) : FSK power control

0/1 → FSK decoder powered down / FSK decoder powered up

It's the control register of FSK block power. **For DTMF power up, be sure FSK powered down. (IOC9 PAGE1 bit7 set 1, this bit be set to 0)**

The relation between bit 1 to bit 3 is shown in Fig.9. You have to power FSK decoder up first, then wait a setup time (Tsup) and check carrier signal (/CD). If the carrier is low, program can process the FSK data.

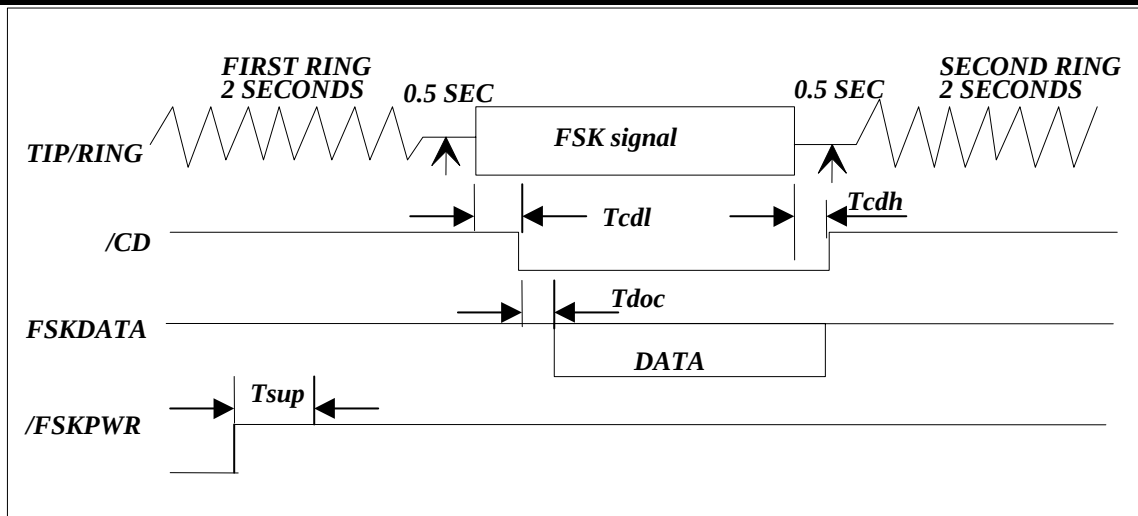


Fig.9 The relation between bit 1 ~ bit 3

The controller is a CMOS device designed to support the Caller Number Deliver feature which is offered by the Regional Bell Operating Companies. The FSK block comprises one path: the signal path. The signal path consist of an input differential buffer, a band pass filter, an FSK demodulator and a data valid with carrier detect circuit.

In a typical application, user can use his own external ring detect output as a triggering input to IO port. User can use this signal to wake up whole chip by external ring detect signal.

By setting "1" to bit 3 (FSKPWR) of register RA to activate the block of FSK decoder. If bit 3 (FSKPWR) of register RA is set to "0", the block of FSK decoder will be powered down.

The input buffer accepts a differential AC coupled input signal through the TIP and RING input and feeds this signal to a band pass filter. Once the signal is filtered, the FSK demodulator decodes the information and sends it to a post filter. The output data is then made available at bit 2 (FSKDATA) of register RA. This data, as sent by the central office, includes the header information (alternate "1" and "0") and 150 ms of marking which precedes the date, time and calling number. If no data is present, the bit 2 (DATA) of register RA is held on "1" state. This is accomplished by an carrier detect circuit which determines if the in-band energy is high enough. If the incoming signal is valid, bit 1 (/CD) of register RA will be "0" otherwise it will be held on "1". And thus the demodulated data is transferred to bit 2 (DATA) of register RA. If it is not, then the FSK demodulator is blocked.

Bit 4 ~ Bit 5 (CLK0 ~ CLK1) : Main clock selection bits

User can choose different frequency of main clock by CLK1 and CLK2. All the clock selection is list below.

PLLEN	CLK1	CLK0	Sub clock	MAIN clock	CPU clock
1	0	0	32.768kHz	895.658kHz	895.658kHz (Normal mode)
1	0	1	32.768kHz	1.7913MHz	1.7913MHz (Normal mode)
1	1	0	32.768kHz	10.7479MHz	10.7479MHz (Normal mode)
1	1	1	32.768kHz	3.5826MHz	3.5826MHz (Normal mode)
0	Don't care	don't care	32.768kHz	Don't care	32.768kHz (Green mode)
0	Don't care	don't care	32.768kHz	Don't care	32.768kHz (Green mode)
0	Don't care	don't care	32.768kHz	Don't care	32.768kHz (Green mode)
0	Don't care	don't care	32.768kHz	Don't care	32.768kHz (Green mode)

Bit 6 (PLLEN) : PLL enable control bit

It is CPU mode control register. If PLL is enabled, CPU will operate at normal mode (high frequency, main clock); otherwise, it will run at green mode (low frequency, 32768 Hz).

0/1 → disable/enable

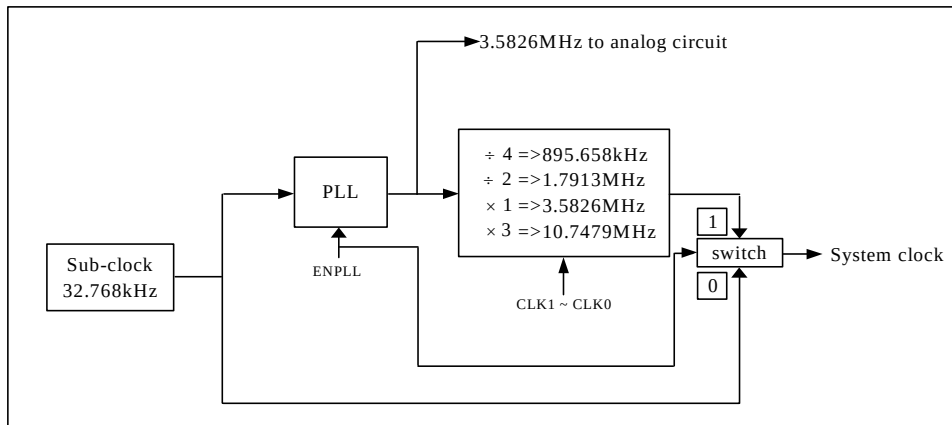


Fig.10 The relation between 32.768kHz and PLL

Bit 7(SLEEP_N) : Power saving mode control register

When PLL is disabled, user can set this bit after using "SLEP" instruction for SLEEP mode or IDLE mode selection

0 → SLEEP mode

1 → Don't allowed this setting

This bit will decide SLEP instruction which mode to go.

The status after wake-up and the wake-up sources list as the table below.

Wakeup signal	SLEEP mode	GREEN mode	NORMAL mode
	RA(7,6)=(0,0) + SLEP	RA(7,6)=(x,0) no SLEP	RA(7,6)=(x,1) no SLEP
TCC time out IOCF bit 0=1 And "ENI"	No function	Interrupt (jump to address 8 at page0)	Interrupt (jump to address 8 at page0)
COUNTER1 time out IOCF bit 1=1 And "ENI"	No function	Interrupt (jump to address 8 at page0)	Interrupt (jump to address 8 at page0)
COUNTER2 time out IOCF bit 2=1 And "ENI"	No function	Interrupt (jump to address 8 at page0)	Interrupt (jump to address 8 at page0)
WDT time out	RESET and Jump to address 0	RESET and Jump to address 0	RESET and Jump to address 0
PORT7 IOCF bit3 or bit4 or bit5 = 1 And "ENI"	RESET and Jump to address 0	Interrupt (jump to address 8 at page0)	Interrupt (jump to address 8 at page0)
IOCE page2 bit 6 = 1 And RE page1 bit6 logic level variation (switch by EDGE bit) And "ENI"	No function	Interrupt (jump to address 8 at page0)	Interrupt (jump to address 8 at page0)
Stack overflow IOC5 page2 bit7=1 &bit 6: 0 → 1 And "ENI"	No function	Interrupt (jump to address 8 at page0)	Interrupt (jump to address 8 at page0)

<Note> Stack overflow interrupt function is exist in ROM less and OTP chip only.

<Note> PORT70 ~ PORT73 's wakeup function is controlled by IOCF bit3 and ENI instruction. They are falling edge trigger.

PORT74 ~ PORT76 's wakeup function is controlled by IOCF bit4 and ENI instruction. They are falling edge trigger.



PORT77's wakeup function is controlled by IOCF bit5 and ENI instruction. It's falling edge or rising edge trigger (controlled by CONT register).

PAGE1 (LCD address)

7	6	5	4	3	2	1	0
LCDA7	LCDA6	LCDA5	LCDA 4	LCDA 3	LCDA 2	LCDA 1	LCDA 0

Bit 0 ~ Bit 7 (LCDA0 ~ LCDA7) : LCD address for LCD RAM reading or writing

The data in the LCD RAM correspond to the COMMON and SEGMENT signals as the table .

COM23 ~ COM16 (set R9 PAGE1 bit7=1)	COM15 ~COM8 (set R9 PAGE1 bit7=0)	COM7 ~ COM0 (set R9 PAGE1 bit7=0)	
Address 100H	Address 80H	Address 00H	SEG0
Address 101H	Address 81H	Address 01H	SEG1
Address 102H	Address 82H	Address 02H	SEG1
:	:	:	:
:	:	:	:
:	:	:	:
Address 14EH	Address CEH	Address 4EH	SEG78
Address 14FH	Address CFH	Address 4FH	SEG79
Address 150H	Address D0H	Address 50H	Empty
:	:	:	:
Address 17FH	Address FFH	Address 7FH	Empty

RB (PORTB I/O data, LCD data)

PAGE0 (PORTB I/O data register)

7	6	5	4	3	2	1	0
PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0

Bit 0 ~ Bit 7 (PB0 ~ PB7) : 8-bit PORTB(0~7) I/O data register

User can use IOC register to define input or output each bit.

PAGE1 (LCD data buffer)

7	6	5	4	3	2	1	0
LCDD7	LCDD6	LCDD5	LCDD4	LCDD3	LCDD2	LCDD1	LCDD0

Bit 0 ~ Bit 7 (LCDD0 ~ LCDD7) : LCD data buffer for LCD RAM reading or writing

Example.

```
MOV    A,@0
MOV    R9_PAGE1,A
MOV    RA_PAGE1,A      ;ADDRESS
MOV    A,@0XAA
MOV    RB_PAGE1,A      ;WRITE DATA 0XAA TO LCD RAM
MOV    A,RB_PAGE1      ;READ DATA FROM LCD RAM
:
```

RC (PORTC I/O data, Data RAM data)

PAGE0 (PORTC I/O data register)

7	6	5	4	3	2	1	0
PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0

Bit 0 ~ Bit 7 (PC0 ~ PC7) : 8-bit PORTC(0~7) I/O data register

User can use IOC register to define input or output each bit.

PAGE1 (Data RAM data buffer)



7	6	5	4	3	2	1	0
RAMD7	RAMD6	RAMD5	RAMD4	RAMD3	RAMD2	RAMD1	RAMD0

Bit 0 ~ Bit 7 (RAMD0 ~ RAMD7) : Data RAM data buffer for RAM reading or writing.

Ex.

```
MOV    A , @1
MOV    RD_PAGE1 , A
MOV    A , @0
MOV    RE_PAGE1 , A
MOV    A , @0x55
MOV    RC_PAGE1 , A      ;write data 0x55 to DATA RAM which address is "0001".
MOV    A , RC_PAGE1     ;read data
:
```

RD (Comparator control, Data RAM address(0 ~ 7))

PAGE0 (Comparator control bits)

7	6	5	4	3	2	1	0
CMPEN	CMPFLAG	CMPS1	CMPS0	CMP_B3	CMP_B2	CMP_B1	CMP_B0

If user define PORT63 , PORT64 or PORT65 (by CMPIN1, CMPIN2, CMPIN3 at IOCE page1) as a comparator input or PORT6. User can use this register to control comparator's function.

Bit 0~Bit 3(CMP_B0~CMP_B3) : Reference voltage selection of internal bias circuit for comparator.

Reference voltage for comparator = $VDD \times (n + 0.5) / 16$, n = 0 to 15

Bit 4~Bit 5(CMPS0~CMPS1) : Channel selection from CMP1 to CMP3 for comparator

CMPS1	CMPS0	Input
0	0	CMP1
0	1	CMP2
1	0	CMP3
1	1	Reserved

Bit 6(CMPFLAG) : Comparator output flag

0 → Input voltage < reference voltage

1 → Input voltage > reference voltage

Bit 7(CMPEN) : Enable control bit of comparator.

0/1 → disable/enable, When this bit is set to "0", 2.0V ref circuit is also powered off.

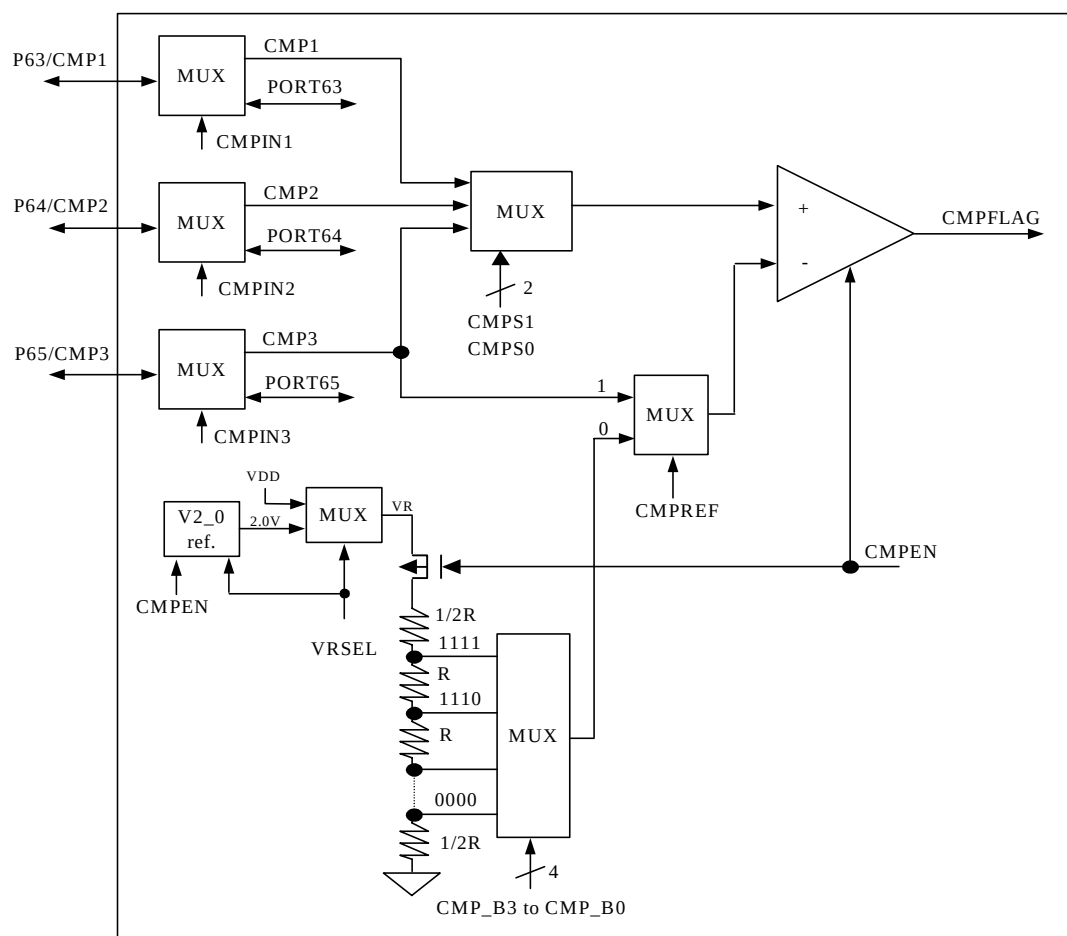


Fig.11 Comparator circuit

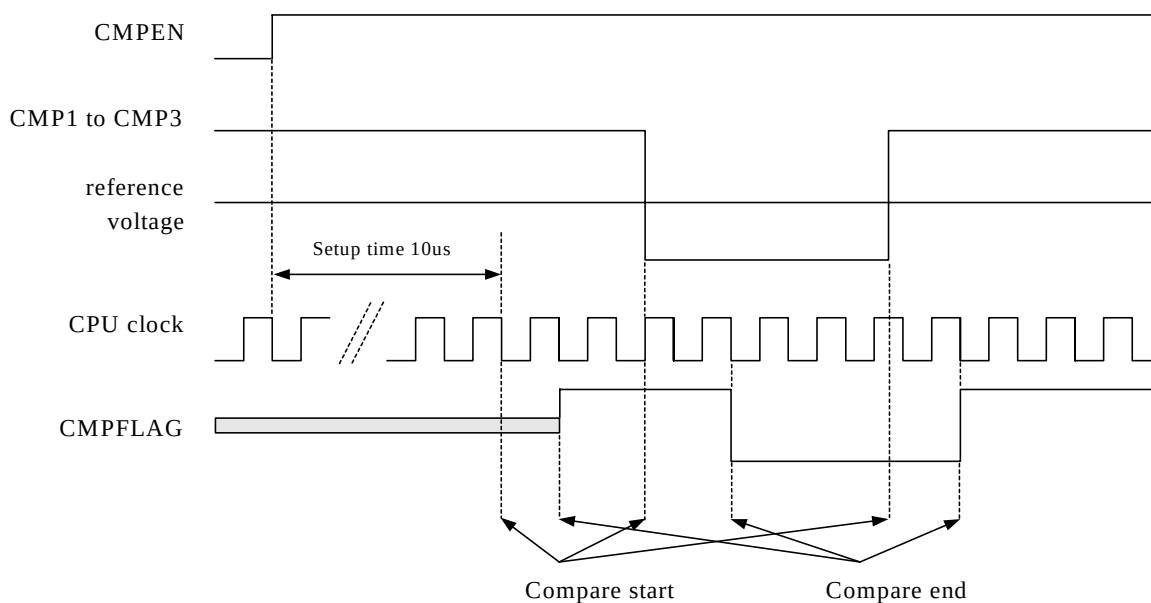


Fig.12 Comparator timing



PAGE1 (Data RAM address0 ~ address7)

7	6	5	4	3	2	1	0
RAMA7	RAMA6	RAMA5	RAMA4	RAMA3	RAMA2	RAMA1	RAMA0

Bit 0~Bit 7(RAMA0~RAMA7) : Data RAM address (address0 to address7) for RAM reading or writing

RE (CAS, Key scan, LCD control, Data RAM address(8 ~ 11))

PAGE0 (Key scan control, LCD control)

7	6	5	4	3	2	1	0
CAS	KEYCHK	KEYSTRB	KEYSCAN	LCD1	LCD0	LCDM1	LCDM0

Bit 0~Bit 1(LCDM0~LCDM1) : LCD common mode, bias select and COM/SEG switch control bits

LCDM1, LCDM0	COM output mode	LCD bias	COM/SEG switch
0,0	16 common	1/4 bias	SEG0 ~ SEG7 select
0,1	9 common	1/4 bias	SEG0 ~ SEG7 select
1,0	8 common	1/4 bias	SEG0 ~ SEG7 select
1,1	24 common	1/5 bias	COM16 ~ COM23 select

<Note> When 8, 9 and 16 LCD common mode is set, COM16/SEG0 pin ~ COM23/SEG7 pin are also set to SEG0 ~ SEG7 and LCD bias is 1/4 bias. When 24 LCD common mode is set, COM16/SEG0 pin ~ COM23/SEG7 pin are also set to COM16 ~ COM23 and LCD bias is 1/5 bias.

Bit 2~Bit 3 (LCD0~LCD1) : LCD operation function definition.

LCD1, LCD0	LCD operation
0,0	Disable
0,1	Blanking
1,0	Reserved
1,1	LCD enable

<Note> Key strobe and Key check functions should be normal operating whenever LCD is enabled or disabled.

The controller can drive LCD directly. LCD block is made up of LCD driver, display RAM, segment output pins, common output pins and LCD operating bias pins.

Duty, the number of segment, the number of common and frame frequency are determined by LCD mode register RE PAGE0 Bit 0~ Bit 1.

When 8, 9 or 16 LCD commons are used, LCD operating bias pins VC1, VC2, VC4 and VC5 need to be connected 0.1uF capacitors to the ground (VC3 is not necessary). When 24 LCD common is used, all LCD operating bias pins VC1 ~ VC5 need to be connected 0.1uF capacitors to the ground.

LCD driver can be controlled as different driving ability (refer to IOC6 PAGE1 Option-B register).

The basic structure contains a timing control which uses the basic frequency 32.768kHz to generate the proper timing for different duty and display access. RE PAGE1 register is a command register for LCD driver and display. The LCD display (disable, enable, blanking) is controlled by RE PAGE0 Bit 2 ~ Bit 3 and the driving duty is decided by RE PAGE Bit 0 ~ Bit 2. LCD display data is stored in data RAM which address and data access controlled by registers R9, RA PAGE1 and RB PAGE1.

User can regulate the contrast of LCD display by IOC5 PAGE1 (BIAS3..BIAS0). Up to 16 levels contrast is convenient for better display. And the internal voltage follower can afford large driving source.

COM signal : The number of COM pins varies according to the duty cycle used, as following:

In 1/8 duty mode COM8 ~ COM15 must be open.

In 1/9 duty mode COM9~ COM15 must be open

In 1/16 duty mode COM0 ~ COM15 pins must be used.

In 1/24 duty mode COM0 ~ COM23 pins must be used.

duty	COM0 ~ COM7	COM8	COM9	..	COM15	COM15 ~ COM23
1/8	o	X	x	..	x	x
1/9	o	O	x	..	x	x
1/16	o	O	o	..	o	x
1/24	o	O	o	..	o	o

x : open, o : select

SEG signal : The segment signal pins are connected to the corresponding display RAM. The high byte to the low byte Bit 0 ~ Bit 7 are correlated to COM0 ~ COM23 respectively . When a bit of display RAM is 1, a select signal is sent to the corresponding segment pin, and when the bit is 0 , a non-select signal is sent to the corresponding segment pin.

Bit 4(KEYSCAN) : Key scan function enable control bit

0/1 → disable/enable

If you enable key scan function LCD waveform will has a small pulse within a period like Fig.13.

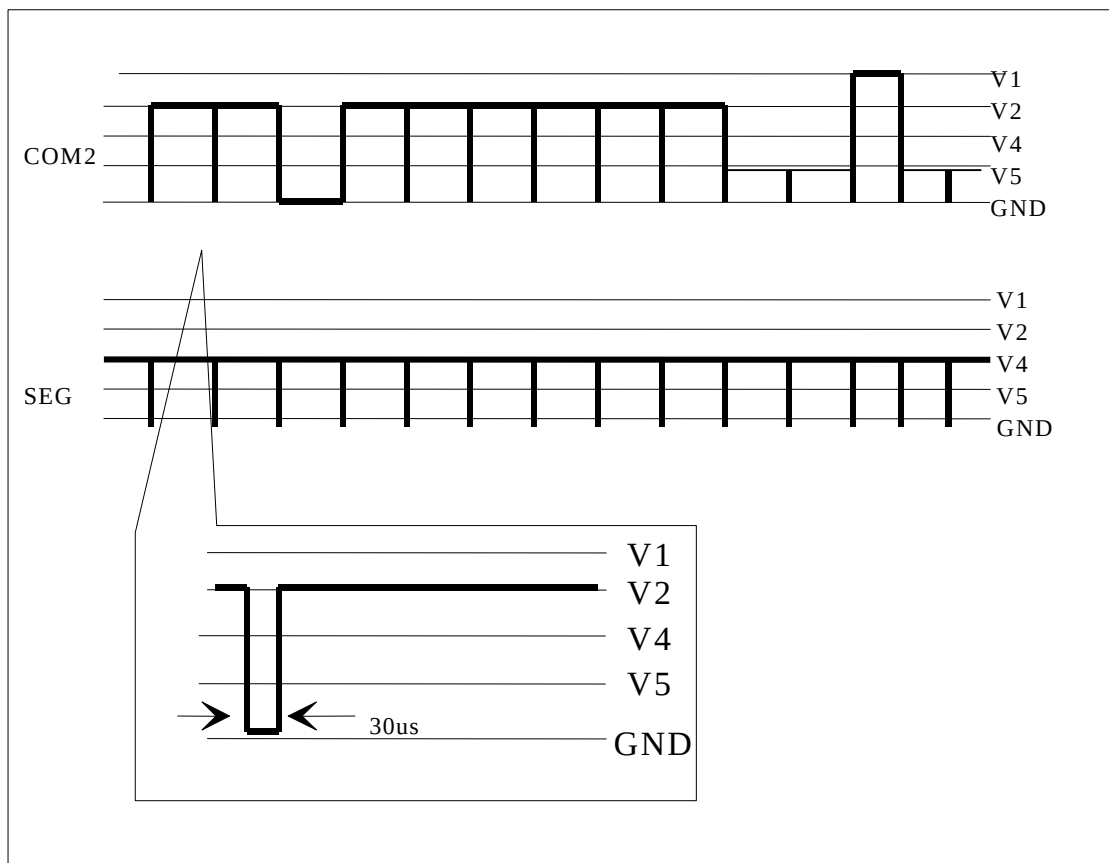


Fig.13. key scan waveform for 1/8, 1/9, 1/16 duty

Bit 5(KEYSTRB) : Key strobe enable control bit

0/1 → disable/enable

key strobe signal , if you set this bit , segment will switch to strobe signal temporally and output zero signal (one instruction long) one by one from segment 8 to segment 23. During one segment strobe time, CPU will check port7(0:3) equal to "1111" or not. If not, CPU will latch a zero at IOC7 PAGE1 and IOC8 PAGE1 one by one depends on which segment strobe.

After strobe, this bit will be cleared . Fig.14 is key strobe signal.

One instruction

	REGISTER	IOC7(0)	IOC7(1)	IOC7(2)	IOC7(3)	IOC7(4)	IOC7(5)	IOC7(6)	IOC7(7)	IOC8(0)	IOC8(1)	IOC8(2)	IOC8(3)	IOC8(4)	IOC8(5)	IOC8(6)	IOC8(7)
STROBE																	
SEG8	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
SEG9	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
SEG10	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
SEG11	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
SEG12	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
SEG13	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
SEG14	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1
SEG15	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1
SEG16	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1
SEG17	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
SEG18	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1
SEG19	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1
SEG20	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
SEG21	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1
SEG22	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
SEG23	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

Fig.14 key strobe signal

Bit 6(KEYCHK) : Key check enable control bit

0 → disable key check function.

1 → enable key check function. SEG8 to SEG23 will keep low level.

Figure 15 is relationship between KEYSKAN, KEYSTROBE , KETCHECK and segments.

And figure 16 is key scan flow by interrupt trigger.

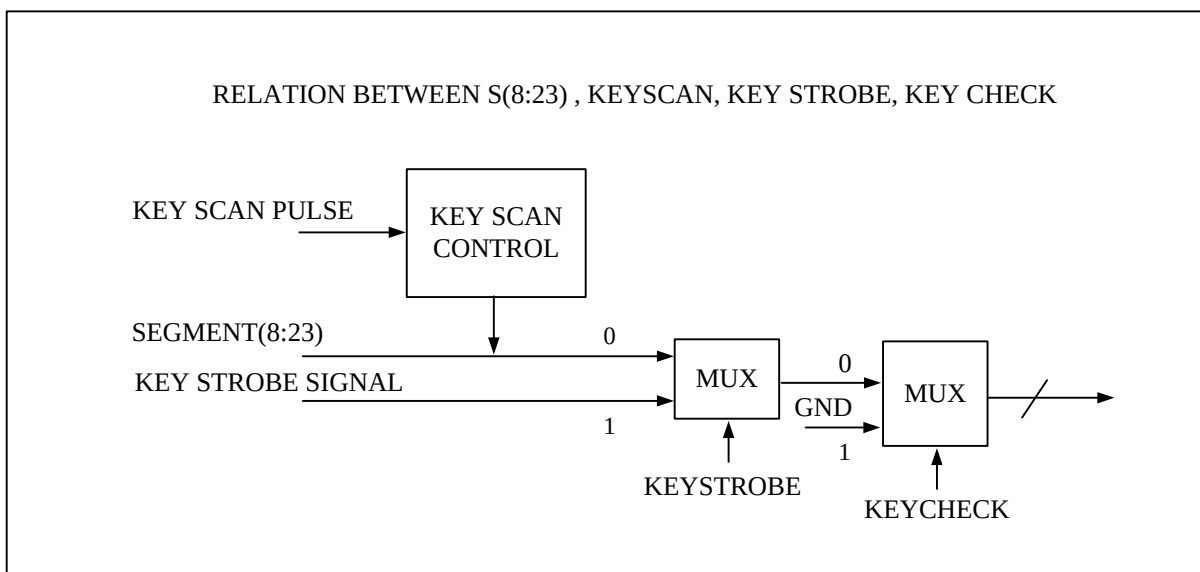


Fig.15 KEYSKAN, KEYSTROBE , KEYCHECK and segments.

Bit 7(CAS) : CALL WAITING decoding output

0/1 → CW data valid / No data

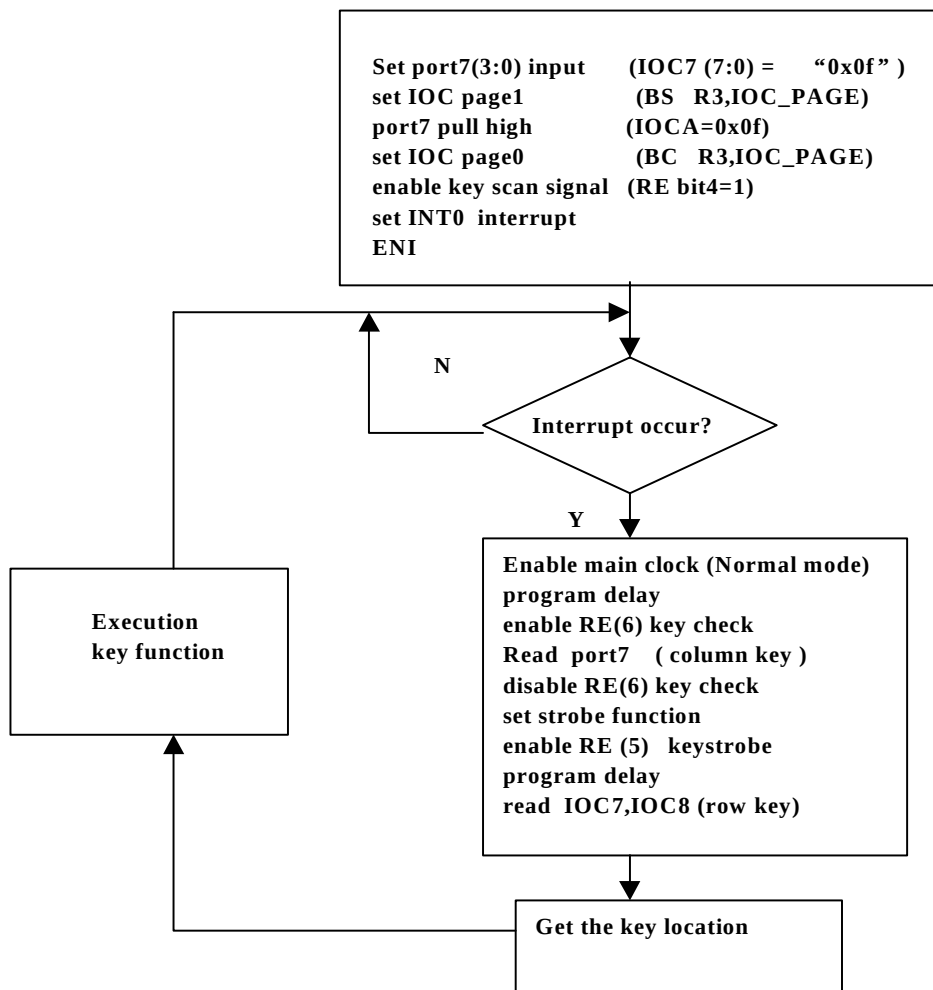


Fig.16 key scan flow by interrupt trigger

PAGE1 (Data RAM address8 ~ address11)

7	6	5	4	3	2	1	0
				RAMA11	RAMA10	RAMA9	RAMA8

Bit 0~Bit 3(RAMA8~RAMA11) : Data RAM address (address8 to address11) for RAM reading.

Bit 4~Bit5 : unused

Bit 6:unused

Bit 7 :unused

RF (Interrupt flags)

7	6	5	4	3	2	1	0
RBF/SDT	FSK/CW	INT2	INT1	INT0	CNT2	CNT1	TCIF

"1" means interrupt request, "0" means non-interrupt

Bit 0(TCIF) : TCC timer overflow interrupt flag

Set when TCC timer overflows .

Bit 1(CNT1) : Counter1 timer overflow interrupt flag

Set when counter1 timer overflows.

Bit 2(CNT2) : Counter2 timer overflow interrupt flag

Set when counter2 timer overflows .

Bit 3(INT0) : External INT0 pin interrupt flag

If PORT70 ,PORT71,PORT72 or PORT73 has a falling edge trigger signal. CPU will set this bit.

Bit 4(INT1) : External INT1 pin interrupt flag

If PORT74 ,PORT75 or PORT76 has a falling edge trigger signal. CPU will set this bit.

Bit 5(INT2) : External INT2 pin interrupt flag

If PORT77 has a falling edge or rising edge (controlled by CONT register) trigger signal. CPU will set this bit.

Bit 6(FSK/CW) : FSK data or Call waiting data interrupt flag.

If FSKDATA or CAS has a falling edge trigger signal, CPU will set this bit.

Bit 7(RBF/STD) : SPI data transfer complete or DTMF receiver signal valid interrupt

If serial IO 's RBF signal has a rising edge signal (RBF set to "1" when transfer data completely), CPU will set this bit. Or DTMF receiver's STD signal has a rising edge signal (DTMF decode a DTMF signal).

IOCF is the interrupt mask register. User can read and clear.

Trigger edge as the table

Signal	Trigger	<Note>
TCC	Time out	
COUNTER1	Time out	
COUNTER2	Time out	
INT0	Falling edge	
INT1	Falling edge	
INT2	Falling/Falling & rising edge	Controlled by CONT register
FSK	Falling edge	
RBF/STD	Rising edge	

R10~R3F (General Purpose Register)

R10~R3F (Banks 0 ~ 3) : All of them are general purpose registers.

VII.2 Special Purpose Registers

A (Accumulator)

Internal data transfer, or instruction operand holding

It's not an addressable register.

CONT (Control Register)

7	6	5	4	3	2	1	0
INT_EDGE	INT	TS		PAB	PSR2	PSR1	PSR0

Bit 0~Bit 2(PSR0~PSR2) : TCC/WDT prescaler bits

PSR2	PSR1	PSR0	TCC rate	WDT rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

Bit 3(PAB) : Prescaler assignment bit

0/1 → TCC/WDT

Bit 4 : unused

Bit 5(TS) : TCC signal source

0 → Instruction clock

1 → 16.384kHz

Instruction clock = MCU clock/2, Refer to RA Bit 4 ~ Bit 6 for PLL and Main clock selection. See fg.17.

Bit 6(INT) : INT enable flag

- 0 → interrupt masked by DISI or hardware interrupt
- 1 → interrupt enabled by ENI/RETI instructions

Bit 7(INT_EDGE) : interrupt edge type of P77

- 0 → P77's interruption source is a rising edge signal and falling edge signal.
- 1 → P77's interruption source is a falling edge signal.

CONT register is readable (CONTR) and writable (CONTW).

TCC and WDT :

There is an 8-bit counter available as prescaler for the TCC or WDT. The prescaler is available for the TCC only or WDT only at the same time.

An 8 bit counter is available for TCC or WDT determined by the status of the bit 3 (PAB) of the CONT register.

See the prescaler ratio in CONT register.

Fig.16 depicts the circuit diagram of TCC/WDT.

Both TCC and prescaler will be cleared by instructions which write to TCC each time.

The prescaler will be cleared by the WDTC and SLEP instructions, when assigned to WDT mode.

The prescaler will not be cleared by SLEP instructions, when assigned to TCC mode.

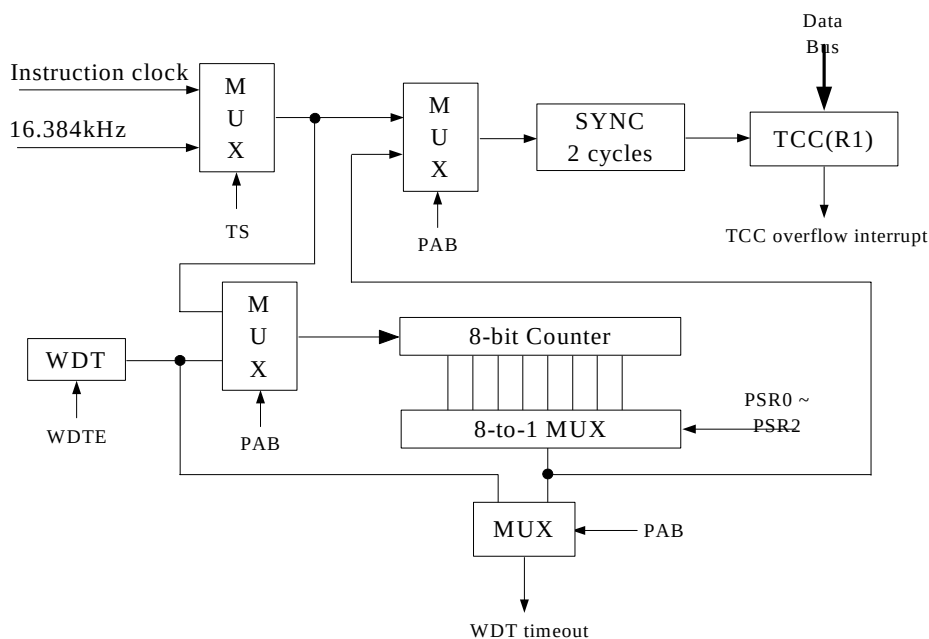


Fig.17 Block diagram of TCC WDT

IOC5 (PORT5 I/O control, PORT switch, Key tone, CDAS, LCD bias)
PAGE0 (PORT5 I/O control register, PORT switch)

7	6	5	4	3	2	1	0
IOC57	IOC56	IOC55	CASPWR	P9SH	P9SL	P8SH	P8SL

Bit 0 (P8SL) : Switch low nibble I/O PORT8 or LCD segment output for share pins SEGxx/P8x pins

- 0 → select normal P80 ~ P83 for low nibble PORT8
- 1 → select SEG64 ~ SEG67 output for LCD SEGMENT output.

Bit 1 (P8SH) : Switch high nibble I/O PORT8 or LCD segment output for share pins SEGxx/P8x pins

- 0 → select normal P84 ~ P87 for high nibble PORT8
- 1 → select SEG68 ~ SEG71 output for LCD SEGMENT output.

Bit 2 (P9SL) : Switch low nibble I/O PORT9 or LCD segment output for share pins SEGxx/P9x pins

- 0 → select normal P90 ~ P93 for low nibble PORT9

1 → select SEG72 ~ SEG75 output for LCD SEGMENT output.

Bit 3 (P9SH) : Switch high nibble I/O PORT9 or LCD segment output for share pins SEGxx/P9x pins

0 → select normal P94 ~ P97 for high nibble PORT9

1 → select SEG76 ~ SEG79 output for LCD SEGMENT output.*Bit 4:general register

Bit 4 (CWPWR) : Power control of Call Waiting circuit

1/0 → enable circuit /disable circuit

Bit 5~Bit 6(IOC55~IOC57) : PORT5 I/O direction control registers.

0 → put the relative I/O pin as output

1 → put the relative I/O pin into high impedance

PAGE1 (Key tone control, CDAS, LCD bias control)

7	6	5	4	3	2	1	0
KT1	KT0	KTS	CDAS	BIAS3	BIAS2	BIAS1	BIAS0

Bit 0~Bit 3(BIAS0~BIAS3) : LCD operation voltage selection

$$V1 = VDD * (5 - n/15)/5$$

(BIAS3 to BIAS0)	V1 voltage	Example (VDD=5V)
0000	$VDD * (5-0/15)/5$	5V
0001	$VDD * (5-1/15)/5$	4.93V
0010	$VDD * (5-2/15)/5$	4.86V
0011	$VDD * (5-3/15)/5$	4.80V
0100	$VDD * (5-4/15)/5$	4.73V
:	:	:
1101	$VDD * (5-13/15)/5$	4.13V
1110	$VDD * (5-14/15)/5$	4.07V
1111	$VDD * (5-15/15)/5$	4.0V

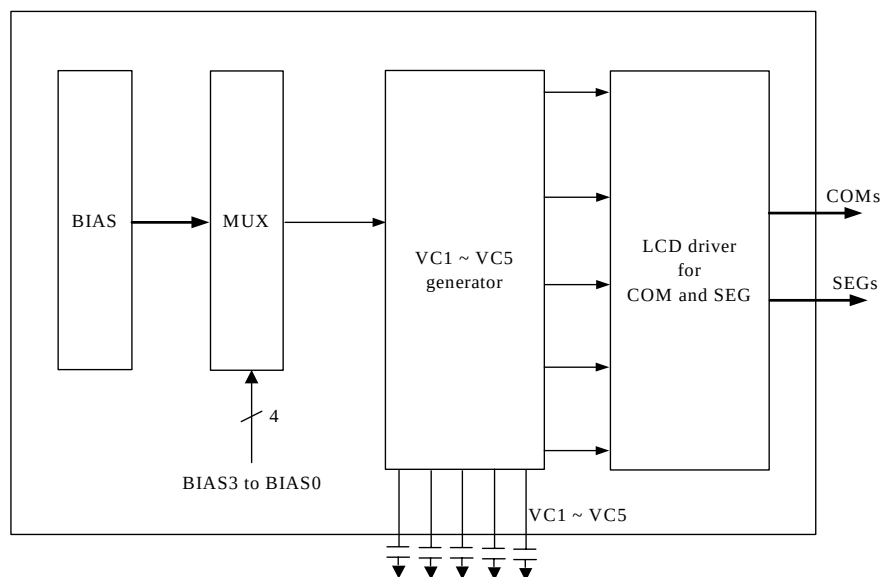
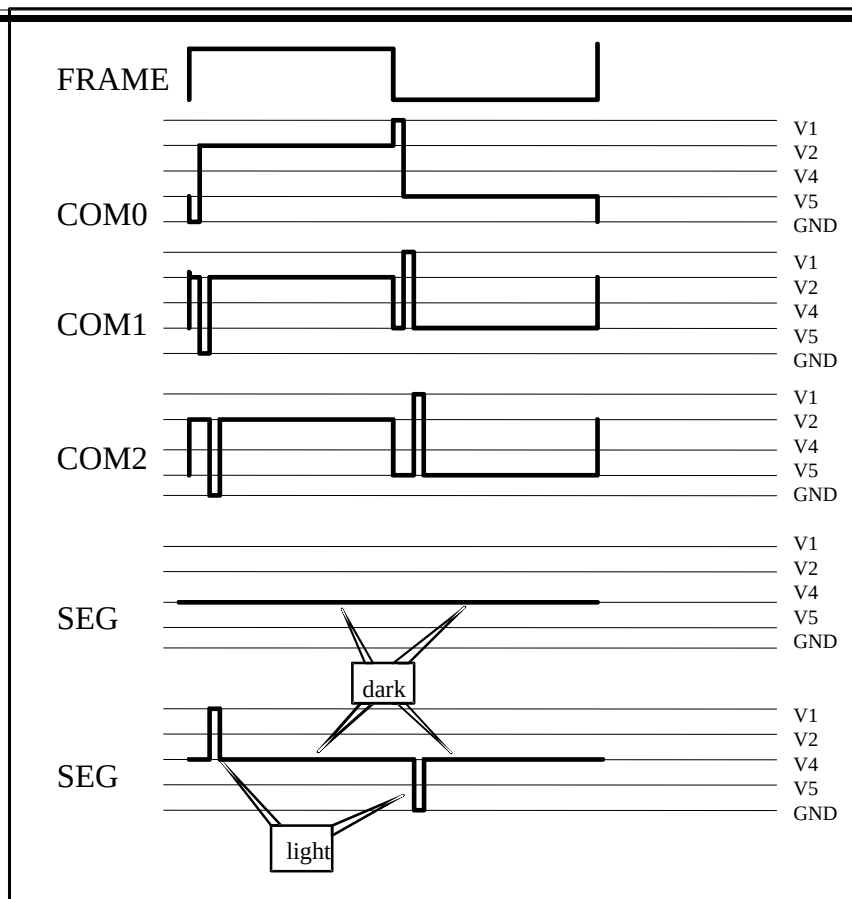


Fig.18 The relation between bias and V1 to V5

Fig.19a LCD waveform (1/4 bias) for 1/8 duty, 1/9 duty, 1/16 duty



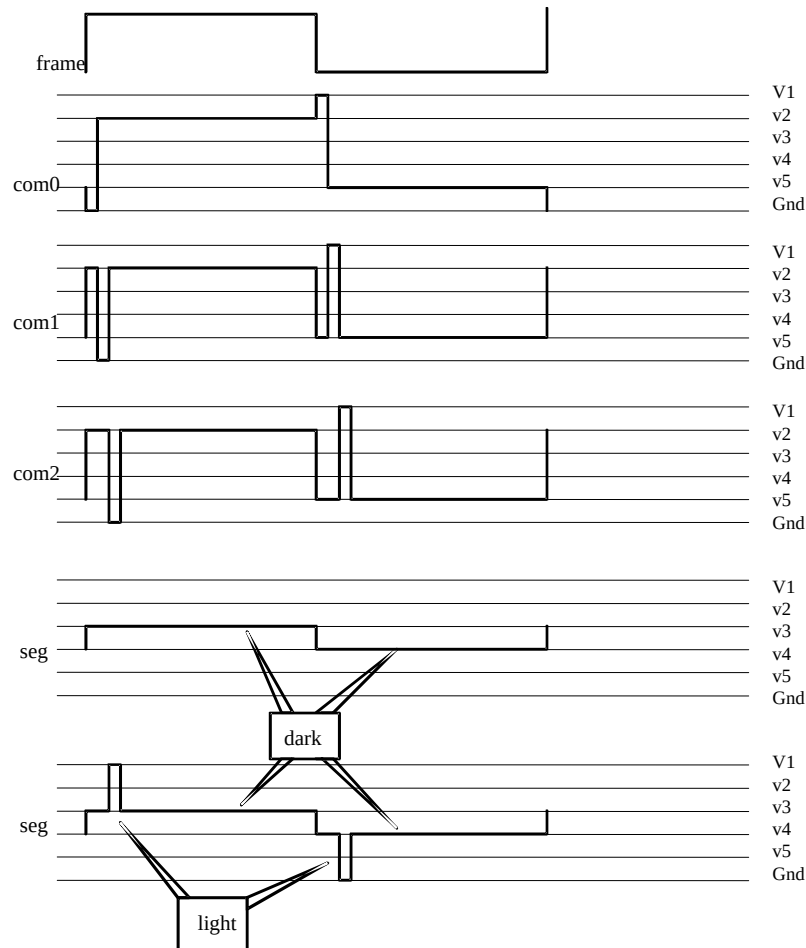


Fig.19b LCD waveform (1/5 bias) for 1/24 duty

Bit 4(CDAS) : Current DA switch

- 0 → normal PORT66
- 1 → Current DA output

Bit 5(KTS) : Key tone output switch

- 0 → normal PORT67
- 1 → key tone output .

Bit 6~Bit 7(KT0~KT1) : Key tone output frequency and its power control

KT1	KT0	Key tone frequency and power
0	0	$32.768\text{KHz}/32 = 1.024\text{kHz}$ clock and enable
0	1	$32.768\text{KHz}/16 = 2.048\text{kHz}$ clock and enable
1	0	$32.768\text{KHz}/8 = 4.096\text{kHz}$ clock and enable
1	1	Power off key tone

IOC6 (PORT6 I/O control, CDA, PORT switch, LCD driving control)
PAGE0 (PORT6 I/O control register)

7	6	5	4	3	2	1	0
IOC67	IOC66	IOC65	IOC64	IOC63	IOC62	IOC61	IOC60

Bit 0~Bit 7(IOC60~IOC67) : PORT6(0~7) I/O direction control register

0 → put the relative I/O pin as output

1 → put the relative I/O pin into high impedance

PAGE1 (Current DA control,)

7	6	5	4	3	2	1	0
DAEN	DA6	DA5	DA4	DA3	DA2	DA1	DA0

Bit 0~Bit 6(DA0~DA6) : Current DA output buffer

User can use this buffer to control the output current of current DA for the driving transistor of speaker.

Bit 7 (DAEN) : Current DA enable control

0/1 → disable/enable

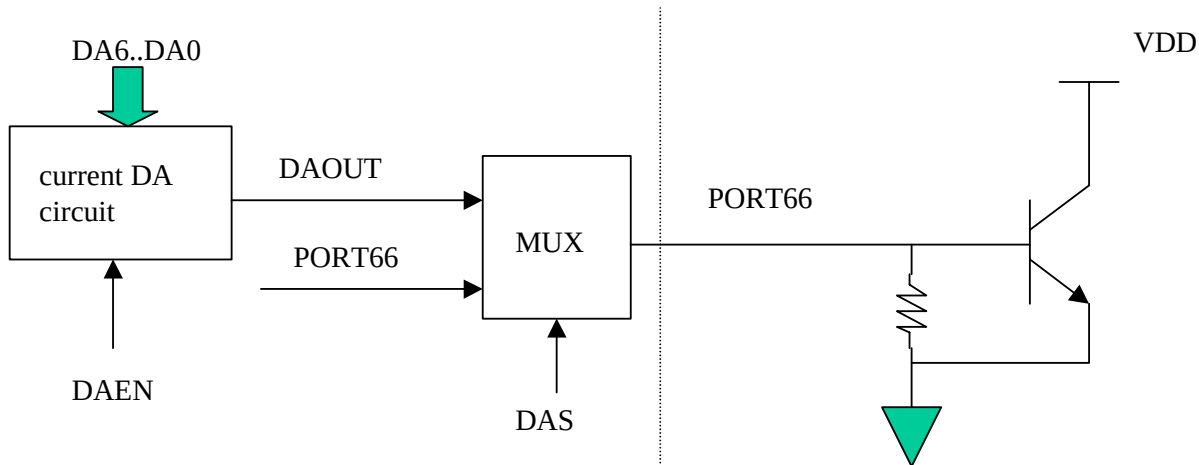


Fig.20 Current DA structure

PAGE 2 (PORT switch, LCD driving ability control)

7	6	5	4	3	2	1	0
PCSH	PCSL	PBS	LCDDV1	LCDDV0	CDAL2	CDAL1	CDAL0

Bit 0~Bit 2(DAL0~DAL1) : change output level of current DA

CDAL2	CDAL1	CDAL0	Output level
0	0	0	L0 (ratio = 1/8)
0	0	1	L1 (ratio = 2/8)
0	1	0	L2 (ratio = 3/8)
0	1	1	L3 (ratio = 4/8)
1	0	0	L4 (ratio = 5/8)
1	0	1	L5 (ratio = 6/8)
1	1	0	L6 (ratio = 7/8)
1	1	1	L7 (ratio = 1)

Bit 3~Bit 4(LCDDV0~LCDDV1) : LCD driver's driving ability control

LCDDV1	LCDDV0	Driving mode
0	0	Normal mode (ratio = 1)
0	1	Weak mode (ratio = 1/2)
1	0	Strong mode (ratio = 2)
1	1	Maximum mode (ratio = 4)

LCDDV0 ~ LCDDV1 are used to select the driving ability of LCD driver. The driving ability is Maximum mode > Strong mode > Normal mode > Weak mode by 1/2 ratio individually. The larger driving ability it is selected, the larger output loading of LCD driver output can be afforded and the more current consumption is occurred. It depends on user's application.

Bit 5(PBS) : Switch I/O PORTB or LCD segment output for share pins SEGxx/PBx

- 0 → select normal PB0 ~ PB7 for PORTB
- 1 → select SEG48 ~ SEG55 output for LCD SEGMENT output.

Bit 6(PCSL) : Switch low nibble I/O PORTC or LCD segment output for share pins SEGxx/PCx

- 0 → select normal PC0 ~ PC3 for low nibble PORTC
- 1 → select SEG56 ~ SEG59 output for LCD SEGMENT output.

Bit 7(PCSH) : Switch high nibble I/O PORTC or LCD segment output for share pins SEGxx/PCx

- 0 → select normal PC4 ~ PC7 for high nibble PORTC
- 1 → select SEG60 ~ SEG63 output for LCD SEGMENT output.

IOC7 (PORT7 I/O control, Key strobe(8~15))
PAGE0 (PORT7 I/O control register)

7	6	5	4	3	2	1	0
IOC77	IOC76	IOC75	IOC74	IOC73	IOC72	IOC71	IOC70

Bit 0~Bit 7(IOC70~IOC77) : PORT7(0~7) I/O direction control register

- 0 → put the relative I/O pin as output
- 1 → put the relative I/O pin into high impedance

PAGE1 (Key strobe control register)

7	6	5	4	3	2	1	0
STRB15	STRB14	STRB13	STRB12	STRB11	STRB10	STRB9	STRB8

Bit 0~Bit 7(STRB8~STRB15) : Key strobe control bits

These key strobe control registers correspond to SEGMENT8 to SEGMENT15. Please refer KEYSTOBE explanation (RE page0).

IOC8 (PORT8 I/O control, , Key strobe(16~23))
PAGE0 (PORT8 I/O control register)

7	6	5	4	3	2	1	0
IOC87	IOC86	IOC85	IOC84	IOC83	IOC82	IOC81	IOC80

Bit 0~Bit 7(IOC80~IOC87) : PORT8(0~7) I/O direction control register

- 0 → put the relative I/O pin as output
- 1 → put the relative I/O pin into high impedance

PAGE1 (Key strobe control register)

7	6	5	4	3	2	1	0
STRB23	STRB22	STRB21	STRB20	STRB19	STRB18	STRB17	STRB16

Bit 0~Bit 7(STRB16~STRB23) : Key strobe control bits

These key strobe control registers correspond to SEGMENT16 to SEGMENT23. Please refer KEYSTOBE explanation (RE page0).

IOC9 (PORT9 I/O control, DTMF receiver)

PAGE0 (PORT9 I/O control register)

7	6	5	4	3	2	1	0
IOC97	IOC96	IOC95	IOC94	IOC93	IOC92	IOC91	IOC90

Bit 0~Bit 7(IOC90~IOC97) : PORT9(0~7) I/O direction control register

0 → put the relative I/O pin as output

1 → put the relative I/O pin into high impedance

PAGE1 (DTMF receiver)

7	6	5	4	3	2	1	0
DREN	STD	TDP2	TDP1	Q4	Q3	Q2	Q1

Bit 0~Bit 3(Q1~Q4) : DTMF receiver decoding data

To provide the code corresponding to the last valid tone-pair received (see code table). STD signal which steering output presents a logic high when a received tone-pair has been registered and the Q4 ~ Q1 output latch updated and generate a interruption (IOCF has enabled); returns to logic low when the voltage on ST/GT falls below V_{tst}.

F low	F high	Key	DREN	Q4~Q1
697	1209	1	1	0001
697	1336	2	1	0010
697	1477	3	1	0011
770	1209	4	1	0100
770	1336	5	1	0101
770	1477	6	1	0110
852	1209	7	1	0111
852	1336	8	1	1000
852	1477	9	1	1001
941	1209	0	1	1010
941	1336	*	1	1011
941	1477	#	1	1100
697	1633	A	1	1101
770	1633	B	1	1110
852	1633	C	1	1111
941	1633	D	1	0000
Any	Any	Any	0	xxxx (x:unknown)

Bit 4~Bit 5(TDP1~TDP2) : Tone detection present time setup.

TDP2	TDP1	Tdp
0	0	20 ms
0	1	15 ms
1	0	10 ms
1	1	5 ms

Bit 6(STD) : Delayed steering output.

Presents a logic high when a received tone-pair has been registered and the output latch updated; returns to logic low when the voltage on St/GT falls below V_{tst}.

0/1 → Data invalid/data valid

Bit 7(DREN) : DTMF receiver power control

0/1 → power down/ power up

Be sure open main clock before using DTMF receiver circuit and shut down FSK power (R9 PAGE0 bit 3 set 0). A logic low applied to DREN will shut down power of the device to minimize the power consumption in a standby mode. It stops functions of the filters.

In many situations not requiring independent selection of receive and pause, the simple steering circuit of is applicable. Component values are chosen according to the following formulae:

$$t_{REC} = t_{DP} + t_{GTP} \quad t_{ID} = t_{DA} + t_{GTA}$$

The value of t_{DP} is a parameter of the device and t_{REC} is the minimum signal duration to be recognized by the receiver. A value for C of 0.1 μ F is recommended for most applications, leaving R to be selected by the designer. For example, a suitable value of R for a t_{REC} of 30mS would be 300k.

Different steering arrangements may be used to select independently the guard-times for tone-present (t_{GTP}) and tone-absent (t_{GTA}). This may be necessary to meet system specifications which place both accept and reject limits on both tone duration and inter digital pause.

Guard-time adjustment also allows the designer to tailor system parameters such as talk off and noise immunity. Increasing t_{REC} improves talk-off performance, since it reduces the probability that tones simulated by speech will maintain signal condition for long enough to be registered. On the other hand, a relatively short t_{REC} with a long t_{DO} would be appropriate for extremely noisy environments where fast acquisition time and immunity to drop-outs would be required.

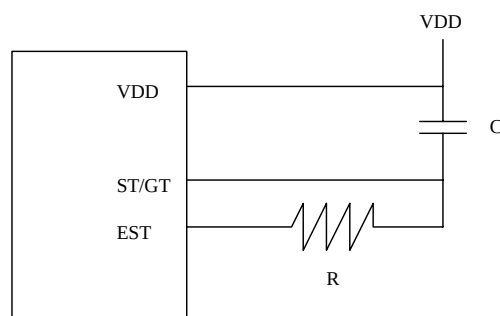


Fig.21. DTMF receiver delay time control

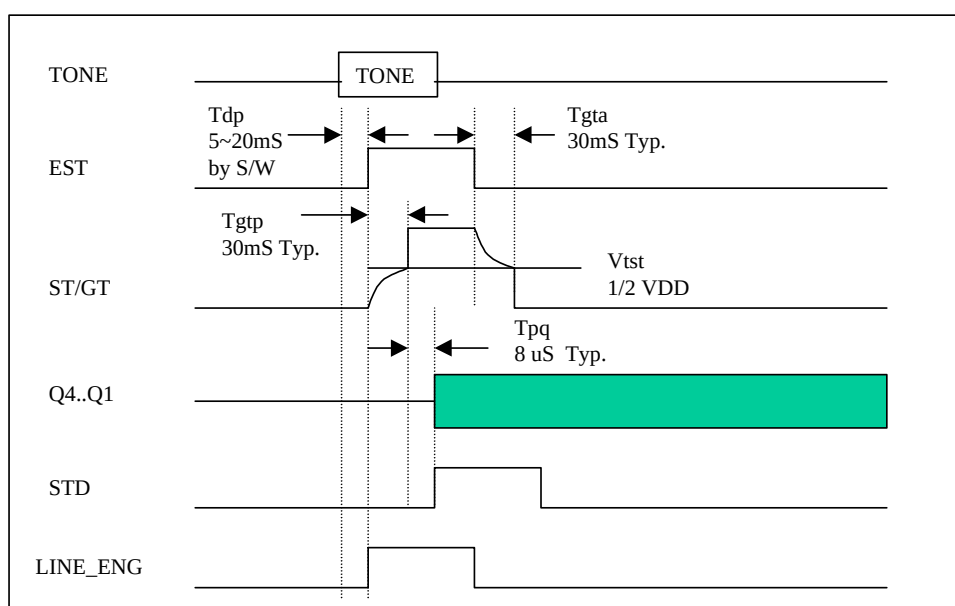


Fig.22. DTMF receiver timing.

IOCA (CN1's and CN2's clock and scaling, PORT7 pull high control)
PAGE0 (Counter1's and Counter2's clock and scale setting)

7	6	5	4	3	2	1	0
CNT2S	C2P2	C2P1	C2P0	CNT1S	C1P2	C1P1	C1P0

Bit 0~Bit 2(C1P0~C1P2) : Counter1 scaling

C1P2	C1P1	C1P0	COUNTER1
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 3(CNT1S) : Counter1 clock source

0/1 → 16.384kHz/instruction clock

Bit 4~Bit 6(C2P0~C2P2) : Counter2 scaling

C2P2	C2P1	C2P0	COUNTER2
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 7(CNT2S) : Counter2 clock source

0/1 → 16.384kHz/instruction clock

PAGE1 (PORT7 pull high control register)

7	6	5	4	3	2	1	0
PH77	PH76	PH75	PH74	PH73	PH72	PH71	PH70

Bit 0~Bit 7(PH70~PH77) : PORT7(0~7) pull high control register

0 → disable pull high function.

1 → enable pull high function

IOCB (PORTB I/O control, PORT6 pull high control)
PAGE0 (PORTB I/O control register)

7	6	5	4	3	2	1	0
IOCB7	IOCB6	IOCB5	IOCB4	IOCB3	IOCB2	IOCB1	IOCB0

Bit 0~Bit 7(IOCB0~IOCB7) : PORTB(0~7) I/O direction control register

0 → put the relative I/O pin as output

1 → put the relative I/O pin into high impedance

PAGE1 (PORT6 pull high control register)

7	6	5	4	3	2	1	0
PH67	PH66	PH65	PH64	PH63	PH62	PH61	PH60

Bit 0~Bit 7(PH60~PH67) : PORT6(0~7) pull high control register

0 → disable pull high function.

1 → enable pull high function



IOCC (PORTC I/O control, TONE1 control)

PAGE0 (PORT9 I/O control register)

7	6	5	4	3	2	1	0
IOCC7	IOCC6	IOCC5	IOCC4	IOCC3	IOCC2	IOCC1	IOCC0

Bit 0~Bit 7(IOCC0~IOCC7) : PORTC(0~7) I/O direction control register

0 → put the relative I/O pin as output

1 → put the relative I/O pin into high impedance

PAGE1 (TONE1 control register)

7	6	5	4	3	2	1	0
T17	T16	T15	T14	T13	T12	T11	T10

Bit 0~Bit 7(T10~T17) : Tone generator1's frequency divider and power control

Please Run in Normal mode .

Clock source = 111957Hz

T17~T10 = '11111111' → Tone generator1 will has 439(111957/N , N=255) Hz SIN wave output.

:

:

T17~T10 = '00000010' → Tone generator1 will has 55978(111957/N , N=2) Hz SIN wave output.

T17~T10 = '00000001' → DC bias voltage output

T17~T10 = '00000000' → Power off

Built-in tone generator can generate dialing tone signals for telephone of dialing tone type or just a single tone. In DTMF application, there are two kinds of tone. One is the group of row frequency (TONE1), the other is the group of column frequency (TONE2), each group has 4 kinds of frequency, user can get 16 kinds of DTMF frequency totally. Tone generator contains a row frequency sine wave generator for generating the DTMF signal which selected by IOCC page1 and a column frequency sine wave generator for generating the DTMF signal which selected by IOCD page1. This block can generate single tone by filling one of these two register.

If all the values are low, the power of tone generators will turn off .

		TONE2 (IOCD PAGE1) High group freq.			
		1203.8Hz (0X5D)	1332.8Hz (0X54)	1473.1Hz (0X4C)	1646.4Hz (0X44)
TONE1(IOCC page1) Low group freq.	699.7Hz(0x0A0)	1	2	3	A
	772.1Hz(0x091)	4	5	6	B
	854.6Hz(0x083)	7	8	9	C
	940.8Hz(0x077)	*	0	#	D

Also TONE1 and TONE2 are an asynchronous tone generator so the both can be used to generate Caller ID FSK signal. In FSK generator application, TONE1 or TONE2 can generate 1200Hz Mark bit and 2200Hz Space bit for Bell202 or 1300Hz Mark bit and 2100Hz Space bit for V.23. See the following table.

TONE1(IOCC PAGE1) or TONE2(IOCD PAGE1)	Freq. (Hz)	meaning
0x5D	1203.8	Bell202 FSK Mark bit
0x33	2195.2	Bell202 FSK Space bit
0x56	1301.8	V.23 FSK Mark bit
0x35	2112.4	V.23 FSK Space bit

IOCD (Counter1 data, TONE2 control)

PAGE0 (Counter1 data buffer)

7	6	5	4	3	2	1	0
CN17	CN16	CN15	CN14	CN13	CN12	CN11	CN10

Bit 0~Bit 7(CN10~CN17) : Counter1's data buffer

User can read and write this buffer. Counter1 is a eight bit up-counter with 8-bit prescaler that user can use IOCD to preset and read the counter. (write = preset) After a interruption, it will reload the preset value.

Example: write: IOW 0x0D ; write the data at accumulator to counter1 (preset)

Example: read: IOR 0x0D ;read IOCD data and write to accumulator

PAGE1 (TONE2 control register)

7	6	5	4	3	2	1	0
T27	T26	T25	T24	T23	T22	T21	T20

Bit 0~Bit 7(T20~T27) : Tone generator1's frequency divider and power control. Please refer to IOCC page1 Tone1 control register for detail.

IOCE (Counter2 data, Comparator and OP control , Energy Detector)

PAGE0 (Counter2 data buffer)

7	6	5	4	3	2	1	0
CN27	CN26	CN25	CN24	CN23	CN22	CN21	CN20

Bit 0~Bit 7(CN20~CN27) : Counter2's data buffer

User can read and write this buffer. Counter2 is a eight bit up-counter with 8-bit prescaler that user can use IOCD to preset and read the counter. (write = preset) After a interruption, it will reload the preset value.

Example: write: IOW 0x0E ; write the data at accumulator to counter2 (preset)

Example: read: IOR 0x0E ;read IOCE data and write to accumulator

PAGE1 (Comparator reference voltage type, PORT switch)

7	6	5	4	3	2	1	0
CMPREF	CMPIN3	CMPIN2	CMPIN1	P5S2	P5S1		

Bit 0 : unused

Bit 1 : unused

Bit 2~Bit 3 (P5S1~P5S2) : PORT5 switch

P5S2	P5S1	PORT55	PORT56	Status
0 or 1	0	PORT55	PORT56	Normal PORT5 IO
0 or 1	1	STGT	EST	DTMF receiver IO

External reference signal

The analog signal that is presented at Cin- compares to the signal at Cin+, and the digital output of the comparator is adjusted accordingly.

*The reference signal must be between Vss and Vdd.

*Threshold detector applications may be the same reference.

*The comparator can operate from the same or different reference source

Bit 4 (CMPIN1) : Switch for controlling PORT63 as IO PORT or a comparator input.

0 → IO PORT63

1 → comparator input

Bit5 (CMPIN2) : Switch for controlling PORT64 as IO PORT or a comparator input.

0 → IO PORT64

1 → comparator input

Bit 6 (CMPIN3) : Switch for controlling PORT65 as IO PORT or a comparator input.

0 → IO PORT65

1 → comparator input

Bit 7 (CMPREF) : Switch for comparator reference voltage type

0 → internal reference voltage

1 → external reference voltage



PAGE2

7	6	5	4	3	2	1	0
VRSEL				CW_SMB			

Bit 0: unused

Bit 1 : unused

Bit 2 : unused

Bit 3(CW_SMB) : Call Waiting / short message receiver switch

0 → Short message mode select. $\pm 5.5\%$ CAS tone accepted frequency range deviation.(Protocol : $\pm 5\%$)

1 → Call Waiting mode select. CAS tone accepted frequency range deviation is decided on CODE Option Register bit 5 (0:for Europe and USA / 1:for China)

Bit 4 : unused

Bit 5 : unused

Bit 6 : unused

Bit 7 (VRSEL) : Reference voltage VR selection bit for Comparator

0/1 → VR = VDD/VR = 2.0V, When this bit is set to “0”, V2_0 ref. circuit will be powered off.

2.0V ref. circuit is only powered on when this bit and RD page0 bit 7(CMPEN) are all set to “1”.

IOCF (Interrupt Mask Register)

7	6	5	4	3	2	1	0
RBF/STD	FSK/CW	INT2	INT1	INT0	CNT2	CNT1	TCIF

Bit 0 ~ Bit 7 : Interrupt enable bits.

0/1 → disable interrupt/enable interrupt

VII.3 I/O Port

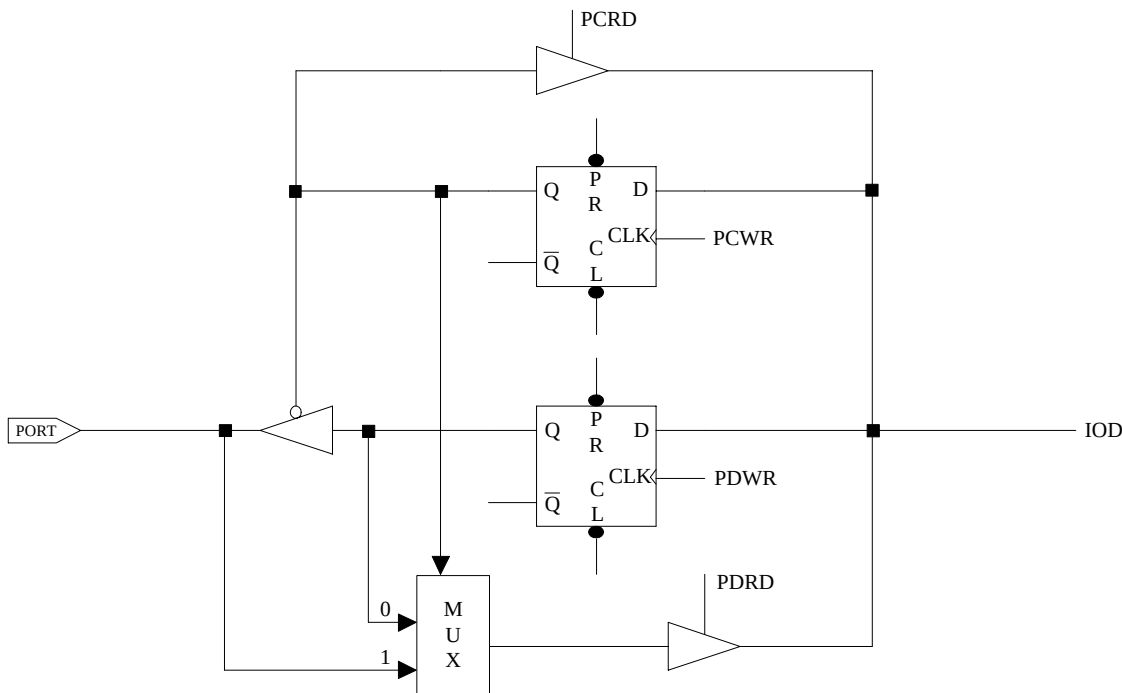


Fig.25 The circuit of I/O port and I/O control register

The I/O registers are bi-directional tri-state I/O ports. The I/O ports can be defined as "input" or "output" pins by the I/O control registers under program control. The I/O registers and I/O control registers are both readable and writable. The I/O interface circuit is shown in Fig.25

VII.4 RESET

The RESET can be caused by

- (1) Power on voltage detector reset (POVD) and power on reset
- (2) WDT timeout. (if enabled and in GREEN or NORMAL mode)
- (3) /RESET pin pull low

<Note> At case (1), POVD is controlled by CODE OPTION. If you enable POVD, CPU will reset at 2V under. And CPU will consume more current about 3uA . And the power on reset is a circuit always enable. It will reset CPU at about 1.4V and consume about 0.5uA.

Once the RESET occurs, the following functions are performed.

- The oscillator is running, or will be started.
- The Program Counter (R2) is set to all "0".
- When power on, the upper 3 bits of R3 and the upper 2 bits of R4 are cleared.
- The Watchdog timer and prescaler counter are cleared.
- The Watchdog timer is disabled.
- The CONT register is set to all "1"
- The other register (bit7..bit0)



address	R register page0	R register page1	IOC register page0	IOC register page1	IOC register page2
4	00xxxxxx	00000000			xxxxxxx
5	xxx00000	xxxxxxx	11100000	00000000	00000000
6	xxxxxxx	xxxxxxx	11111111	00000000	00000000
7	xxxxxxx	xxxxxxx	11111111	11111111	xxxxxxx
8	xxxxxxx	xxxxxxx	11111111	11111111	xxxxxxx
9	xxxxxxx	xxxxxxx	11111111	00000000	xxxxxxx
A	0000xx0	xxxxxxx	00000000	00000000	xxxxxxx
B	xxxxxxx	xxxxxxx	11111111	00000000	xxxxxxx
C	xxxxxxx	xxxxxxx	11111111	00000000	xxxxxxx
D	00000000	xxxxxxx	00000000	00000000	xxxxxxx
E	00000000	00xxxxxx	00000000	00000000	00000000
F	00000000	-	00000000	-	

VII.5 wake-up

The controller has two types of sleep mode for power saving.

- (1) **SLEEP** mode , RA(7)=0 + "SLEP" instruction .

The controller will turn off all the CPU and crystal. Other circuit with power control like key tone control or PLL control (which has enable register), user has to turn it off by software.

Wake-up from SLEEP mode

- (1) DT time out
- (2) external interrupt
- (3) /RESET pull low

All these cases will reset controller , and run the program at address zero. The status just like the power on reset. Be sure to enable circuit at case (1) or (2).

VII.6 Interrupt

RF is the interrupt status register which records the interrupt request in flag bits. IOCF is the interrupt mask register. TCC timer, Counter1 and Counter2 are internal interrupt source. P70 ~ P77(INT0 ~ INT1) are external interrupt input which interrupt sources are come from the external. If the interrupts are happened by these interrupt sources, then RF register will generate '1' flag to corresponding register if you enable IOCF register. Global interrupt is enabled by ENI instruction and is disabled by DISI instruction. When one of the interrupts (when enabled) generated, will cause the next instruction to be fetched from address 008H. Once in the interrupt service routine the source of the interrupt can be determined by polling the flag bits in the RF register. The interrupt flag bit must be cleared in software before leaving the interrupt service routine and enabling interrupts to avoid recursive interrupts.

VII.7 Instruction Set

Instruction set has the following features:

- (1) Every bit of any register can be set, cleared, or tested directly.
 - (2) The I/O register can be regarded as general register. That is, the same instruction can operates on I/O register.
- The symbol "R" represents a register designator which specifies which one of the 64 registers (including operational registers and general purpose registers) is to be utilized by the instruction. Bits 6 and 7 in R4 determine the selected register bank. "b" represents a bit field designator which selects the number of the bit, located in the register "R", affected by the operation. "k" represents an 8 or 10-bit constant or literal value.

INSTRUCTION BINARY	HEX	MNEMONIC	OPERATION	STATUS AFFECTED	Instruction cycle
0 0000 0000 0000	0000	NOP	No Operation	None	1



0 0000 0000 0001	0001	DAA	Decimal Adjust A	C	1
0 0000 0000 0010	0002	CONTW	A → CONT	None	1
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T,P	1
0 0000 0000 0100	0004	WDTC	0 → WDT	T,P	1
0 0000 0000 rrrr	000r	IOW R	A → IOCR	None	1
0 0000 0001 0000	0010	ENI	Enable Interrupt	None	1
0 0000 0001 0001	0011	DISI	Disable Interrupt	None	1
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None	2
0 0000 0001 0011	0013	RETI	[Top of Stack] → PC Enable Interrupt	None	2
0 0000 0001 0100	0014	CONTR	CONT → A	None	1
0 0000 0001 rrrr	001r	IOR R	IOCR → A	None	1
0 0000 0010 0000	0020	TBL	R2+A → R2 bits 9,10 do not clear	Z,C,DC	2
0 0000 01rr rrrr	00rr	MOV R,A	A → R	None	1
0 0000 1000 0000	0080	CLRA	0 → A	Z	1
0 0000 11rr rrrr	00rr	CLR R	0 → R	Z	1
0 0001 00rr rrrr	01rr	SUB A,R	R-A → A	Z,C,DC	1
0 0001 01rr rrrr	01rr	SUB R,A	R-A → R	Z,C,DC	1
0 0001 10rr rrrr	01rr	DECA R	R-1 → A	Z	1
0 0001 11rr rrrr	01rr	DEC R	R-1 → R	Z	1
0 0010 00rr rrrr	02rr	OR A,R	A ∨ R → A	Z	1
0 0010 01rr rrrr	02rr	OR R,A	A ∨ R → R	Z	1
0 0010 10rr rrrr	02rr	AND A,R	A & R → A	Z	1
0 0010 11rr rrrr	02rr	AND R,A	A & R → R	Z	1
0 0011 00rr rrrr	03rr	XOR A,R	A ⊕ R → A	Z	1
0 0011 01rr rrrr	03rr	XOR R,A	A ⊕ R → R	Z	1
0 0011 10rr rrrr	03rr	ADD A,R	A + R → A	Z,C,DC	1
0 0011 11rr rrrr	03rr	ADD R,A	A + R → R	Z,C,DC	1
0 0100 00rr rrrr	04rr	MOV A,R	R → A	Z	1
0 0100 01rr rrrr	04rr	MOV R,R	R → R	Z	1
0 0100 10rr rrrr	04rr	COMA R	/R → A	Z	1
0 0100 11rr rrrr	04rr	COM R	/R → R	Z	1
0 0101 00rr rrrr	05rr	INCA R	R+1 → A	Z	1
0 0101 01rr rrrr	05rr	INC R	R+1 → R	Z	1
0 0101 10rr rrrr	05rr	DJZA R	R-1 → A, skip if zero	None	2 if skip
0 0101 11rr rrrr	05rr	DJZ R	R-1 → R, skip if zero	None	2 if skip
0 0110 00rr rrrr	06rr	RRCA R	R(n) → A(n-1) R(0) → C, C → A(7)	C	1
0 0110 01rr rrrr	06rr	RRC R	R(n) → R(n-1) R(0) → C, C → R(7)	C	1
0 0110 10rr rrrr	06rr	RLCA R	R(n) → A(n+1) R(7) → C, C → A(0)	C	1
0 0110 11rr rrrr	06rr	RLC R	R(n) → R(n+1) R(7) → C, C → R(0)	C	1
0 0111 00rr rrrr	07rr	SWAPA R	R(0-3) → A(4-7) R(4-7) → A(0-3)	None	1
0 0111 01rr rrrr	07rr	SWAP R	R(0-3) ↔ R(4-7)	None	1
0 0111 10rr rrrr	07rr	JZA R	R+1 → A, skip if zero	None	2 if skip
0 0111 11rr rrrr	07rr	JZ R	R+1 → R, skip if zero	None	2 if skip
0 100b brrr rrrr	0xxx	BC R,b	0 → R(b)	None	1
0 101b brrr rrrr	0xxx	BS R,b	1 → R(b)	None	1



0	110b	brrr	rrrr	0xxx	JBC R,b	if R(b)=0, skip	None	2 if skip
0	111b	brrr	rrrr	0xxx	JBS R,b	if R(b)=1, skip	None	2 if skip
1	00kk	kkkk	kkkk	1kkk	CALL k	PC+1 → [SP] (Page, k) → PC	None	2
1	01kk	kkkk	kkkk	1kkk	JMP k	(Page, k) → PC	None	2
1	1000	kkkk	kkkk	18kk	MOV A,k	k → A	None	1
1	1001	kkkk	kkkk	19kk	OR A,k	A ∨ k → A	Z	1
1	1010	kkkk	kkkk	1Akk	AND A,k	A & k → A	Z	1
1	1011	kkkk	kkkk	1Bkk	XOR A,k	A ⊕ k → A	Z	1
1	1100	kkkk	kkkk	1Ckk	RETL k	k → A, [Top of Stack] → PC	None	2
1	1101	kkkk	kkkk	1Dkk	SUB A,k	k-A → A	Z,C,DC	1
1	1110	0000	0001	1E01	INT	PC+1 → [SP] 001H → PC	None	1
1	1110	100k	kkkk	1E8k	PAGE k	K→R5(4:0)	None	1
1	1111	kkkk	kkkk	1Fkk	ADD A,k	k+A → A	Z,C,DC	1

VII.8 CODE Option Register

The controller has one CODE option register which is not part of the normal program memory. The option bits cannot be accessed during normal program execution.

CODE Option Register1 (Program ROM)

7	6	5	4	3	2	1	0
-			/POVD	CWMODE	PACKSEL1	PACKSEL0	

Bit 1~2(PACKSEL0~PACKSEL1) : package select.

PACKSEL1	PACKSEL0	PACKAGE	PS
X	1	132 pin die	
1	0	128 pin QFPA	PC0~PC3 floating

Bit 3(CWMODE) : CAS tone (2130 Hz plus 2750 Hz) accepted frequency range select.

0 → ± 2% Call waiting accepted frequency range deviation.(Application for China protocol : ± 1.5%)

1 → ± 1.2% Call waiting accepted frequency range deviation.(Application for Europe and USA protocol : ± 0.5%)

Bit 4 (/POVD) : Power on voltage detector, 0/1 → enable/disable

/POVD	2.2V /POVD reset voltage	2.2V Power on reset voltage	Sleep mode current (VDD=5V)
1	No	Yes (2.2V)	1uA
0	Yes (2.2V)	No	15uA



VII.9 CALL WAITING Function Description

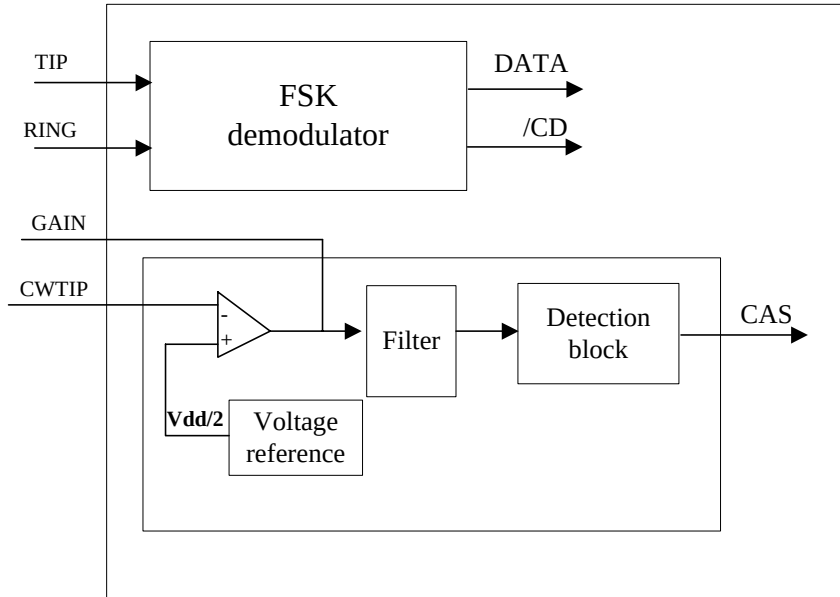


Fig.26 Call Waiting Block Diagram

Call Waiting service works by alerting a customer engaged in a telephone call to a new incoming call. This way the customer can still receive important calls while engaged in a current call. The CALL WAITING DECODER can detect CAS(Call-Waiting Alerting Signal 2130Hz plus 2750Hz) and generate a valid signal on the data pins.

The call waiting decoder is designed to support the Caller Number Deliver feature, which is offered by regional Bell Operating Companies.

In a typical application, after enabling CW circuit (by IOC5 page0 bit4 CWPWR) this IC receives Tip and Ring signals from twisted pairs. The signals as inputs of pre-amplifier, and the amplifier sends input signal to a band pass filter. Once the signal is filtered, the Detection block decodes the information and sends it to R3 register bit7 . The output data made available at R3 CAS bit.

The data is CAS signals. The CAS is normal high. When this IC detects 2130Hz and 2750Hz frequency, then CAS pin goes to low.

VIII. Absolute Operation Maximum Ratings

RATING	SYMBOL	VALUE	UNIT
DC SUPPLY VOLTAGE	VDD	-0.3 To 6	V
INPUT VOLTAGE	V _{in}	-0.5 to VDD +0.5	V
OPERATING TEMPERATURE RANGE	T _a	0 to 70	°C

IX. DC Electrical Characteristic

(Operation current consumption for Analog circuit)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Operation current for FSK	I_FSK	VDD=5V, CID power on		2.0		mA
		VDD=3V, CID power on		1.8		
Operation current for CW	I_CW	VDD=5V, CID power on		1.8		mA
		VDD=5V, CID power on		1.5		
Operation current for DTMF receiver	I_DR	VDD=3V, DTMFr power on		1.8		mA
		VDD=3V, DTMFr power on		1.5		
Operation current for TONE generator	I_DTMF	VDD=5V, DTMF power on		0.35		mA
		VDD=3V, DTMF power on		0.15		
Operation current for Current DA	I_DA	VDD=5V, CDA power on				mA
		VDD=3V, CDA power on				
Operation current for OP	I_OP	VDD=5V, PT power on		0.17		mA
		VDD=3V, PT power on		0.1		
Operation current for Comparator	I_CMP	VDD=5V, PT power on		0.17		mA
		VDD=3V, PT power on		0.1		

(Current DA output current)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Current DA output current	I_DAO	VDD=5V, CDA power on				mA
		VDD=3V, CDA power on				

(Ta=0°C ~ 70°C, VDD=5V±5%, VSS=0V)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Leakage Current for input pins	IIL1	VIN = VDD, VSS			±1	μA
Input Leakage Current for bi-directional pins	IIL2	VIN = VDD, VSS			±1	μA
Input High Voltage	VIH		2.0			V
Input Low Voltage	VIL				0.8	V
Input High Threshold Voltage	VIHT	/RESET, TCC, RDET1	2.0			V
Input Low Threshold Voltage	VILT	/RESET, TCC, RDET1			0.8	V
Clock Input High Voltage	VIHX	OSCI	1.8			V
Clock Input Low Voltage	VILX	OSCI			1.2	V
Output High Voltage (port5,8,9,B,C)	VOH1	IOH = -5mA	2.0			V
(port6,7)		IOH = -8mA	2.0			V
Output Low Voltage (port5,8,9,B,C)	VOL1	IOL = 5mA			0.4	V
(port6,7)		IOL = 8mA			0.4	V
Pull-high current	IPH	Pull-high active input pin at VSS		-10	-15	μA
Power down current (SLEEP mode)	ISB1	All input and I/O pin at VDD, output pin floating, WDT disabled		1	4	μA
Low clock current (GREEN mode)	ISB2	CLK=32.768KHz, All analog circuit disable, All input and I/O pin at VDD, output pin floating, WDT disabled, LCD		50	80	μA



Operating supply current (NORMAL mode)	ICC	enable /RESET=High, PLL enable CLK=3.579MHz, output pin floating and LCD enable, all analog circuit disable		1.0	1.3	mA
Tone generator reference voltage	Vref2		0.5		0.7	VDD

X. AC Electrical Characteristic

CPU instruction timing (Ta=0°C ~ 70°C, VDD=5V, VSS=0V)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input CLK duty cycle	Dclk		45	50	55	%
Instruction cycle time	Tins	32.768kHz		60		us
		3.579MHz		550		ns
Device delay hold time	Tdrh			16		ms
TCC input period	Ttcc	Note 1	(Tins+20)/N			ns
Watchdog timer period	Twdt	Ta = 25°C		16		ms

Note 1: N= selected prescaler ratio.

FSK AC Characteristic (Vdd=5V, Ta=+25°C)

CHARACTERISTIC	Min	Typ	Max	Unit
FSK sensitivity				
Low Level Sensitivity Tip & Ring @SNR 20dB	-40	-48		dBm
High Level Sensitivity Tip & Ring @SNR 20dB		0		dBm
Signal Reject		-51		dBm
FSK twist				
Positive Twist (High Level)	+10			dB
Positive Twist (Low Level)	+10			dB
Negative Twist (High Level)	-6			dB
Negative Twist (Low Level)	-6			dB

CW AC Characteristic (Vdd=5V, Ta=+25°C)

CHARACTERISTIC	Min	Typ	Max	Unit
CW sensitivity				
Sensitivity @SNR 20dB		-38		dBm
Low Tone Frequency 2130Hz		±1.2		%
High Tone Frequency 2750Hz		±1.2		%
CW twist				
Twist	±7			dB

DTMFr (DTMF receiver) AC Characteristic (Vdd=5V, Ta=+25°C)

CHARACTERISTIC	Min	Typ	Max	Unit
DTMFr				
Low Level Signal Sensitivity		-36		dBm
High Level Signal Sensitivity		0		dBm
Low Tone Frequency		±2		%
High Tone Frequency		±2		%
DTMFr noise endurance				
Signal to noise ratio	15			dB

TONE generators for AC Characteristic (Vdd=5V,Ta=+25°C)

CHARACTERISTIC	Min	Typ	Max	Unit
Tone1/Tone2 signal strength (root mean square voltage)				
Tone1 signal strength V1rms (ps1)	130	155	180	mV
Tone2 signal strength V2rms (ps1)	1.259V1rms			mV
Tone twist				
(Tone1 – Tone2) twist		-2		dB
Tone frequency deviation				
Frequency deviation			±1	%

(ps1) : V1rms and V2rms has 2 dB difference. It means $20\log(V2rms/V1rms) = 20\log 1.259 = 2$ (dB)

Timing characteristic (Vdd=5V,Ta=+25°C)

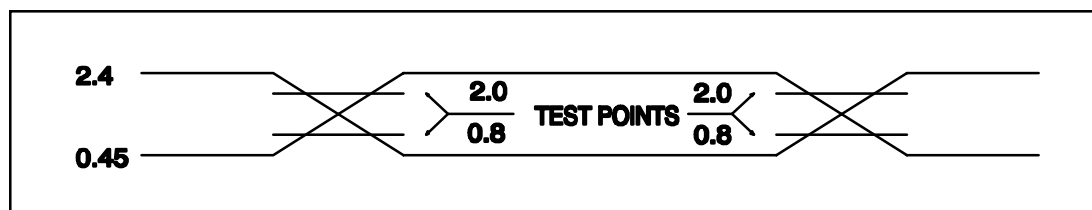
Description	Symbol	Min	Typ	Max	Unit
Oscillator timing characteristic					
OSC start up	32.768kHz	Tosc		400	ms
	3.579MHz PLL			10	
FSK timing characteristic					
Carrier detect low	Tcdl	--	10	14	ms
Data out to Carrier det low	Tdoc	--	10	20	ns
Power up to FSK(setup time)	Tsup	--	15	20	ms
End of FSK to Carrier Detect high	Tcdh		--	4	ms
CW timing characteristic					
CAS input signal length (2130 ,2750 Hz @ -20dBm)	Tcasi		80		ms
Call waiting data detect delay time	Tcwd		42		ms
Call waiting data release time	Tcwr		26		ms
DTMF receiver timing characteristic					
Tone Present Detection Time	Tdp		(ps1)		
the guard-times for tone-present (C=0.1uF, R=300K)	Tgtp		30		ms
the guard-times for tone-absent (C=0.1uF, R=300K)	Tgta		30		mS
Propagation Delay (St to Q)	Tpq		8		us
Tone Absent Detection Time	Tda		(ps2)		ms
SPI timing characteristic (CPU clock 3.58MHz and Fsc0 = 3.58Mhz /2)					
/SS set-up time	Tcss	560			ns
/SS hold time	Tcsh	250			
SCLK high time	Thi	250			ns
SCLK low time	Tlo	250			ns
SCLK rising time	Tr		15	30	ns
SCLK falling time	Tf		15	30	ns
SDI set-up time to the reading edge of SCLK	Tisu	25			ns
SDI hold time to the reading edge of SCLK	Tihd	25			ns
SDO disable time	Tdis			560	ns

(ps1) : Controlled by software

(ps2) : Controlled by RC circuit.

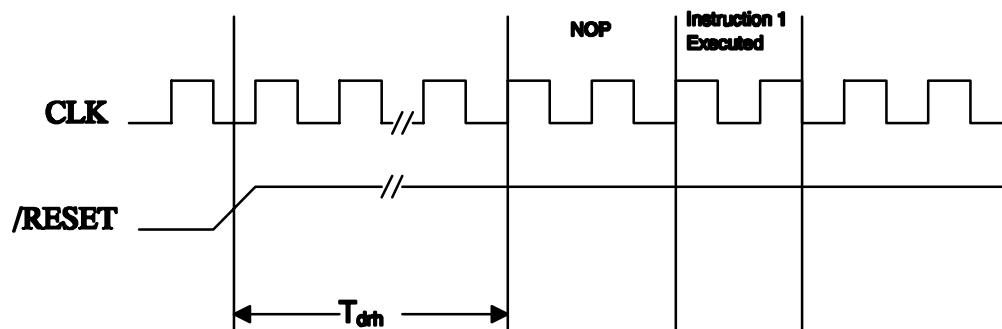
XI. Timing Diagrams

AC Test Input/Output Waveform



AC Testing: Input are driven at 2.4V for logic "1", and 0.45V for logic "0". Timing measurements are made at 2.0V for logic "1", and 0.8V for logic "0".

RESET Timing



TCC Input Timing

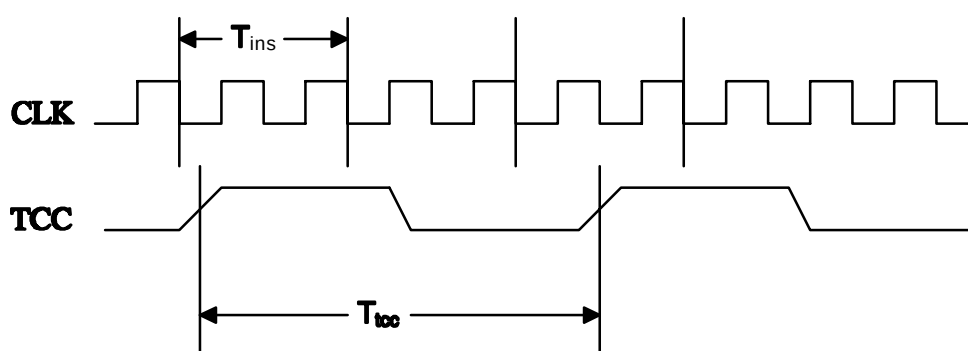


Fig.28 AC timing

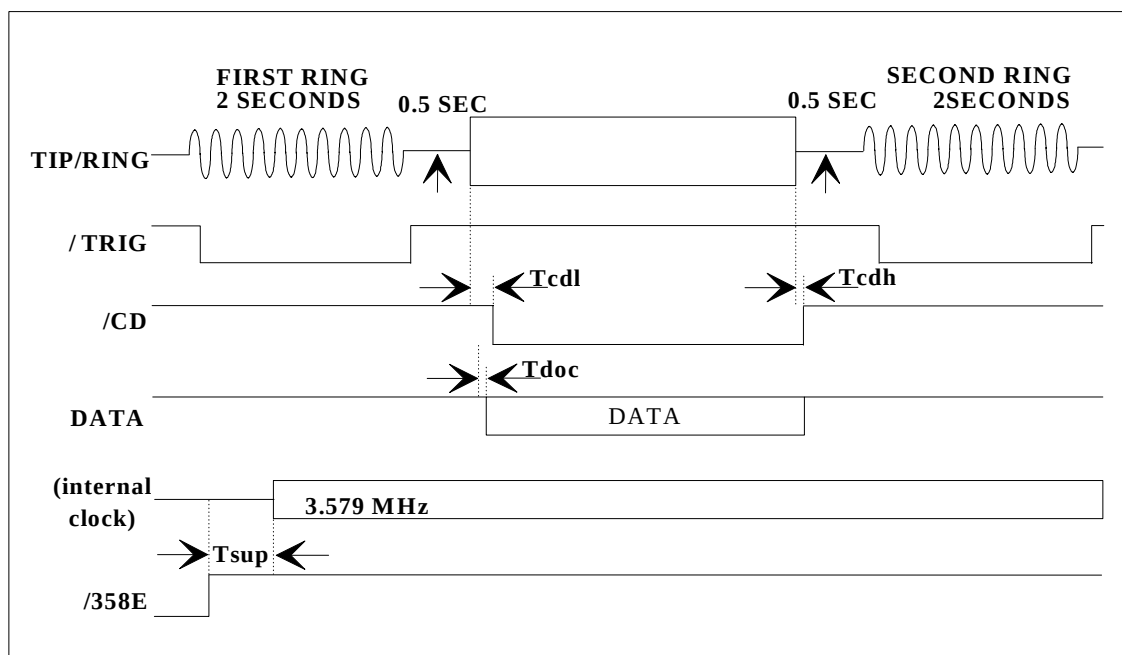


Fig.29 FSK timing diagram

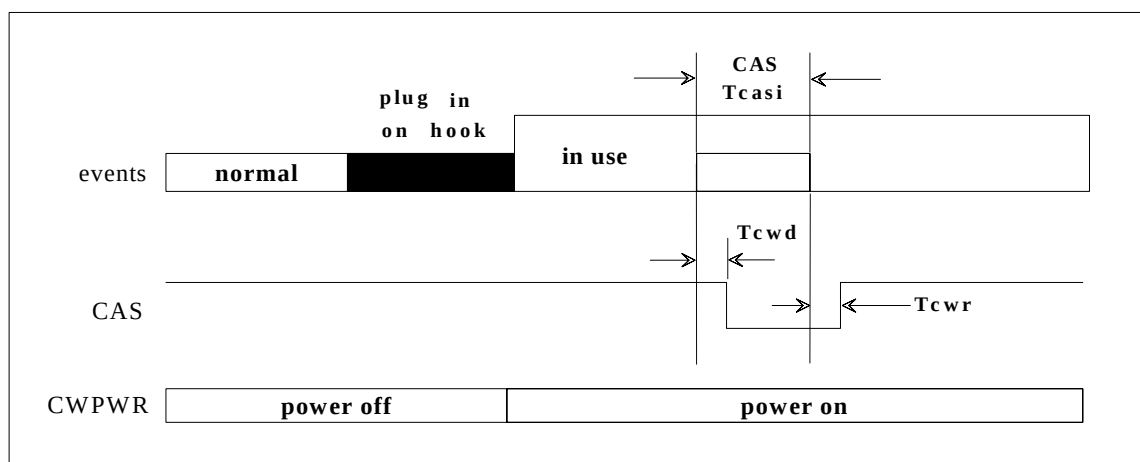


Fig.30 Call waiting timing diagram

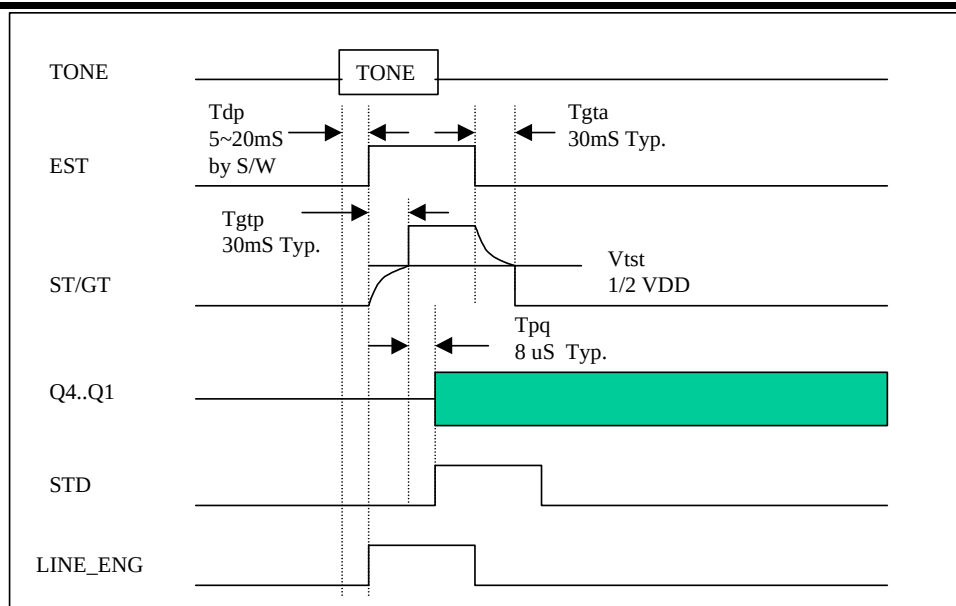
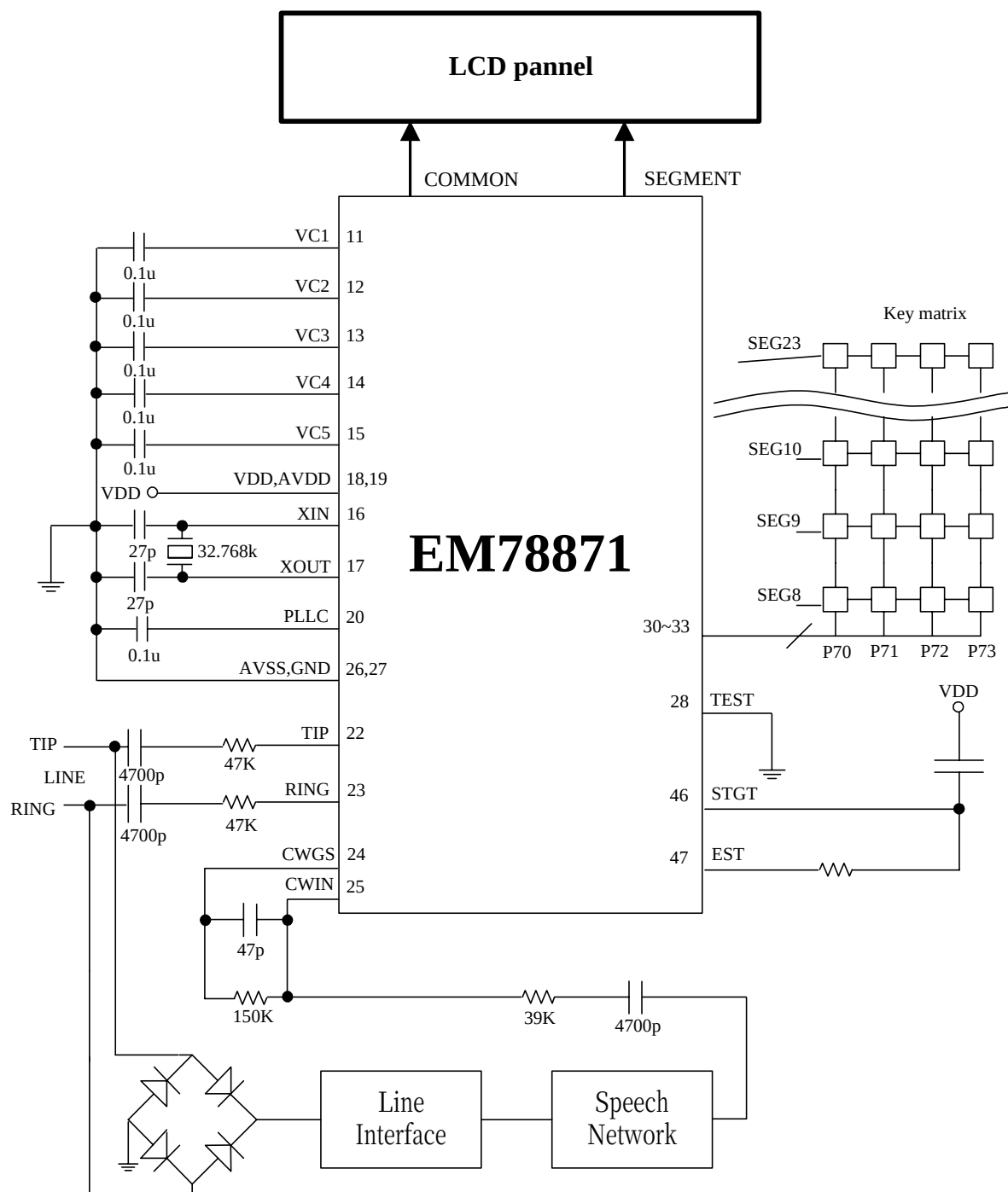
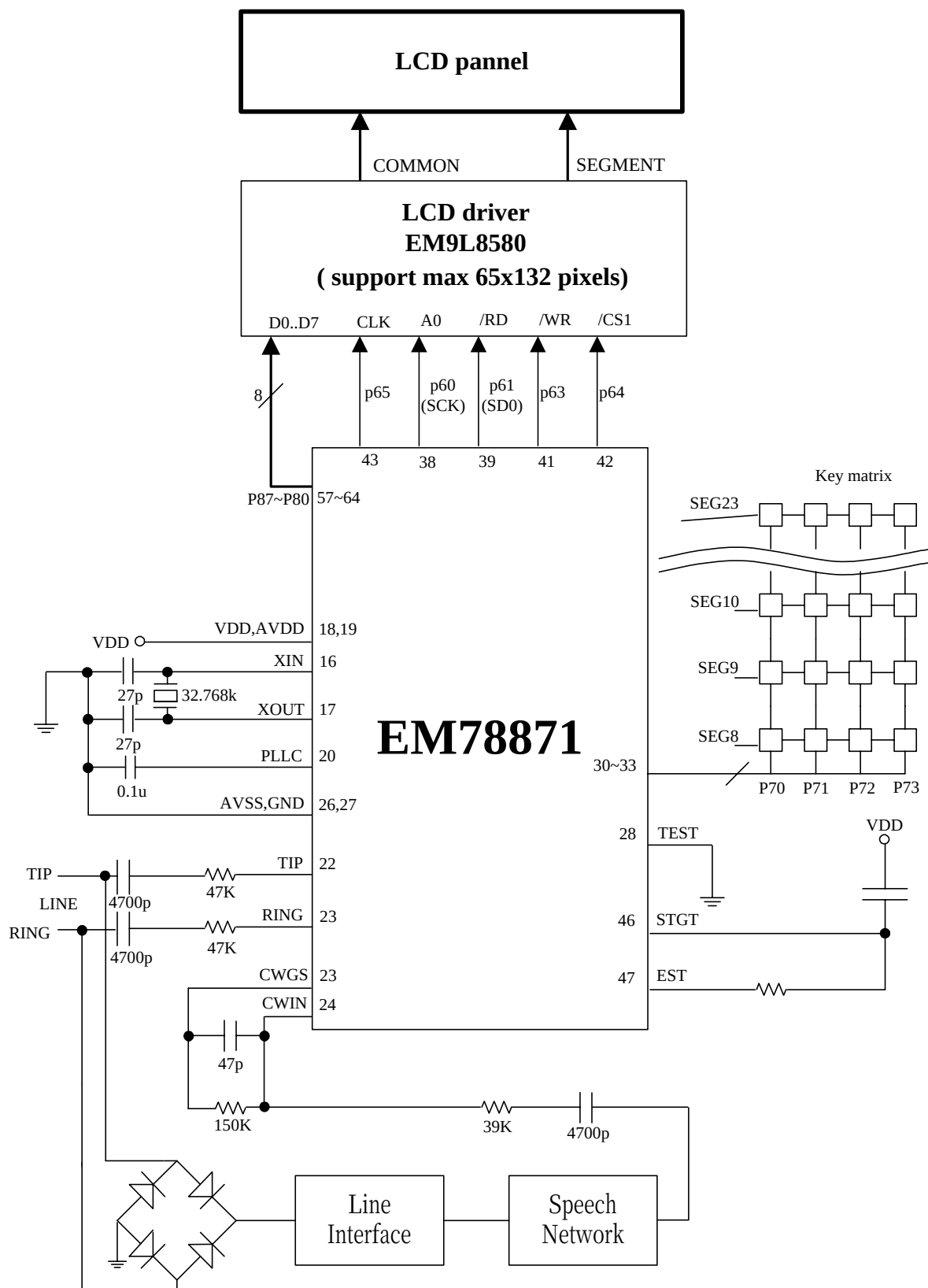


Fig.31 DTMF receiver timing diagram

XII. Application Circuit

(Using 871 built-in LCD driver)





(Using external EMC LCD driver)



附錄: EM78R808 SPEC. (SPEC. is only shown the differences with EM78871)

II.Feature

CPU

- Operating voltage range : 2.2V 5.5V
- 32K×13 Program ROM
- 4M×8 data ROM.
- 8K×8 data RAM

IV.Pin Configuration

COM9	1	SEG45	157	156	SEG46
COM8	2	SEG44	158	155	SEG47
COM7	3	SEG43	159	154	SEG48
COM6	4	SEG42	160	153	SEG49
COM5	5	SEG41	161	152	SEG50
COM4	6	SEG40	162	151	SEG51
COM3	7	SEG39	163	150	SEG52
COM2	8	SEG38	164	149	SEG53
COM1	9	SEG37	165	148	SEG54
COM0	10	SEG36	166	147	SEG55
VC5	11	SEG35	167	146	SEG56
VC4	12	SEG34	168	145	SEG57
VC3	13	SEG33	169	144	SEG58
VC2	14	SEG32	170	143	SEG59
VC1	15	SEG31	171	142	SEG60
XIN	16	SEG30	172	141	SEG61
XOUT	17	SEG29	173	140	SEG62
VDD,AVDD	18	SEG28	174	139	SEG63
PLLC	19	SEG27	175	138	SEG64
TONE	20	SEG26	176	137	SEG65
TIP/EGIN1	21	SEG25	177	136	SEG66
RING/EGIN2	22	SEG24	178	135	SEG67
CWGS	23	SEG23	179	134	SEG68
CWIN	24	SEG22	180	133	SEG69
GND,AVSS	25	SEG21	181	132	SEG70
/RESET	26	SEG20	182	131	SEG71
P70/INT0	27	SEG19	183	130	SEG72
P71/INT0	28	SEG18	184	129	SEG73
P72/INT0	29	SEG17	185	128	SEG74
P73 /INT0	30	SEG16	186	127	SEG75
P74 /INT1	31	SEG15	187	126	SEG76
P75 /INT1	32	SEG14	188	125	SEG77
P76 /INT1	33	SEG13	189	124	SEG78
P77 /INT2	34	SEG12	190	123	SEG79
P60/SCK	35	SEG11	191	122	ROMA19
P61/SDO	36	SEG10	192	121	ROMA18
P62/SDI	37	SEG9	193	120	ROMA17
P63/CMP1	38	SEG8	194	119	ROMA16
P64/CMP2	39	SEG7	195	118	ROMA15
P65/CMP3	40	COM23/SEG7	196	117	ROMA14
P66/DAOUT	41	COM22/SEG6	197	116	ROMA13
P67/KTONE	42	COM21/SEG5	198	115	ROMA12
P55/OP-/STGT	43	COM20/SEG4	199	114	ROMA11
P56/OP+/EST	44	COM19/SEG3	200	113	ROMA10
P57/OP0	45	COM18/SEG2	201	112	ROMA9
ERS	46	COM17/SEG1	202	111	ROMA8
CA-1	47	COM16/SEG0	203	110	ROMA7
CA0	48	COM15	204	109	ROMA6
CA1	49	COM14	205	108	ROMA5
CA2	50	COM13	206	107	ROMA4
CA3	51	COM12	207	106	ROMA3
CA4	52	COM11	208	105	ROMA2
CA5	53	COM10			
CA6	54				
CA7	55				
CA8	56				
CA9	57				
CA10	58				
CA11	59				
CA12	60				
CA13	61				
CA14	62				
CD0	63				
CD1	64				
CD2	65				
CD3	66				
CD4	67				
CD5	68				
CD6	69				
CD7	70				
CD8	71				
CD9	72				
CD10	73				
CD11	74				
CD12	75				
CD13	76				
CD14	77				
CD15	78				
CD16	79				
CD17	80				
CD18	81				
CD19	82				
CD20	83				
CD21	84				
CD22	85				
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CD62	125				
CD63	126				
CD64	127				
CD65	128				
CD66	129				
CD67	130				
CD68	131				
CD69	132				
CD70	133				
CD71	134				
CD72	135				
CD73	136				
CD74	137				
CD75	138				
CD76	139				
CD77	140				
CD78	141				
CD79	142				
CD80	143				
CD81	144				
CD82	145				
CD83	146				
CD84	147				
CD85	148				
CD86	149				
CD87	150				
CD88	151				
CD89	152				
CD90	153				
CD91	154				
CD92	155				
CD93	156				
CD94	157				
CD95	158				
CD96	159				
CD97	160				
CD98	161				
CD99	162				
CD100	163				
CD101	164				
CD102	165				
CD103	166				
CD104	167				
CD105	168				
CD106	169				
CD107	170				
CD108	171				
CD109	172				
CD110	173				
CD111	174				
CD112	175				
CD113	176				
CD114	177				
CD115	178				
CD116	179				
CD117	180				
CD118	181				
CD119	182				
CD120	183				
CD121	184				
CD122	185				
CD123	186				
CD124	187				
CD125	188				
CD126	189				
CD127	190				
CD128	191				
CD129	192				
CD130	193				
CD131	194				
CD132	195				
CD133	196				
CD134	197				
CD135	198				
CD136	199				
CD137	200				
CD138	201				
CD139	202				
CD140	203				
CD141	204				
CD142	205				
CD143	206				
CD144	207				
CD145	208				

Fig .3

2 EM78R808 pin configuration



VI. Pin Descriptions

PIN	I/O	DESCRIPTION
POWER		
VDD AVDD	POWER	Digital power Analog power They connect together when package as 128 pin QFP.
GND AVSS	POWER	Digital ground Analog ground They connect together when package as 128 pin QFP.
CLOCK		
XIN	I	Input pin for 32.768 kHz oscillator
XOUT	O	Output pin for 32.768 kHz oscillator
PLLC	I	Phase loop lock capacitor, connect a capacitor 0.01u to 0.047u with GND
LCD		
COM0..COM15	O	Common driver pins of LCD drivers
SEG0...SEG7 SEG8..SEG47 SEG48..SEG55 SEG56..SEG63 SEG64..SEG71 SEG72..SEG79	O (COM16..COM23) O (I/O : PORTB) O (I/O : PORTC) O (I/O : PORT8) O (I/O : PORT9)	Segment driver pins of LCD drivers SEG0 to SEG7 are share with COM16 to COM23 SEG8 to SEG79 are shared with IO PORT.
VC1..VC5	I	Reference voltage input. Each one connect a capacitor (0.1u) with GND.
FSK , TONE , KTONE		
TIP	I	Should be connected with TIP side of twisted pair lines for FSK.
RING	I	Should be connected with RING side of twisted pair lines for FSK.
TONE	O	Dual tone output pin
KTONE	O (PORT67)	Key tone output. Shared with PORT67.
CW		
CWGS	O	Gain adjustment of single-ended input OP Amp
CWIN	I	Single-ended input OP Amp for call waiting decoder
DTMF receiver		
EST	O	Early steering output. Presents a logic high immediately when the digital algorithm detects a recognizable tone-pair (signal condition). Any momentary loss of signal condition will cause EST to return to a logic low. This pin shared with PORT56.
STGT	I/O	Steering input/guard time output (bi-directional). A voltage greater than V _{tst} detected at ST causes the device to register the detected tone-pair and update the output latch. A voltage less than V _{tst} frees the device to accept a new tone-pair. The GT output acts to reset the external steering time-constant; its state is a function of EST and the voltage on ST . This pin shared with PORT55.
OP		
OP-	I (PORT55)	The negative Vin input pin of the OP. This pin shared with PORT55.
OP+	I (PORT56)	The positive Vin input pin of the OP. This pin shared with PORT56.
OPO	O (PORT57)	The output of OP. This pin shared with PORT57.
SERIAL IO		
SCK	IO (PORT60)	Master: output pin, Slave: input pin. This pin shared with PORT60.
SDO	O (PORT61)	Output pin for serial data transferring. This pin shared with PORT61.



SDI	I (PORT62)	Input pin for receiving data. This pin shared with PORT62.
Comparator		
CMP1	I (PORT63)	Comparator input pins. Shared with PORT63, PORT64 and PORT65.
CMP2	I (PORT64)	
CMP3	I (PORT65)	
CURRENT DA		
DAOUT	O (PORT66)	Current DA output pin. It can be a control signal for sound generating. Shared with PORT66.
IO		
P55 ~ P57	I/O	PORT 5 can be INPUT or OUTPUT port each bit.
P60 ~ P67	I/O	PORT 6 can be INPUT or OUTPUT port each bit. Internal pull high.
P70 ~ P77	I/O	PORT 7 can be INPUT or OUTPUT port each bit. Internal Pull high function. Auto key scan function. Interrupt function.
P80 ~ P87	I/O	PORT 8 can be INPUT or OUTPUT port each bit. Shared with LCD Segment signal.
P90 ~ P97	I/O	PORT 9 can be INPUT or OUTPUT port each bit. Shared with LCD Segment signal.
PB0 ~ PB7	I/O	PORT B can be INPUT or OUTPUT port each bit. Shared with LCD Segment signal.
PC0 ~ PC7	I/O	PORT C can be INPUT or OUTPUT port each bit. Shared with LCD Segment signal.
INT0	PORT70..73	Interrupt sources which has the same interrupt flag. Any pin from PORT70 to PORT73 has a falling edge signal, it will generate a interruption.
INT1	PORT74..76	Interrupt sources which has the same interrupt flag. Any pin from PORT74 to PORT76 has a falling edge signal, it will generate a interruption.
INT2	PORT77	Interrupt source. Once PORT77 has a falling edge or rising edge signal (controlled by CONT register), it will generate a interruption.
/RESET	I	Low reset
X2OUT	O	System clock output.
CA-1	O	CA-1 is used as address line to select low-order data (8 bits, through CD0~CD7) or high-order data (5 bits, through CD0~CD4) ERS=1 => CA-1 NO USE ERS=0 => CA-1=0 HIGH ORDER DATA CA-1=1 LOW ORDER DATA
ERS	I	Input pin used to select the external ROM data bus through bus CD0~D12 or CD0~CD7 only. HIGH/LOW = CD0~CD12 / CD0~CD7.
CA0~CA14	O	Program code address bus. CA0~CA14 are address output pins for external programming ROM access.
CD0~CD12	I	Data access in terms of CA0 ~ CA12 addressing.
IRSEL	O	IRSEL is an output pin used to select an external EVEN/ODD ROM.
INSEND	O	Used to indicate the instruction completion and ready for next instruction.
/HOLD	I	Microcontroller hold request.
IOD0~IOD7	O	I/O data bus.



PH1OUT	O	Phase 1 output	
ROMA0..ROMA19	O	External data ROM address	
ROMD0..ROMD7	IO	External data ROM data bus	
ROMEN1..ROMEN4	O	Data ROM enable pin. User can select one of four external DATA ROM by these enable signal. Please refer to RB address of data ROM.	
		ROMA21,ROMA20	ROMEN4, ROMEN3, ROMEN2, ROMEN1
		0 0	1,1,1,0
		0 1	1,1,0,1
		1 0	1,0,1,1
		1 1	0,1,1,1
ROMREAD	O	External data ROM reading signal. Normal high . When you read data ROM, it will generate a low pulse a instruction long.	
ROMWRITE	O	External data ROM writing signal. Normal high . When you write data ROM, it will generate a low pulse a instruction long.	

VII Operational Registers

R9

PAGE1 (LCD address MSB bit, Data ROM address bits)

7	6	5	4	3	2	1	0
LCDA8	-	DROM_A21	DROM_A20	DROM_A19	DROM_A18	DROM_A17	DROM_A16

Bit 0~Bit 5(DROM_A16~DROM_A21) : Data ROM address(16~21) for ROM reading.

Bit 6 : unused

Bit 7(LCDA8) : MSB of LCD address for LCD RAM reading or writing

Other LCD address bits LCDA7 ~ LCDA0 are set from RA PAGE1 Bit 7 ~ Bit 0.

For LCD address access over 0xFFH, set this bit to "1"; otherwise set this bit to "0".

IOC5

PAGE2 (Stack Pointer)

7	6	5	4	3	2	1	0
STKF	STKM	STKP5	STKP4	STKP3	STKP2	STKP1	STKP0

Bit 0~Bt 5(STKP0~STKP5) : Stack Point selection bits(User must enable CODE Option Register bit 2 before using Stack pointer function)

Stack5	Stack4	STKP3	STKP2	STKP1	STKP0	Stack Point
0	0	0	0	0	0	Stack 0
0	0	0	0	0	1	Stack 1
0	0	0	0	1	0	Stack 2
0	0	0	0	1	1	Stack 3
0	:	:	:	:	:	:
0	:	:	:	:	:	:
0	1	1	1	1	0	Stack 30
0	1	1	1	1	1	Stack 31
1	0	0	0	0	0	Stack 32
:	:	:	:	:	:	:

User can read bit 5 .. bit 0 to understand how many stack layer that program used . Bit 5 .. bit 0 is a six bit counter. The counter will incrementally after user use internal , external interrupt or “CALL” instruction and it will decrement when user use “RET” or “RETI” instruction. When Bit6(STKM) is set to 1 and bit 5 .. bit 0 are 0b011110 → 0b011111 , interrupt will occur.

Bit 6(STKM) : Stack overflow mask bit.

0 → STK interrupt disable.

1 → STK interrupt enable.

Bit 7(STKF) : Stack Point overflow interrupt flag bit.

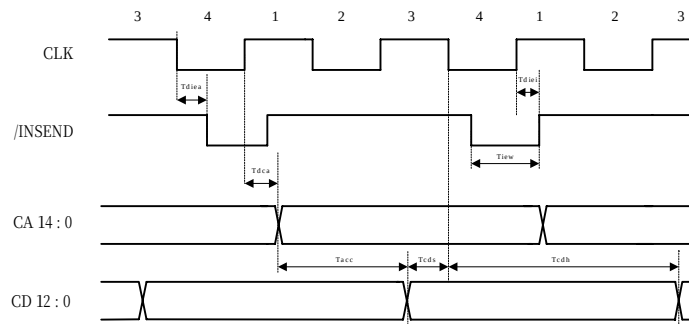
STKF will set to 1 when bit 5 .. bit 0 are 0b011110 → 0b011111

IX AC Electrical Characteristic

Tdiea	Delay from Phase 3 end to INSEND active	Cl=100pF			30	ns
Tdiei	Delay from Phase 4 end to INSEND inactive	Cl=100pF			30	ns
Tiew	INSEND pulse width		30			ns
Tdca	Delay from Phase 4 end to CA Bus valid	C1=100pF			30	ns
Tacc	ROM data access time		100			ns
Tcds	ROM data setup time		20			ns
Tcdh	ROM data hold time		20			ns
Tdca-1	Delay time of CA-1	C1=100pF			30	ns

Note 1: N= selected prescaler ratio.

ERS=1 , CA-1=DISABLE



ERS=0 , CA-1=0 HIGH ORDER DATA
CA-1=1 LOW ORDER DATA

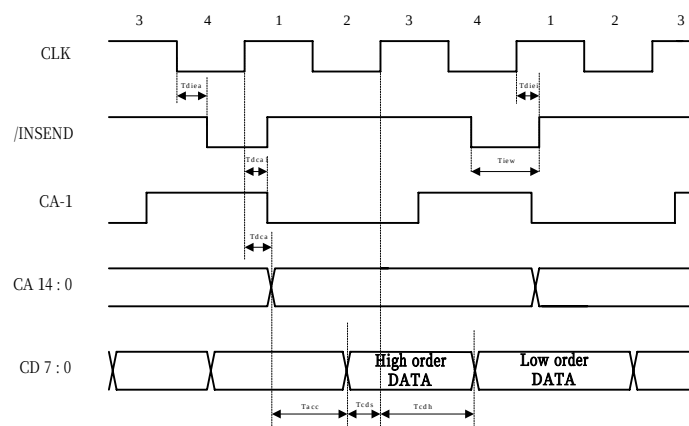


Fig.33 Program ROM access timing